

N-channel 30 V 3.3 mΩ logic level MOSFET in D2PAK

Rev. 1 — 22 March 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

| Table 1. | Quick reference data | | | | | | |
|---------------------|---|---|-----|-----|------|-----|------|
| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
| V _{DS} | drain-source voltage | T _j ≥ 25 °C; T _j ≤ 175 °C | | - | - | 30 | V |
| I _D | drain current | T _{mb} = 25 °C; V _{GS} = 10 V; see <u>Figure 1</u> | [1] | - | - | 100 | Α |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; see <u>Figure 2</u> | | - | - | 114 | W |
| Tj | junction temperature | | | -55 | - | 175 | °C |
| Static cha | aracteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; see <u>Figure 12</u> ; see <u>Figure 13</u> | | - | 3.91 | 4.6 | mΩ |
| | | $\label{eq:VGS} \begin{array}{l} V_{GS} = 10 \ V; \ I_D = 25 \ A; \ T_j = 25 \ ^\circ C; \\ \text{see } \overline{Figure \ 13} \end{array}$ | | - | 2.79 | 3.3 | mΩ |
| Dynamic | characteristics | | | | | | |
| Q _{GD} | gate-drain charge | V_{GS} = 4.5 V; I_{D} = 25 A; V_{DS} = 15 V; | | - | 8 | - | nC |
| Q _{G(tot)} | total gate charge | see Figure 14; see Figure 15 | | - | 31 | - | nC |
| | e ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $\label{eq:GS} \begin{array}{l} V_{GS} = 10 \ V; \ T_{j(init)} = 25 \ ^{\circ}C; \\ I_{D} = 100 \ A; \ V_{sup} \leq 30 \ V; \ R_{GS} = 50 \ \Omega; \\ unclamped \end{array}$ | | - | - | 200 | mJ |

[1] Continuous current is limited by package.

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2. Pinning information

| Table 2. | Pinning | information | | | |
|----------|---------|-----------------------------------|--------------------|----------------|--|
| Pin | Symbol | Description | Simplified outline | Graphic symbol | |
| 1 | G | gate | | | |
| 2 | D | drain ^[1] | mb | | |
| 3 | S | source | | | |
| mb | D | mounting base; connected to drain | | mbb076 S | |
| | | | SOT404 (D2PAK) | | |

[1] it is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information Type number Package Name Description Version PSMN3R4-30BL D2PAK plastic single-ended surface-mounted package (D2PAK); 3 leads SOT404 (one lead cropped)

4. Marking

| Table 4. Marking codes | |
|--------------------------------|--------------|
| Type number | Marking code |
| PSMN3R4-30BL | PSMN3R4-30BL |

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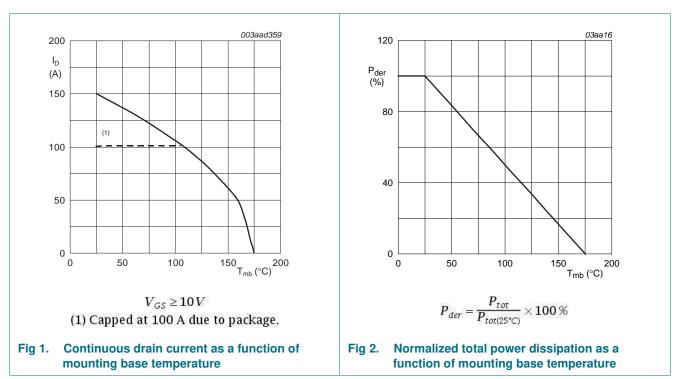
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Мах | Unit |
|----------------------|--|--|-----|-----|-----|------|
| V _{DS} | drain-source voltage | T _j ≥ 25 °C; T _j ≤ 175 °C | | - | 30 | V |
| V _{DGR} | drain-gate voltage | T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ | | - | 30 | V |
| V _{GS} | gate-source voltage | | | -20 | 20 | V |
| I _D | drain current | V_{GS} = 10 V; T_{mb} = 100 °C; see <u>Figure 1</u> | [1] | - | 100 | А |
| | | V_{GS} = 10 V; T_{mb} = 25 °C; see <u>Figure 1</u> | [1] | - | 100 | А |
| I _{DM} | peak drain current | pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$; see Figure 3 | | - | 609 | А |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; see <u>Figure 2</u> | | - | 114 | W |
| T _{stg} | storage temperature | | | -55 | 175 | °C |
| Tj | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| Source-dra | ain diode | | | | | |
| I _S | source current | T _{mb} = 25 °C | [1] | - | 100 | А |
| I _{SM} | peak source current | pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$ | | - | 609 | А |
| Avalanche | ruggedness | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; unclamped | | - | 200 | mJ |

[1] Continuous current is limited by package.



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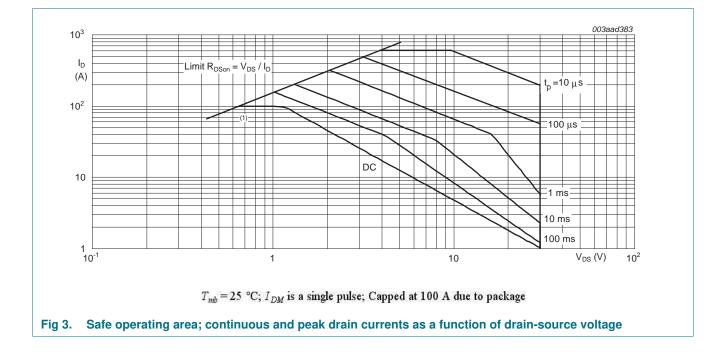


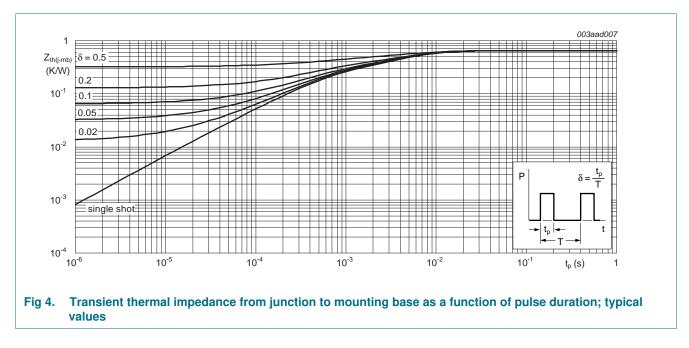
Table C

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6. Thermal characteristics

The word is here stavistics

| Table 6. | I nermal characteristics | | | | | |
|----------------------|---|--|-----|------|-----|------|
| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | 0.65 | 1 | K/W |
| R _{th(j-a)} | thermal resistance from junction to ambient | Minimum foot print; mounted on a printed circuit board | - | 50 | - | K/W |



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7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---|-----------------------------------|---|-----|------|------|------|
| Static char | acteristics | | | | | |
| V _{(BR)DSS} | drain-source breakdown voltage | $I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^\circ C$ | 30 | - | - | V |
| | | $I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^\circ C$ | 27 | - | - | V |
| V _{GS(th)} | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see <u>Figure 10</u> ; see <u>Figure 11</u> | 1.3 | 1.7 | 2.15 | V |
| | | $\label{eq:ID} \begin{split} I_D &= 1 \text{ mA; } V_{DS} = V_{GS} \text{; } T_j = 175 \ ^\circ\text{C} \text{;} \\ \text{see } \overline{\text{Figure } 11} \end{split}$ | 0.5 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ see Figure 11 | - | - | 2.45 | V |
| I _{DSS} | drain leakage current | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$ | - | 0.3 | 5 | μA |
| | | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$ | - | - | 100 | μA |
| I _{GSS} | gate leakage current | V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C | - | 10 | 100 | nA |
| | | V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C | - | 10 | 100 | nA |
| R _{DSon} drain-source on-state resista | drain-source on-state resistance | V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see <u>Figure 12</u> ; see <u>Figure 13</u> | - | 5.3 | 6.2 | mΩ |
| | | V_{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; see <u>Figure 13</u> | - | 3.27 | 3.8 | mΩ |
| | | V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; see <u>Figure 12</u> ; see <u>Figure 13</u> | - | 3.91 | 4.6 | mΩ |
| | | V_{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see <u>Figure 13</u> | - | 2.79 | 3.3 | mΩ |
| R _G | gate resistance | f = 1 MHz | - | 1 | - | Ω |
| Dynamic c | haracteristics | | | | | |
| Q _{G(tot)} | total gate charge | $I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14; see Figure 15 | - | 64 | - | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$ | - | 58 | - | nC |
| | | $I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ | - | 31 | - | nC |
| Q _{GS} | gate-source charge | see Figure 14; see Figure 15 | - | 12 | - | nC |
| Q _{GS(th)} | pre-threshold gate-source charge | | - | 6.2 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 5.8 | - | nC |
| Q _{GD} | gate-drain charge | | - | 8 | - | nC |
| $V_{GS(\text{pl})}$ | gate-source plateau voltage | $I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; \text{see } \frac{\text{Figure } 14}{\text{Figure } 15};$ see $\frac{\text{Figure } 15}{\text{Figure } 15}$ | - | 2.8 | - | V |
| C _{iss} | input capacitance | V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz; | - | 3907 | - | pF |
| C _{oss} | output capacitance | T _j = 25 °C; see <u>Figure 16</u> | - | 822 | - | pF |
| C _{rss} | reverse transfer capacitance | | - | 356 | - | pF |

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Table 7. Characteristics ...continued

Tested to JEDEC standards where applicable.

| | | <u>-</u> | | | | |
|---------------------|-----------------------|---|-----|-----|-----|------|
| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
| t _{d(on)} | turn-on delay time | $V_{DS} = 15 \; V; \; R_L = 0.5 \; \Omega; \; V_{GS} = 4.5 \; V; \;$ | - | 40 | - | ns |
| t _r | rise time | $R_{G(ext)} = 4.7 \ \Omega$ | - | 73 | - | ns |
| t _{d(off)} | turn-off delay time | | - | 59 | - | ns |
| t _f | fall time | | | 28 | - | ns |
| Source-dr | ain diode | | | | | |
| V_{SD} | source-drain voltage | I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see <u>Figure 17</u> | - | 0.7 | 1.2 | V |
| t _{rr} | reverse recovery time | $I_{S} = 25 \text{ A}; \text{ d}I_{S}/\text{d}t = -100 \text{ A}/\mu\text{s};$ | - | 36 | - | ns |
| Q _r | recovered charge | $V_{GS} = 0 V; V_{DS} = 15 V$ | - | 28 | - | nC |
| | | | | | | |

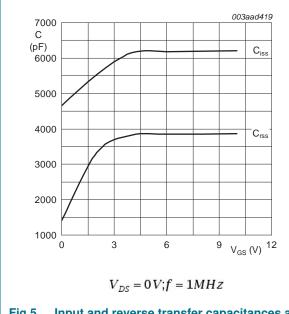


Fig 5. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

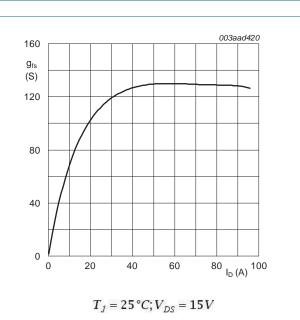
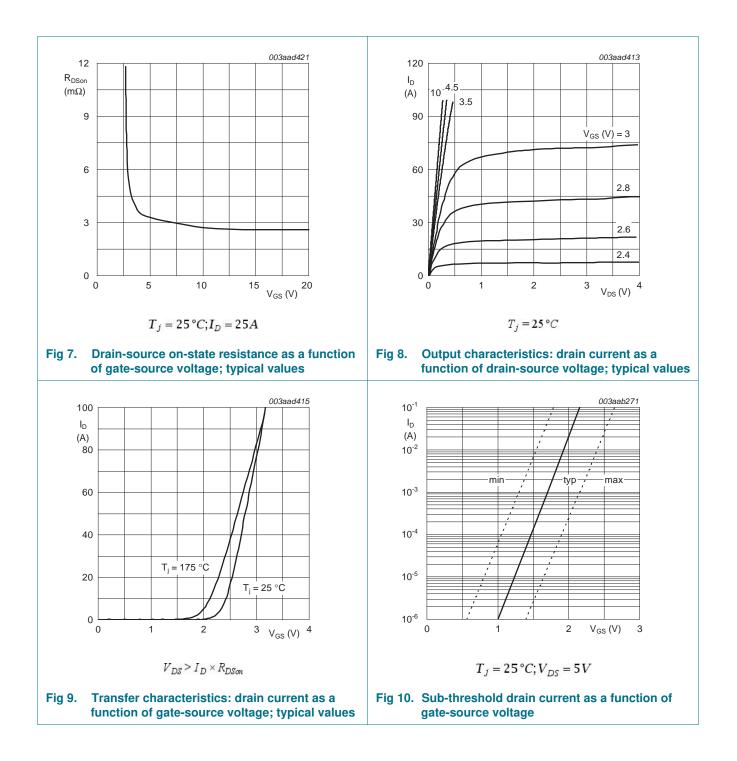


Fig 6. Forward transconductance as a function of drain current; typical values

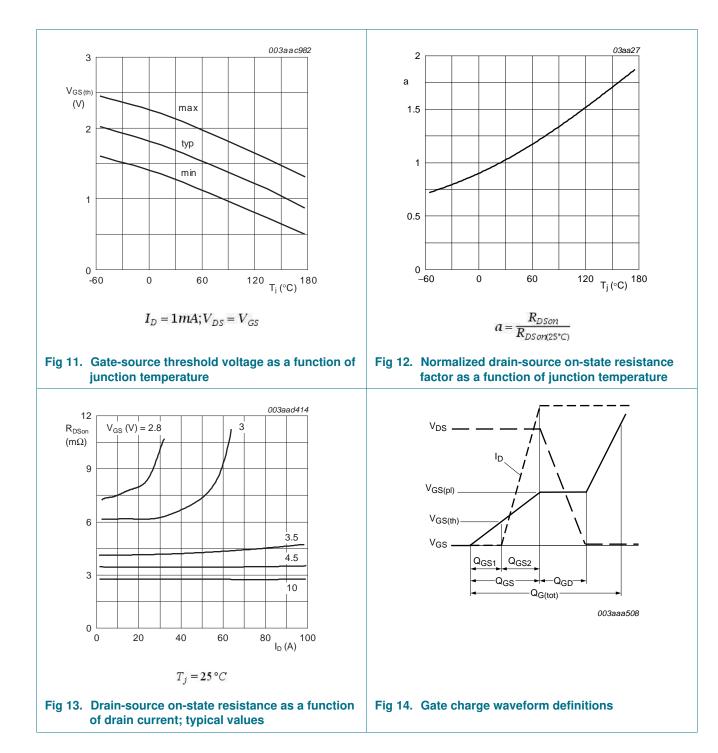
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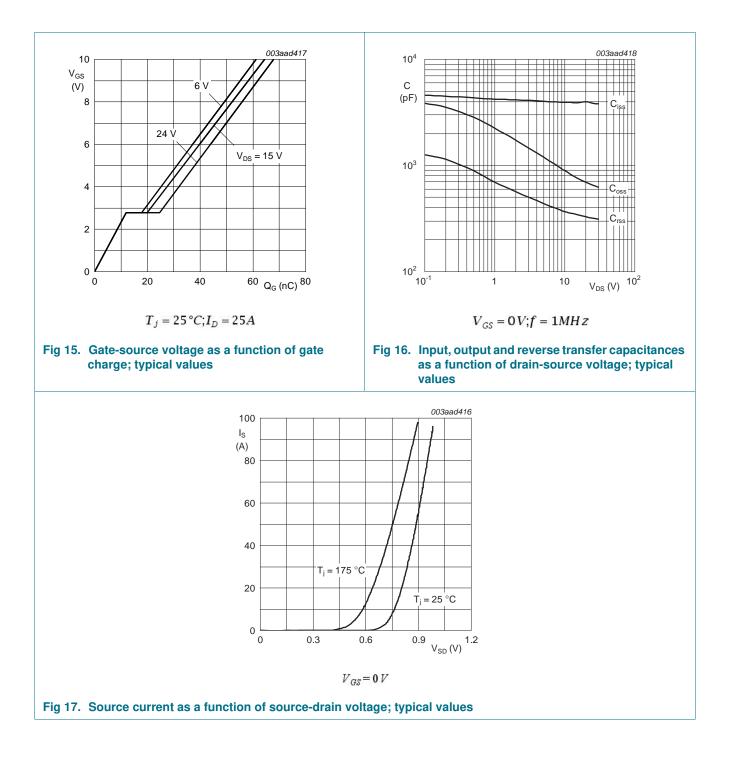
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N-channel 30 V 3.3 m Ω logic level MOSFET in D2PAK



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8. Package outline

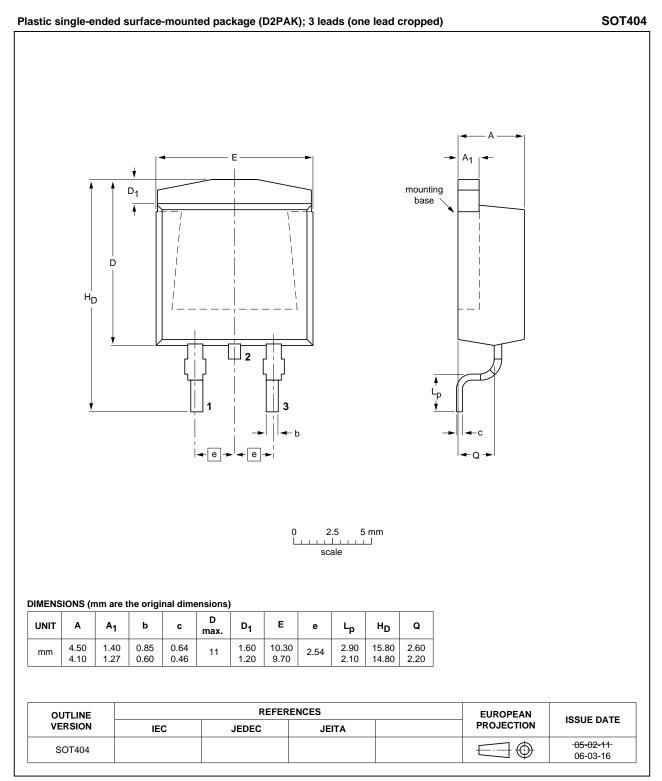


Fig 18. Package outline SOT404 (D2PAK)

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9. Revision history

| Table 8. Revision h | Revision history | | | | | | | |
|---------------------|------------------|--------------------|---------------|------------|--|--|--|--|
| Document ID | Release date | Data sheet status | Change notice | Supersedes | | | | |
| PSMN3R4-30BL v.1 | 20120322 | Product data sheet | - | - | | | | |

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|--------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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