BGA7L1N6

Silicon Germanium Low Noise Amplifier for LTE

Data Sheet

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RF & Protection Devices

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 3.1 (Min/Max), 2014-02-11	
10-15	Min/Max values added
Revision 3.0, 2014-02-10	
7	Marking added
10-15	Electrical characteristics updated
10-15	Footnotes updated

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Silicon Germanium Low Noise Amplifier for LTE **BGA7L1N6**

Features

- Insertion power gain: 13.3 dB
- Low noise figure: 0.90 dB
- Low current consumption: 4.4 mA
- Operating frequencies: 728 - 960 MHz
- Supply voltage: 1.5 V to 3.3 V
- Digital on/off switch (1V logic high level)
- Ultra small TSNP-6-2 leadless package (footprint: 0.7 x 1.1 mm^2)
- B7HF Silicon Germanium technology
- RF output internally matched to 50 Ω
- Only 1 external SMD component necessary
- 2kV HBM ESD protection (including AI-pin)
- Pb-free (RoHS compliant) package

RoHS

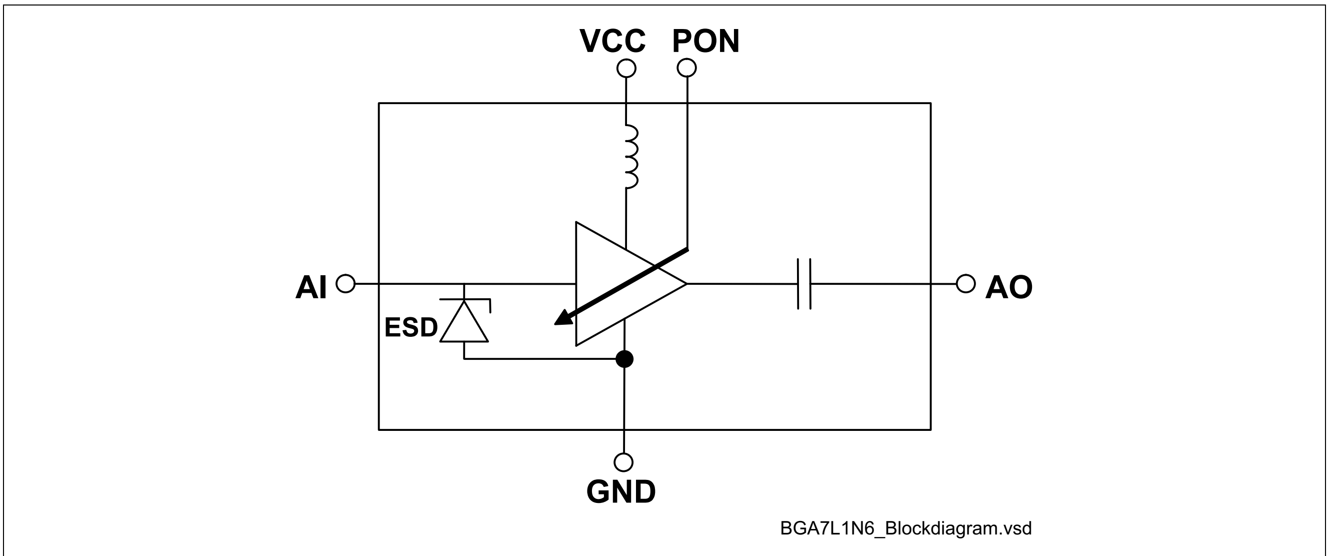

Figure 1 Block Diagram

Product Name	Marking	Package
BGA7L1N6	C	TSNP-6-2

Description

The BGA7L1N6 is a front-end low noise amplifier for LTE which covers a wide frequency range from 728 MHz to 960 MHz. The LNA provides 13.3 dB gain and 0.90 dB noise figure at a current consumption of 4.4 mA in the application configuration described in **Chapter 3**. The BGA7L1N6 is based upon Infineon Technologies‘ B7HF Silicon Germanium technology. It operates from 1.5 V to 3.3 V supply voltage.

Pin Definition and Function

Table 1 Pin Definition and Function

Pin No.	Name	Function
1	GND	Ground
2	VCC	DC supply
3	AO	LNA output
4	GND	Ground
5	AI	LNA input
6	PON	Power on control

1 Maximum Ratings

Table 2 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at pin VCC	V_{CC}	-0.3	–	3.6	V	1)
Voltage at pin AI	V_{AI}	-0.3	–	0.9	V	–
Voltage at pin AO	V_{AO}	-0.3	–	V_{CC} + 0.3	V	–
Voltage at pin PON	V_{PON}	-0.3	–	V_{CC} + 0.3	V	–
Voltage at pin GNDRF	V_{GNDRF}	-0.3	–	0.3	V	–
Current into pin VCC	I_{CC}	–	–	16	mA	–
RF input power	P_{IN}	–	–	0	dBm	–
Total power dissipation, T_S < tbd. °C[2]	P_{tot}	–	–	60	mW	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{STG}	-65	–	150	°C	–
ESD capability all pins	V_{ESD_HBM}	–	–	2000	V	according to JESD22A-114

1) All voltages refer to GND-Node unless otherwise noted

2) T_S is measured on the ground lead at the soldering point

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Thermal Resistance

Table 3 Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[1]	R_{thJS}	tbd.	K/W

1) For calculation of R_{thJA} please refer to Application Note Thermal Resistance

2 Electrical Characteristics

2.1 Measured RF Characteristics Band 5

Table 4 Electrical Characteristics:[1] T_A = 25 °C, V_{CC} = 1.8 V, $V_{PON,ON}$ = 1.8 V, $V_{PON,OFF}$ = 0 V, f = 869 - 894 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.3	V	–
Supply current	I_{CC}	–	4.4	5.4	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Power On voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{pon}	–	5	10	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	11.8	13.3	14.8	dB	–
Noise figure[2]	NF	–	0.9	1.5	dB	Z_S = 50 Ω
Input return loss[3]	RL_{in}	10	25	–	dB	–
Output return loss[3]	RL_{out}	10	17	–	dB	–
Reverse isolation[3]	$1/\|S_{12}\|^2$	17	21	–	dB	–
Power gain settling time[4][5]	t_S	–	4	7	µs	OFF- to ON-mode
Inband input 1dB-compression point[3]	IP_{1dB}	-10	-6	–	dBm	–
Inband input 3rd-order intercept point[6][3]	IIP_3	-6	-1	–	dBm	f_1 = 880 MHz $f_2 = f_1$ +/-1 MHz
Stability[5]	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) Verification based on AQL; not 100% tested in production
4) To be within 1 dB of the final gain
5) Guaranteed by device design; not tested in production
6) Input power = -30 dBm for each tone

Table 5 Electrical Characteristics:[1] T_A **= 25 °C,** V_{CC} **= 2.8 V,** $V_{PON,ON}$ **= 2.8 V,** $V_{PON,OFF}$ **= 0 V,** f **= 869 - 894 MHz**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.3	V	–
Supply current	I_{CC}	–	4.5	5.5	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Power On voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{pon}	–	10	15	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	11.8	13.3	14.8	dB	–
Noise figure[2]	NF	–	0.9	1.5	dB	$Z_S = 50\ \Omega$
Input return loss[3]	RL_{in}	10	24	–	dB	–
Output return loss[3]	RL_{out}	10	15	–	dB	–
Reverse isolation[3]	$1/\|S_{12}\|^2$	18	22	–	dB	–
Power gain settling time[4][5]	t_S	–	3	6	µs	OFF- to ON-mode
Inband input 1dB-compression point[3]	IP_{1dB}	-7	-3	–	dBm	–
Inband input 3rd-order intercept point[6][3]	IIP_3	-5	0	–	dBm	f_1 = 880 MHz $f_2 = f_1$ +/-1 MHz
Stability[5]	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) Verification based on AQL; not 100% tested in production
4) To be within 1 dB of the final gain
5) Guaranteed by device design; not tested in production
6) Input power = -30 dBm for each tone

2.2 Measured RF Characteristics Band 8

Table 6 Electrical Characteristics:[1] T_A = 25 °C, V_{CC} = 1.8 V, $V_{PON,ON}$ = 1.8 V, $V_{PON,OFF}$ = 0 V, f = 925 - 960 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.3	V	–
Supply current	I_{CC}	–	4.4	5.4	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Power On voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{pon}	–	5	10	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	11.5	13.0	14.5	dB	–
Noise figure[2]	NF	–	0.9	1.5	dB	Z_S = 50 Ω
Input return loss[3]	RL_{in}	10	16	–	dB	–
Output return loss[3]	RL_{out}	10	25	–	dB	–
Reverse isolation[3]	$1/\|S_{12}\|^2$	17	21	–	dB	–
Power gain settling time[4)5)]	t_S	–	4	7	µs	OFF- to ON-mode
Inband input 1dB-compression point[3]	IP_{1dB}	-10	-6	–	dBm	–
Inband input 3rd-order intercept point[6)3)]	IIP_3	-4	+1	–	dBm	f_1 = 940 MHz $f_2 = f_1$ +/-1 MHz
Stability[5]	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) Verification based on AQL; not 100% tested in production
4) To be within 1 dB of the final gain
5) Guaranteed by device design; not tested in production
6) Input power = -30 dBm for each tone

Table 7 Electrical Characteristics:[1] T_A = 25 °C, V_{CC} = 2.8 V, $V_{PON,ON}$ = 2.8 V, $V_{PON,OFF}$ = 0 V, f = 925 - 960 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.3	V	–
Supply current	I_{CC}	–	4.5	5.5	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Power On voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{pon}	–	10	15	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	11.6	13.1	14.6	dB	–
Noise figure[2]	NF	–	0.9	1.5	dB	Z_S = 50 Ω
Input return loss[3]	RL_{in}	10	17	–	dB	–
Output return loss[3]	RL_{out}	10	23	–	dB	–
Reverse isolation[3]	$1/\|S_{12}\|^2$	17	21	–	dB	–
Power gain settling time[4)5)]	t_S	–	3	6	µs	OFF- to ON-mode
Inband input 1dB-compression point[3]	IP_{1dB}	-6	-2	–	dBm	–
Inband input 3rd-order intercept point[6)3)]	IIP_3	-3	+2	–	dBm	f_1 = 940 MHz $f_2 = f_1$ +/-1 MHz
Stability[5]	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) Verification based on AQL; not 100% tested in production
4) To be within 1 dB of the final gain
5) Guaranteed by device design; not tested in production
6) Input power = -30 dBm for each tone

2.3 Measured RF Characteristics Band 17

Table 8 Electrical Characteristics:[1] T_A = 25 °C, V_{CC} = 1.8 V, $V_{PON,ON}$ = 1.8 V, $V_{PON,OFF}$ = 0 V, f = 734 - 746 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.3	V	–
Supply current	I_{CC}	–	4.4	5.4	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Power On voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{pon}	–	5	10	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	11.1	12.6	14.1	dB	–
Noise figure[2]	NF	–	0.9	1.5	dB	Z_S = 50 Ω
Input return loss[3]	RL_{in}	6	9	–	dB	–
Output return loss[3]	RL_{out}	6	8	–	dB	–
Reverse isolation[3]	$1/\|S_{12}\|^2$	20	24	–	dB	–
Power gain settling time[4][5]	t_S	–	4	7	µs	OFF- to ON-mode
Inband input 1dB-compression point[3]	IP_{1dB}	-12	-8	–	dBm	–
Inband input 3rd-order intercept point[6][3]	IIP_3	-7	-2	–	dBm	f_1 = 740 MHz $f_2 = f_1$ +/-1 MHz
Stability[5]	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) Verification based on AQL; not 100% tested in production
4) To be within 1 dB of the final gain
5) Guaranteed by device design; not tested in production
6) Input power = -30 dBm for each tone

Table 9 Electrical Characteristics:[1] T_A = 25 °C, V_{CC} = 2.8 V, $V_{PON,ON}$ = 2.8 V, $V_{PON,OFF}$ = 0 V, f = 734 - 746 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.3	V	–
Supply current	I_{CC}	–	4.5	5.5	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Power On voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{pon}	–	10	15	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	11.1	12.6	14.1	dB	–
Noise figure[2]	NF	–	0.9	1.5	dB	Z_S = 50 Ω
Input return loss[3]	RL_{in}	6	9	–	dB	–
Output return loss[3]	RL_{out}	6	8	–	dB	–
Reverse isolation[3]	$1/\|S_{12}\|^2$	21	25	–	dB	–
Power gain settling time[4][5]	t_S	–	3	6	µs	OFF- to ON-mode
Inband input 1dB-compression point[3]	IP_{1dB}	-10	-6	–	dBm	–
Inband input 3rd-order intercept point[6][3]	IIP_3	-7	-2	–	dBm	f_1 = 740 MHz $f_2 = f_1$ +/-1 MHz
Stability[5]	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) Verification based on AQL; not 100% tested in production
4) To be within 1 dB of the final gain
5) Guaranteed by device design; not tested in production
6) Input power = -30 dBm for each tone

3 Application Information

3.1 Application Circuit Schematic Band 5

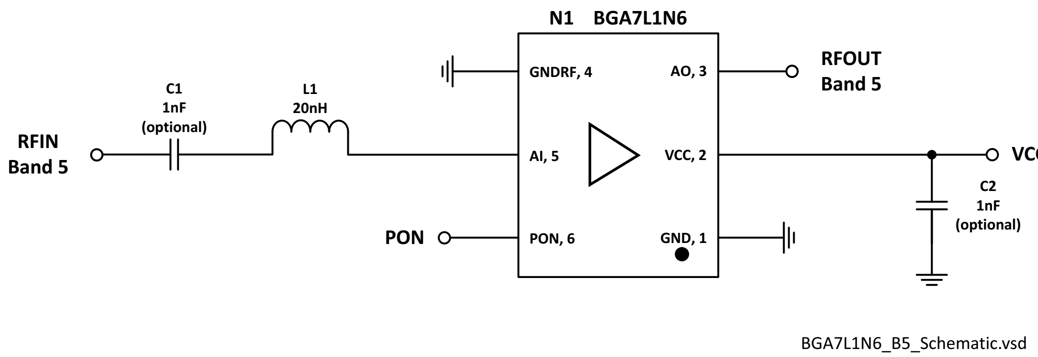

Figure 2 Application Schematic BGA7L1N6

Table 10 Bill of Materials

Name	Part Type	Package	Manufacturer	Function
C1 (optional)	Chip capacitor	0402	Various	DC block [1]
C2 (optional)	≥ 1nF[2]	0402	Various	RF bypass [3]
L1	Chip inductor	0402	Murata LQW type	Input matching
N1	BGA7L1N6	TSNP-6-2	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in LTE applications
2) For data sheet characteristics 1nF used
3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at **http://www.infineon.com/gpslna.appnotes**.

3.2 Application Circuit Schematic Band 8

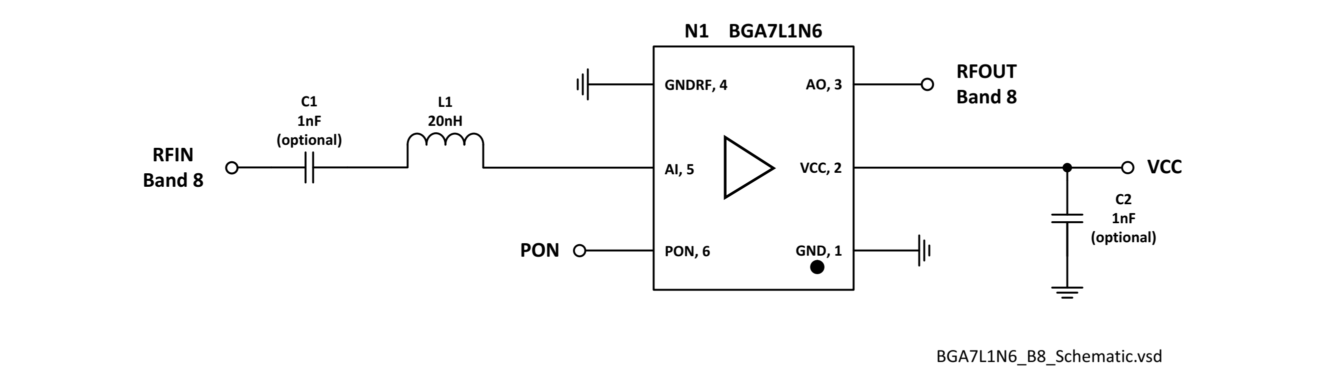

Figure 3 Application Schematic BGA7L1N6

Table 11 Bill of Materials

Name	Part Type	Package	Manufacturer	Function
C1 (optional)	Chip capacitor	0402	Various	DC block 1)
C2 (optional)	≥ 1nF2)	0402	Various	RF bypass 3)
L1	Chip inductor	0402	Murata LQW type	Input matching
N1	BGA7L1N6	TSNP-6-2	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in LTE applications
2) For data sheet characteristics 1nF used
3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at **http://www.infineon.com/gpslna.appnotes**.

3.3 Application Circuit Schematic Band 17

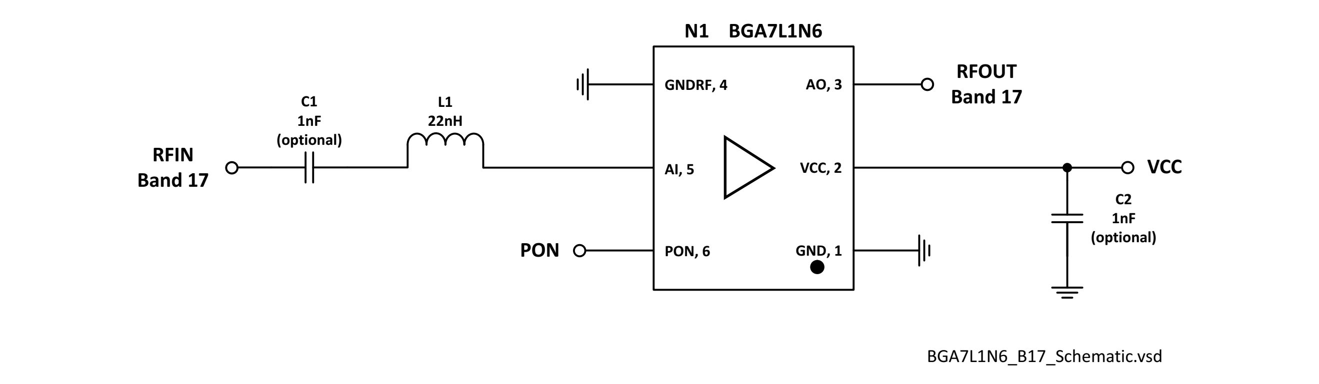

Figure 4 Application Schematic BGA7L1N6

Table 12 Bill of Materials

Name	Part Type	Package	Manufacturer	Function
C1 (optional)	Chip capacitor	0402	Various	DC block 1)
C2 (optional)	≥ 1nF 2)	0402	Various	RF bypass 3)
L1	Chip inductor	0402	Murata LQW type	Input matching
N1	BGA7L1N6	TSNP-6-2	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in LTE applications
2) For data sheet characteristics 1nF used
3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at **http://www.infineon.com/gpslna.appnotes**.

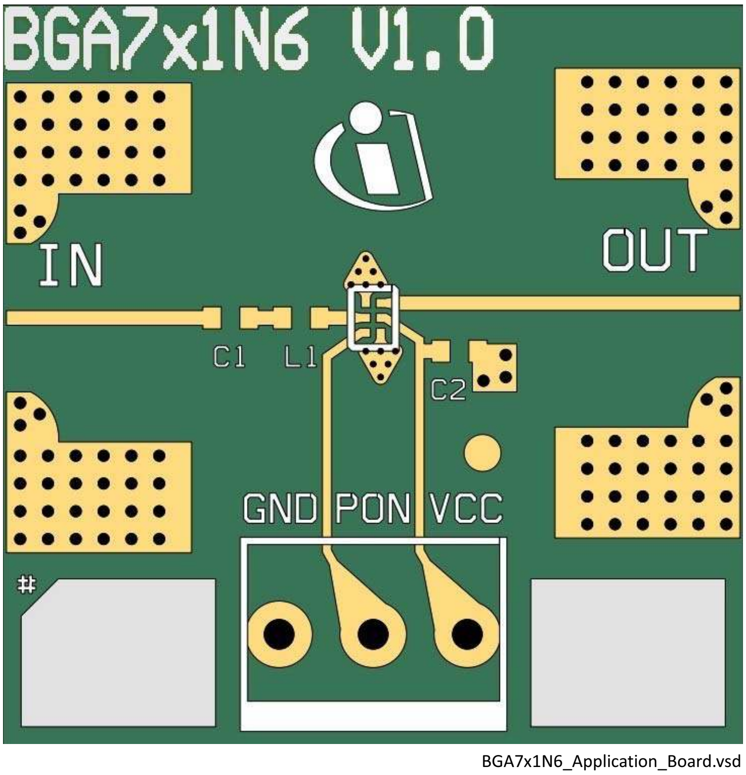

Figure 5 Drawing of Application Board

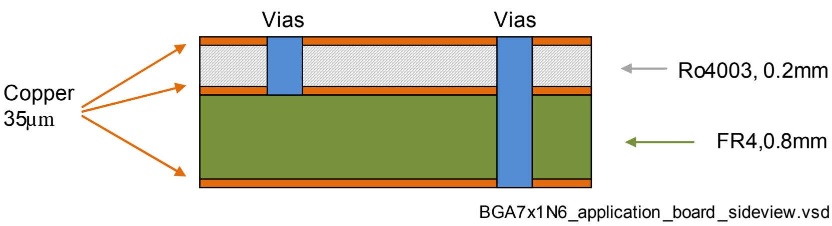

Figure 6 Application Board Cross-Section

4 Package Information

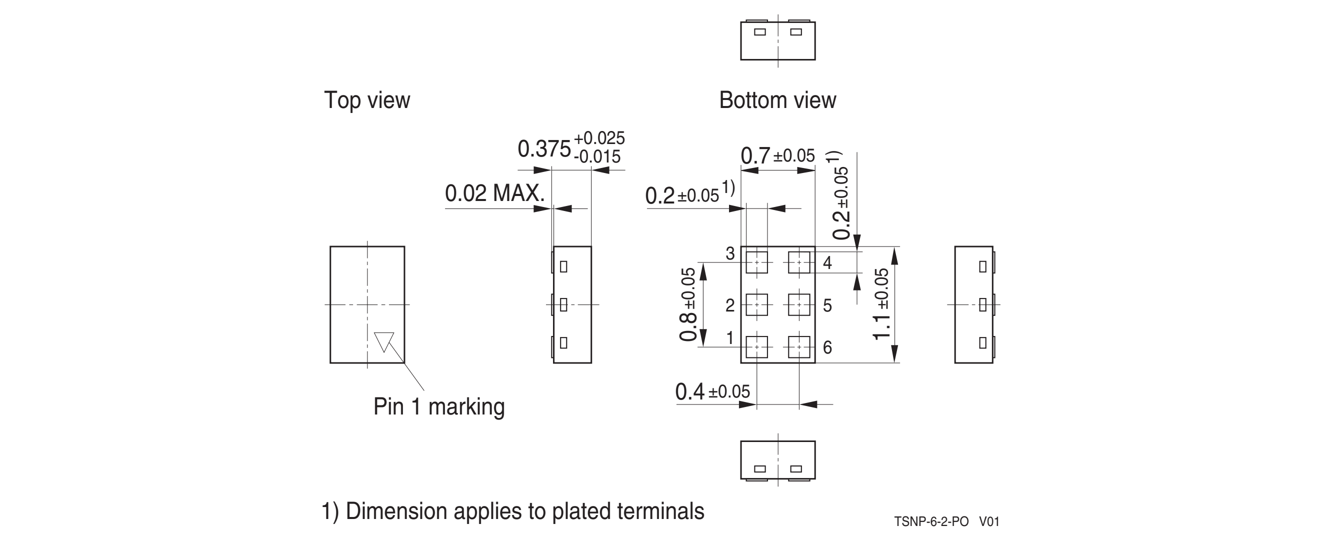

Figure 7 TSNP-6-2 Package Outline (top, side and bottom views)

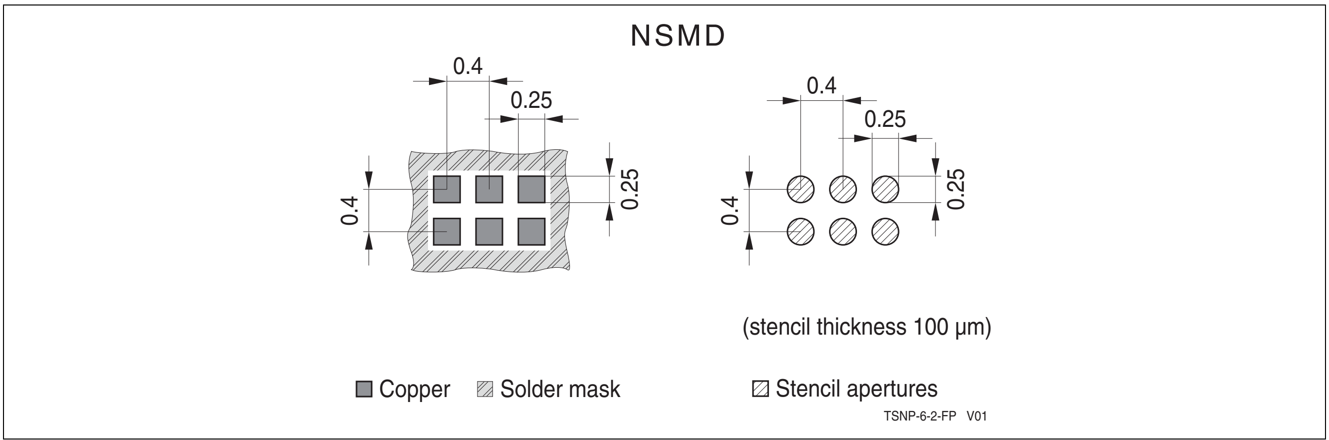

Figure 8 Footprint Recommendation TSNP-6-2

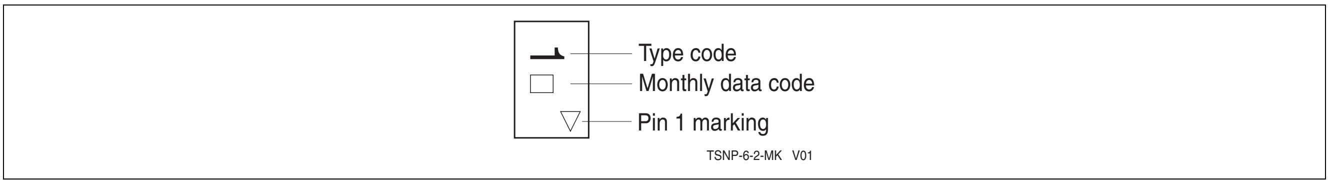

Figure 9 Marking Layout (top view)

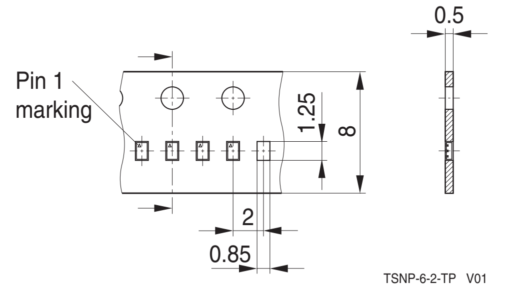

Figure 10 Tape & Reel Dimensions (reel diameter 180 mm, pieces/reel 15000)

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