

File Number 2341

D42C Series

T-33-05

3-Ampere Silicon N-P-N Power Transistors

Complementary to the D43C Series

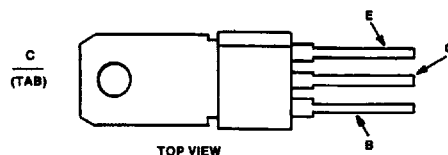
Features:

- High free-air power dissipation
- Low collector saturation voltage (0.5V typ. @ 3A I_C)
- Excellent linearity
- Fast switching

The D42C-series of silicon n-p-n power transistors are designed for various specific and general purpose applications, such as: output and driver stages of amplifiers operating at frequencies from DC to greater than 1 MHz; series, shunt and switching regulators; and low and high frequency inverters/converters.

These devices are supplied in the JEDEC TO-202AB plastic package.

TERMINAL DESIGNATIONS



92CS-43473

JEDEC TO-202AB

POWER TRANSISTORS

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$) (unless otherwise specified)

RATING	SYMBOL	D42C1, 2, 3	D42C4, 5, 6	D42C7, 8, 9	D42C10, 11, 12	UNITS
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Volts
Collector-Emitter Voltage	V_{CES}	40	55	70	90	Volts
Emitter Base Voltage	V_{EBO}	5	5	5	5	Volts
Collector Current — Continuous	I_C	3	3	3	3	A
Peak ⁽¹⁾	I_{CM}	5	5	5	5	A
Base Current — Continuous	I_B	2	2	2	2	A
Total Power Dissipation ¹ @ $T_A = 25^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$	P_D	2.1 12.5	2.1 12.5	2.1 12.5	2.1 12.5	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	60	60	60	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	10	10	10	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: $\frac{1}{8}$ " from Case for 5 Seconds	T_L	+260	+260	+260	+260	$^\circ\text{C}$

(1) Pulse Test Pulse Width = 300ms Duty Cycle \leq 2%.

D42C Series

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ELECTRICAL CHARACTERISTICS (T_C = 25°C) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
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OFF CHARACTERISTICS⁽¹⁾

Collector-Emitter Sustaining Voltage (I _C = 100mA)	D42C1, 2, 3 D42C4, 5, 6 D42C7, 8, 9 D42C10, 11, 12	V _{CEO(sus)}	30 45 60 80	— — — —	— — — —	Volts
Collector Cutoff Current (V _{CE} = Rated V _{CE})		I _{CES}	—	—	10	μA
Emitter Cutoff Current (V _{EB} = 5V)		I _{EBO}	—	—	100	μA

SECOND BREAKDOWN

Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURES 3 & 4
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ON CHARACTERISTICS⁽¹⁾

DC Current Gain (I _C = 200mA, V _{CE} = 1V)	D42C1, 4, 7, 10 D42C2, 5, 8, 11 D42C3, 6, 9, 12	h _{FE}	25 100 40	— — —	— 220 120	—
(I _C = 1A, V _{CE} = 1V) (I _C = 2A, V _{CE} = 1V)	D42C1, 4, 7, 10 D42C2, 5, 8, 11 D42C3, 6, 9, 12	h _{FE}	10 20 20	— — —	— — —	—
Collector-Emitter Saturation Voltage (I _C = 1A, I _B = 50mA)	D42C2, 5, 8, 11 D42C3, 6, 9, 12	V _{CE(sat)}	— —	— —	0.5 0.5	Volts
(I _C = 1A, I _B = 100mA)	D42C1, 4, 7, 10	V _{CE(sat)}	—	—	0.5	Volts
Base-Emitter Saturation Voltage (I _C = 1A, I _B = 100mA)		V _{BE(sat)}	—	—	1.3	Volts

DYNAMIC CHARACTERISTICS

Collector Capacitance (V _{CB} = 10V, f = 1MHz)	C _{CB0}	—	—	100	pF
Current-Gain — Bandwidth Product (I _C = 20mA, V _{CE} = 4V)	f _T	—	50	—	MHz

SWITCHING CHARACTERISTICS

Resistive Load						
Delay Time + Rise Time	I _C = 1A, I _{B1} = I _{B2} = 0.1A, V _{CC} = 30V, t _p = 25 μsec	t _d + t _r	—	100	—	nS
Storage Time		t _s	—	500	—	
Fall Time		t _f	—	75	—	

(1) Pulse Test PW = 300ms Duty Cycle ≤ 2%.

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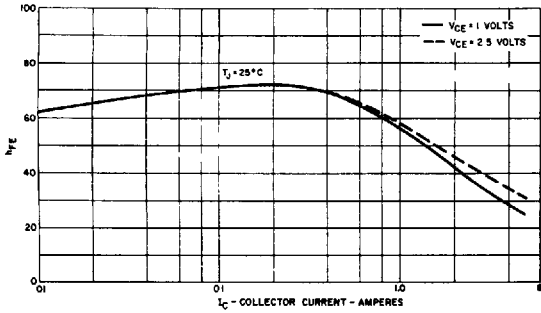


FIG. 1 TYPICAL h_{FE} VS. I_C

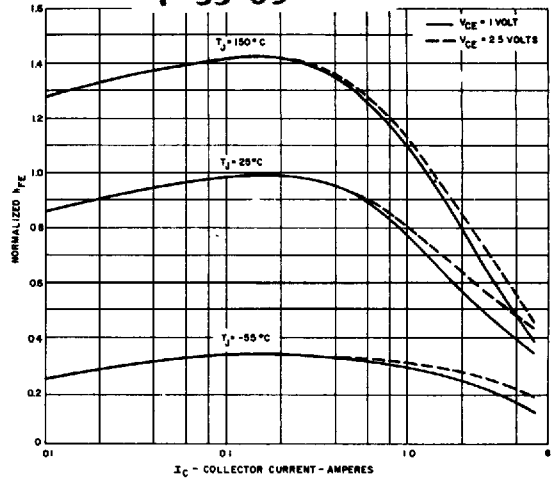


FIG. 2 TYPICAL NORMALIZED h_{FE} VS. I_C

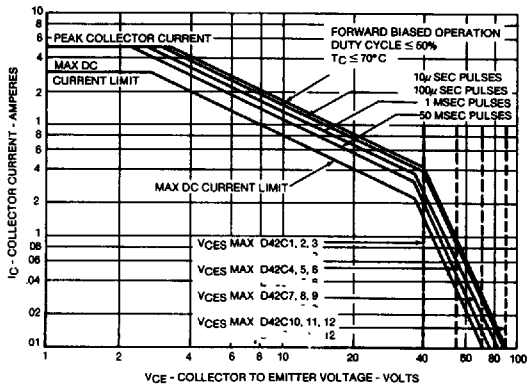


FIG. 3 SAFE REGION OF OPERATION

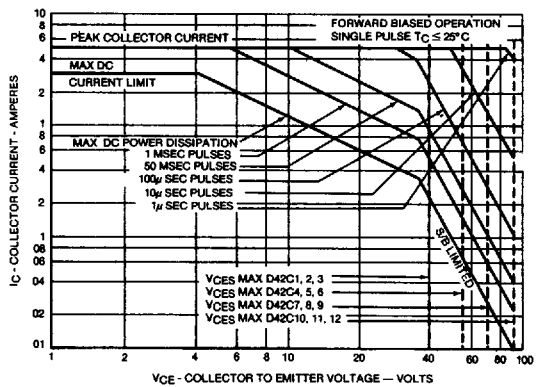


FIG. 4 SAFE REGION OF OPERATION

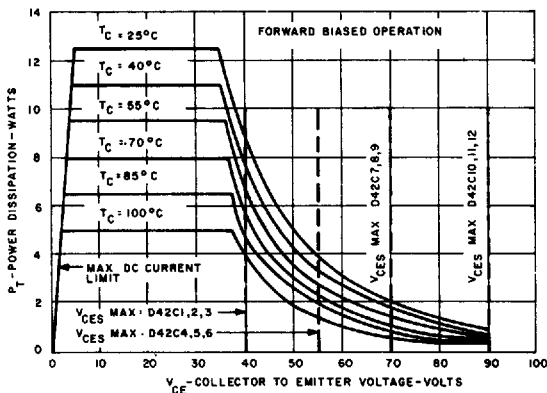


FIG. 5 MAXIMUM PERMISSIBLE DC POWER DISSIPATION

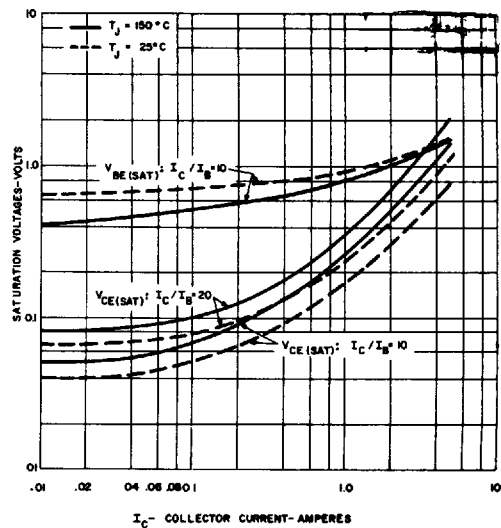


FIG. 6 TYPICAL SATURATION VOLTAGE CHARACTERISTICS

POWER TRANSISTORS

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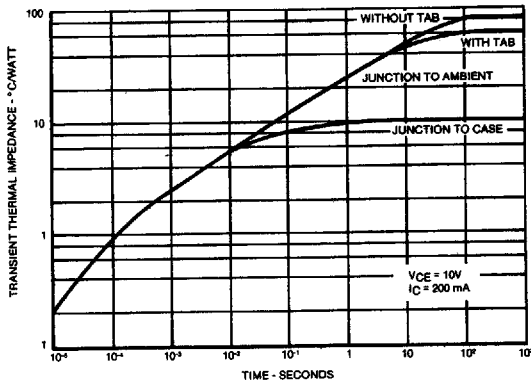


FIG. 7 MAXIMUM TRANSIENT THERMAL IMPEDANCE

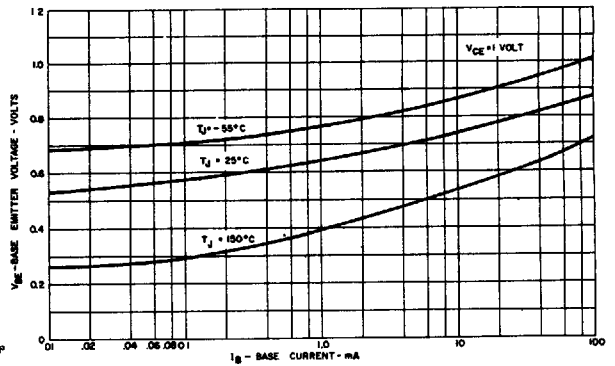


FIG. 8 TYPICAL INPUT CHARACTERISTICS

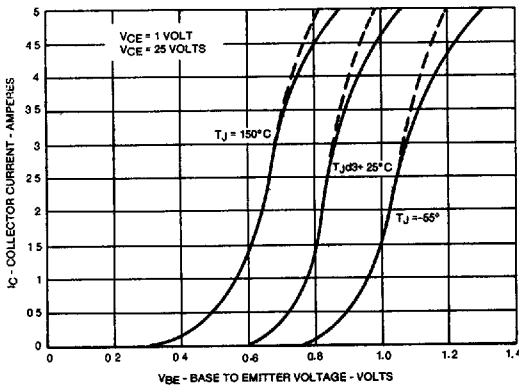


FIG. 9 TYPICAL TRANSCONDUCTANCE CHARACTERISTICS

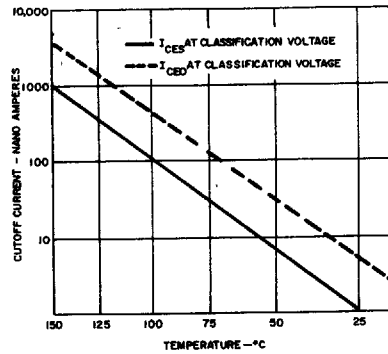


FIG. 10 TYPICAL ICES, ICES VS. TEMPERATURE