TS3USB221A-Q1 ESD Protected, High-Speed USB 2.0 (480 Mbps) 1:2 Multiplexer/Demultiplexer Switch With Single Enable

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- V_{CC} Operation at 2.5 V to 3.3 V
- $V_{I/O}$ Accepts Signals Up to 5.5 V
- 1.8-V Compatible Control-Pin Inputs
- Low-Power Mode When $\overline{OE}$ Is Disabled (1 µA)
- r_{ON} = 16 Ω Maximum
- Δr_{ON} = 0.2 Ω Typical
- $C_{io(on)}$ = 6 pF Typical
- Low Power Consumption (30 µA Maximum)
- High Bandwidth (900 MHz Typical)
- ESD Performance Tested Per JESD 22
  - 7000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance I/O to GND Per JESD 22
  - 12-kV Human-Body Model

2 Applications

- Routing High Speed USB Signals
- Automotive USB Hubs
- Phone-Controlled Automotive Infotainment

3 Description

The TS3USB221A-Q1 is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in automotive USB hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221A-Q1 integrates ESD protection cells on all pins, is available in a tiny UQFN package (2 mm × 1.5 mm) and is characterized over the free air temperature range from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USB221A-Q1	UQFN (10)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

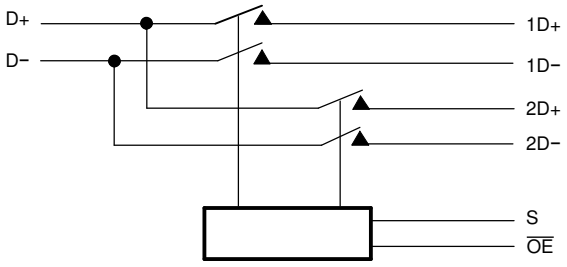


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2016) to Revision E — **Page**

- Changed CDM spec to align with AEC Q100-011 ... 4

Changes from Revision C (October 2012) to Revision D — **Page**

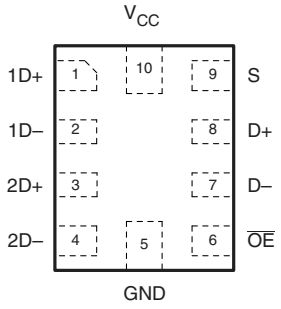
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted the *Ordering Information* table; see the *POA* at the end of the data sheet ... 1
- Updated *Applications* section ... 1
- Changed "in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os" to "in automotive USB hubs or controllers with limited USB I/Os" in *Description* section 1
- Changed the $R_{\theta JA}$ and $R_{\theta JC(top)}$ values in the *Thermal Information* table, and added more thermal values ... 4

Changes from Revision B (July 2011) to Revision C — **Page**

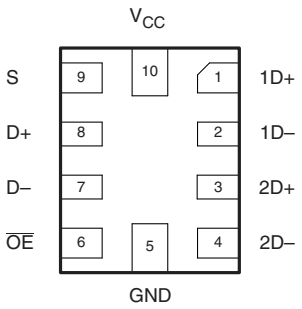
- Added AEC-Q100 info to Features. ... 1
- Added "Per JESD 22" to ESD Performance I/O to GND in Features. ... 1
- Added ESD ratings to Abs Max table. ... 4

5 Pin Configuration and Functions

RSE Package
10-Pin UQFN
Top View



RSE Package
10-Pin UQFN
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1D+	I/O	USB port 1
2	1D–	I/O	
3	2D+	I/O	USB port 2
4	2D–	I/O	
5	GND	—	Ground
6	$\overline{OE}$	I	Bus-switch enable
8	D+	I/O	Common USB port
7	D–	I/O	
9	S	I	Select input
10	V_{CC}	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
$I_{I/O}$	ON-state switch current(5)			±120	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 Classification Level H2[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Classification C5	±750 for corner pins ±500 for all other pins	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0.46 × V_{CC}		V
		V_{CC} = 2.7 V to 3.6 V	0.46 × V_{CC}		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.25 × V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V		0.25 × V_{CC}	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TS3USB221A-Q1 RSE (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}	Input-source clamp voltage	V_{CC} = 3.6 V, 2.7 V, I_I = –18 mA					–1.8	V
I_{IN}	Input leakage current, control inputs	V_{CC} = 3.6 V, 2.7 V, 0 V, V_{IN} = 0 V to 3.6 V					±1	µA
I_{OZ} (3)	Off-state leakage current	V_{CC} = 3.6 V, 2.7 V, V_O = 0 V to 5.25 V, V_I = 0 V, V_{IN} = V_{CC} or GND, Switch OFF					±1	µA
$I_{(OFF)}$	Power-off leakage current	V_{CC} = 0 V	$V_{I/O}$ = 0 V to 5.25 V				±2	µA
			$V_{I/O}$ = 0 V to 3.6 V				±2	
			$V_{I/O}$ = 0 V to 2.7 V				±1	
I_{CC}	Supply current	V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND, $I_{I/O}$ = 0 V, Switch ON or OFF					30	µA
I_{CC}	Supply current (low power mode)	V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND, Switch disabled, $\overline{OE}$ in high state					1	µA
ΔI_{CC} (4)	Supply-current change, control inputs	One input at 1.8 V, Other inputs at V_{CC} or GND	V_{CC} = 3.6 V				20	µA
			V_{CC} = 2.7 V				0.5	
C_{in}	Input capacitance, control inputs	V_{CC} = 3.3 V, 2.5 V, V_{IN} = V_{CC} or 0 V				1.5	2.5	pF
$C_{io(OFF)}$	OFF capacitance	V_{CC} = 3.3 V, 2.5 V, $V_{I/O}$ = V_{CC} or 0 V, Switch OFF				3.5	5	pF
$C_{io(ON)}$	ON capacitance	V_{CC} = 3.3 V, 2.5 V, $V_{I/O}$ = V_{CC} or 0 V, Switch ON				6	7.5	pF
R_{ON} (5)	ON-state resistance	V_{CC} = 3 V, 2.3 V	V_I = 0 V, I_O = 30 mA	T_A = 25°C		3	6	Ω
			V_I = 2.4 V, I_O = –15 mA			3.4	6	
			V_I = 0 V, I_O = 30 mA	T_A = 125°C		6	10	
			V_I = 2.4 V, I_O = –15 mA			10	16	
ΔR_{ON}	ON-state resistance match between channels	V_{CC} = 3 V, 2.3 V	V_I = 0 V, I_O = 30 mA			0.2		Ω
			V_I = 1.7, I_O = –15 mA			0.2		
$r_{ON(flat)}$	ON-state resistance flatness	V_{CC} = 3 V, 2.3 V	V_I = 0 V, I_O = 30 mA			1		Ω
			V_I = 1.7, I_O = –15 mA			1		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Dynamic Electrical Characteristics: V_{CC} = 3.3 V

over operating range, T_A = –40°C to 125°C, V_{CC} = 3.3 V ±10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250 MHz	–40	dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250 MHz	–41	dB
BW	Bandwidth (–3 dB)	R_L = 50	0.9	GHz

6.7 Dynamic Electrical Characteristics: V_{CC} = 2.5 V

over operating range, T_A = –40°C to 125°C, V_{CC} = 2.5 V ±10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250 MHz	–39	dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250 MHz	–40	dB
BW	Bandwidth (3 dB)	R_L = 50	0.9	GHz

6.8 Switching Characteristics: V_{CC} = 3.3 V

over operating range, T_A = –40°C to 125°C, V_{CC} = 3.3 V ±10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			30	ns
		$\overline{OE}$ to D, nD			17	
t_{OFF}	Line disable time	S to D, nD			12	ns
		$\overline{OE}$ to D, nD			10	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under *Dynamic Electrical Characteristics: V_{CC} = 3.3 V* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.9 Switching Characteristics: V_{CC} = 2.5 V

over operating range, T_A = –40°C to 125°C, V_{CC} = 2.5 V ±10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			50	ns
		$\overline{OE}$ to D, nD			32	
t_{OFF}	Line disable time	S to D, nD			23	ns
		$\overline{OE}$ to D, nD			12	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under *Dynamic Electrical Characteristics: V_{CC} = 2.5 V* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.10 Typical Characteristics

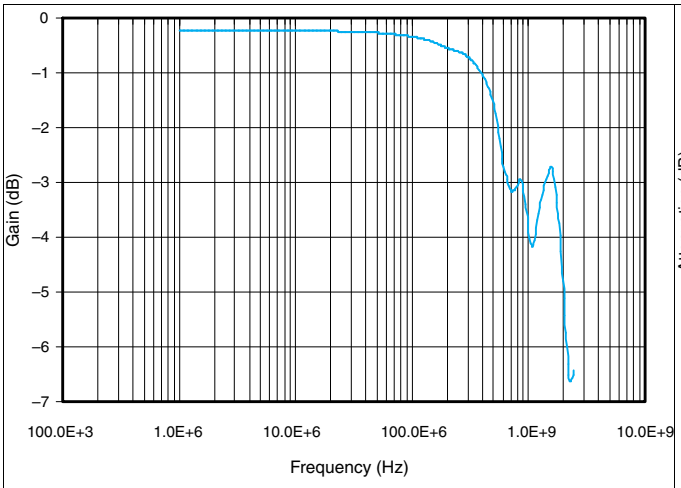


Figure 1. Gain vs Frequency

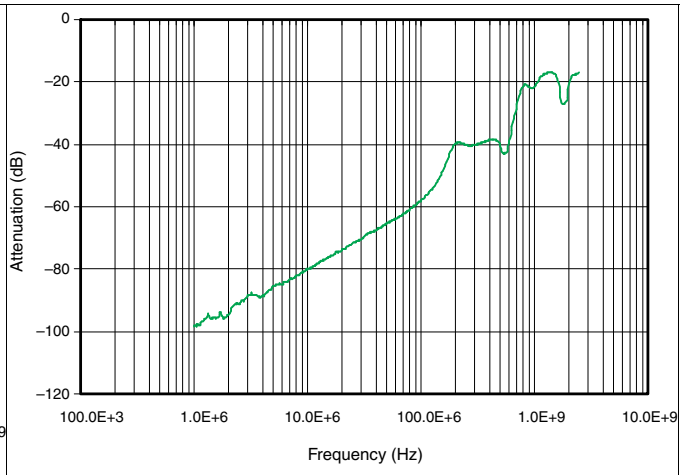


Figure 2. OFF Isolation vs Frequency

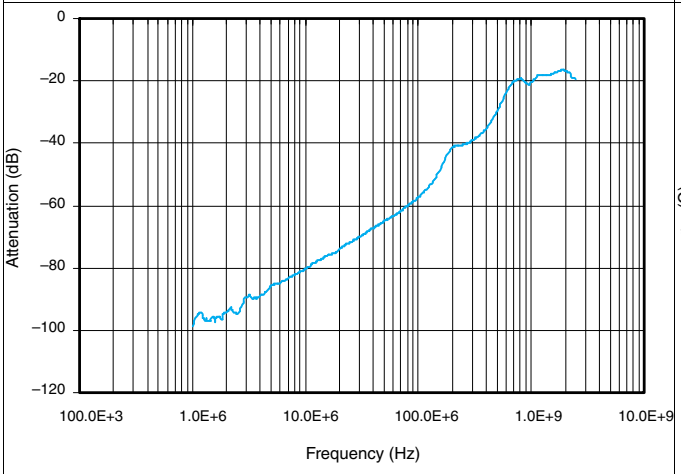


Figure 3. Crosstalk vs Frequency

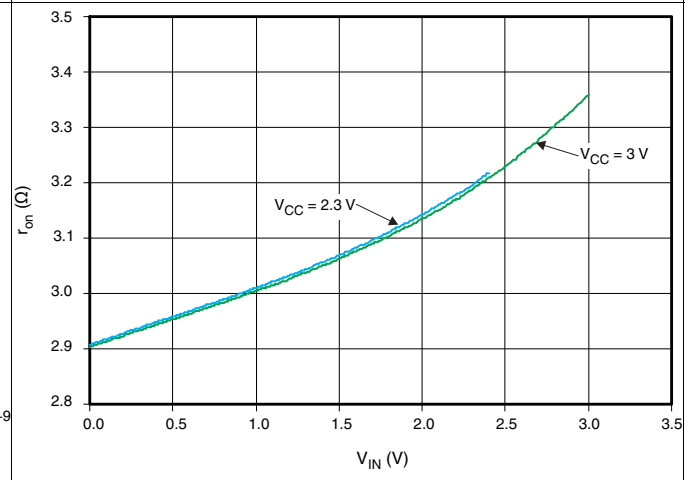


Figure 4. r_{on} vs V_{IN} (I_{OUT} = –15 mA)

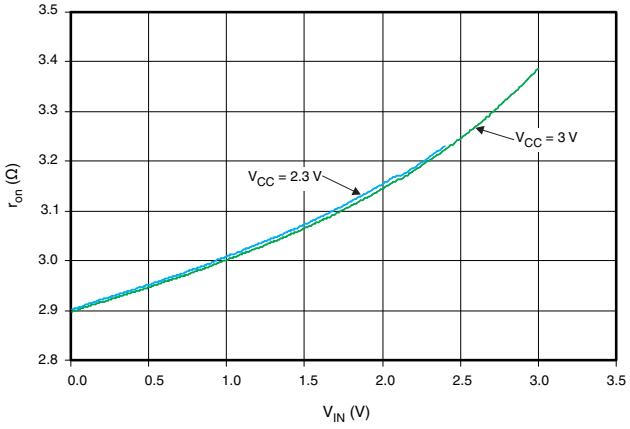
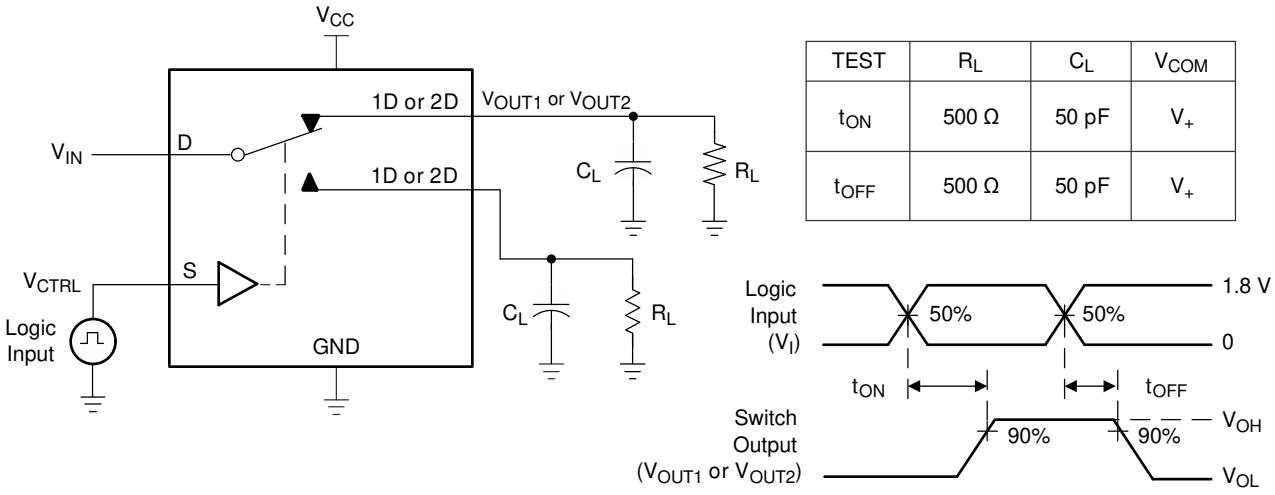


Figure 5. r_{ON} vs V_{IN} (I_{OUT} = 30 mA)

7 Parameter Measurement Information



TEST	R_L	C_L	V_{COM}
t_{ON}	500 Ω	50 pF	V_+
t_{OFF}	500 Ω	50 pF	V_+

Figure 6. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

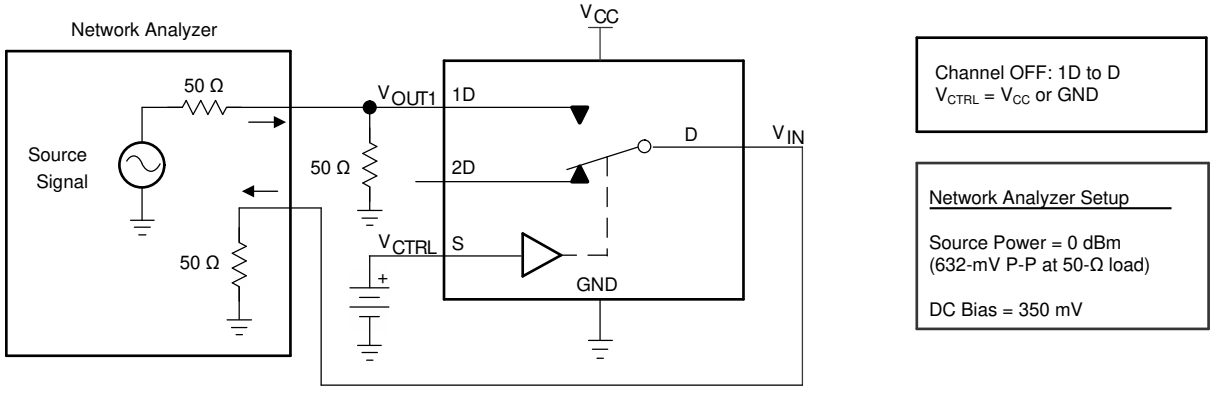


Figure 7. OFF Isolation (O_{ISO})

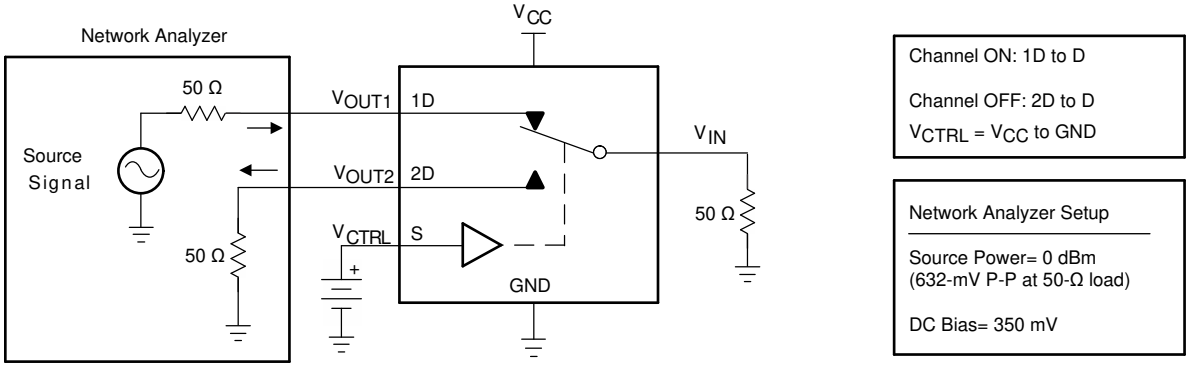


Figure 8. Crosstalk (X_{TALK})

Parameter Measurement Information (continued)

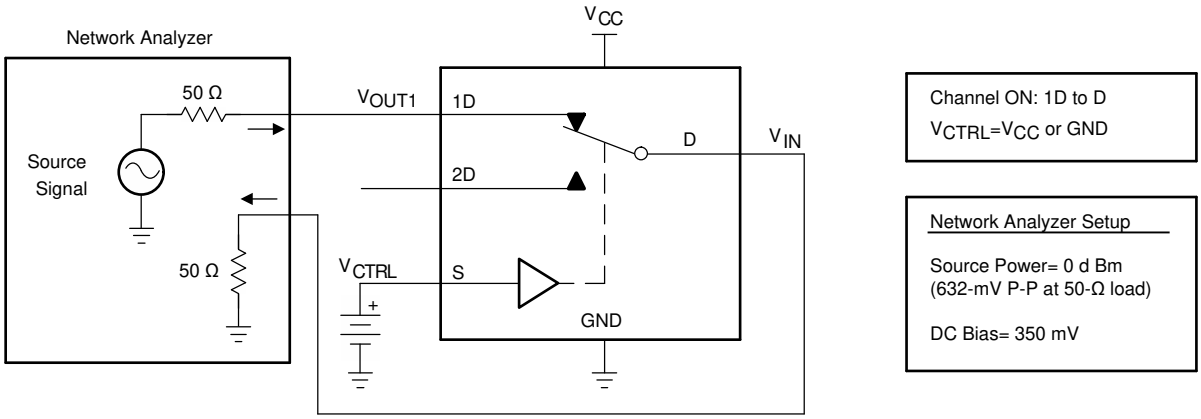


Figure 9. Bandwidth (BW)

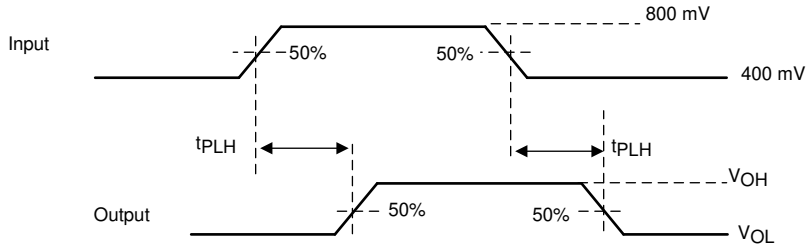


Figure 10. Propagation Delay

Parameter Measurement Information (continued)

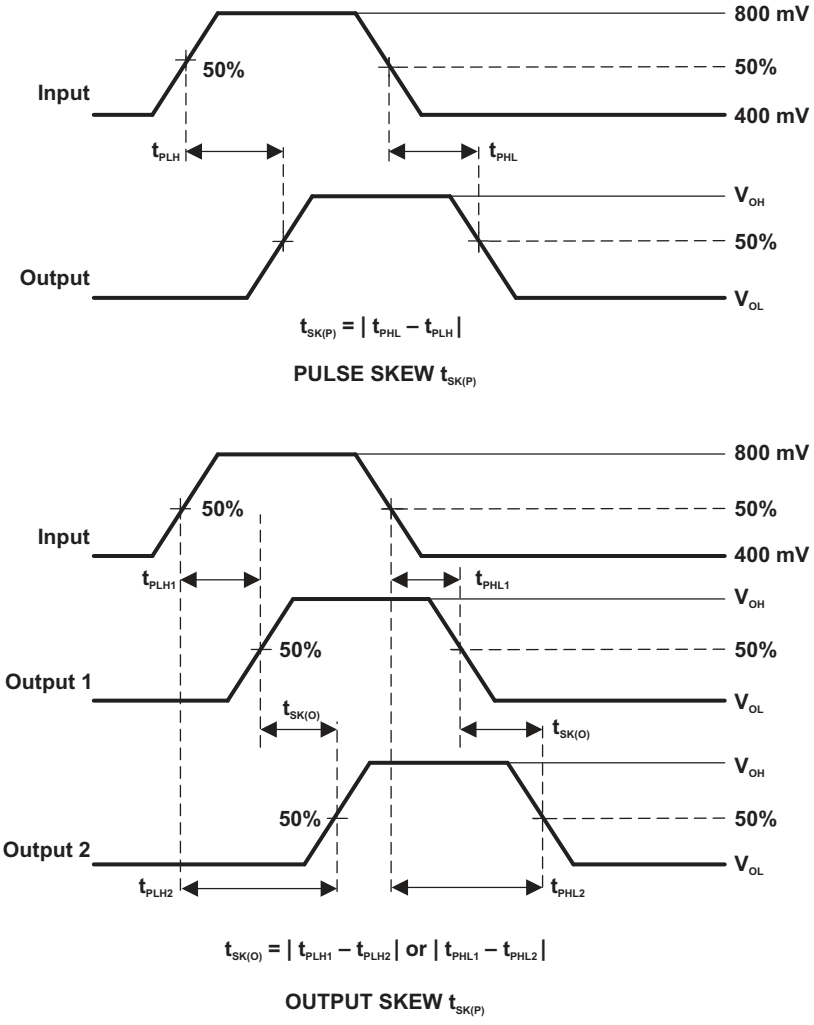


Figure 11. Skew Test

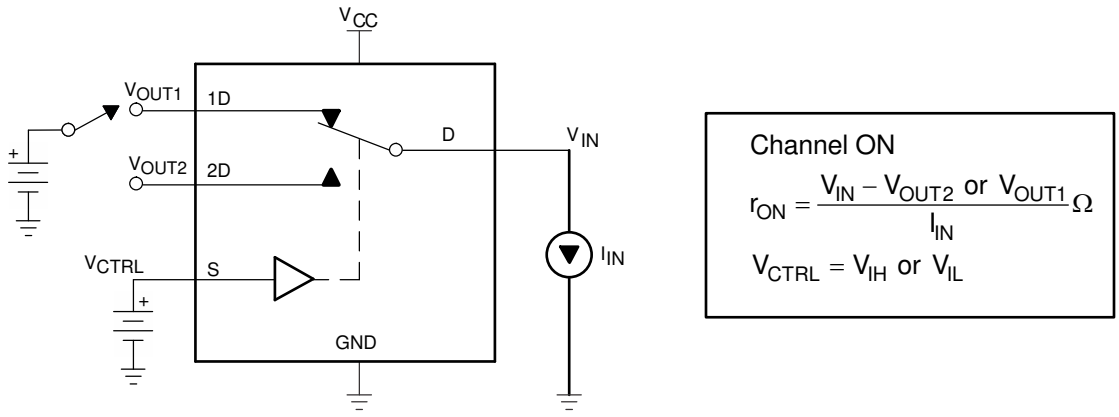


Figure 12. ON-State Resistance (r_{on})

Parameter Measurement Information (continued)

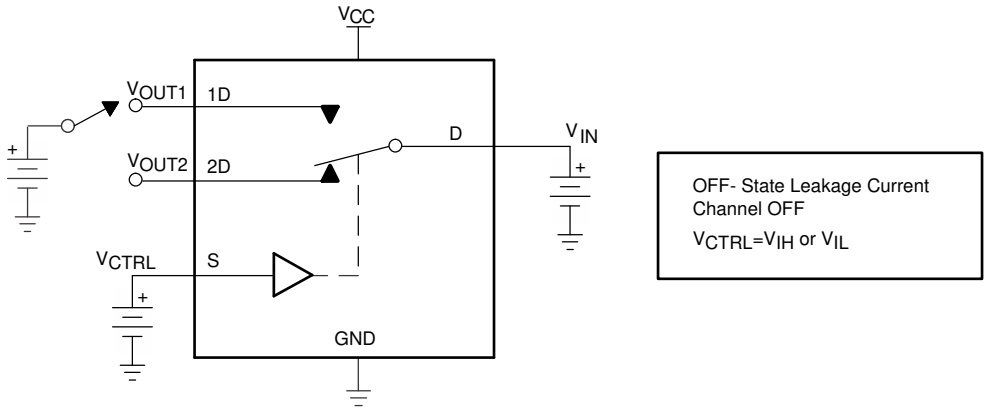


Figure 13. OFF-State Leakage Current

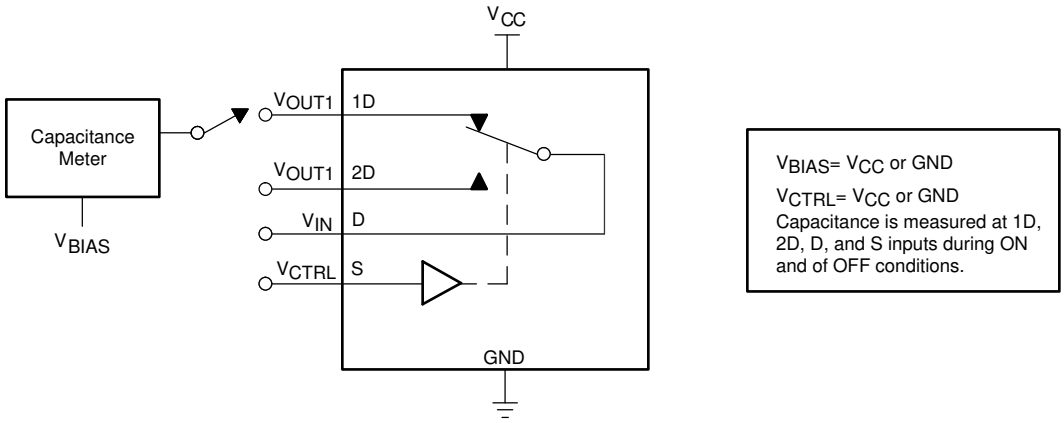


Figure 14. Capacitance

8 Detailed Description

8.1 Overview

The TS3USB221A-Q1 device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in automotive applications, such as USB hubs. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that will reduce the power consumption to 1 µA for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221A-Q1 device integrates ESD protection cells on all pins, is available in a tiny UQFN package (2 mm × 1.5 mm) and is characterized over the free air temperature range from –40°C to 125°C.

8.2 Functional Block Diagram

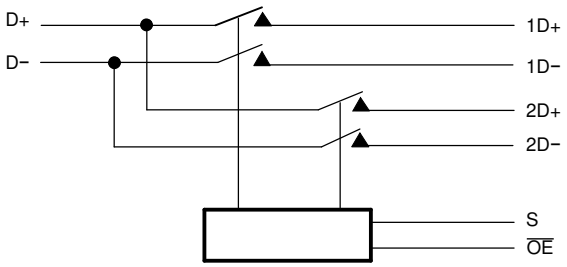
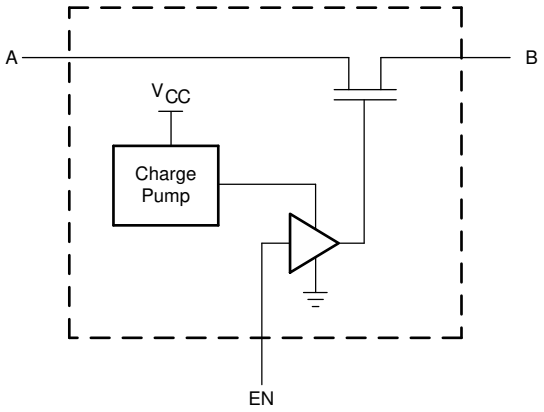


Figure 15. Block Diagram



EN is the internal enable signal applied to the switch.

Figure 16. Simplified Schematic of Each FET Switch (SW)

8.3 Feature Description

8.3.1 Low Power Mode

The TS3USB221A-Q1 has a low power mode that reduces the power consumption to 1 µA while the devices is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{OE}$ must be supplied with a logic High signal.

8.4 Device Functional Modes

Table 1 lists the functions of this device.

Table 1. Truth Table

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221A-Q1 solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller.

9.2 Typical Application

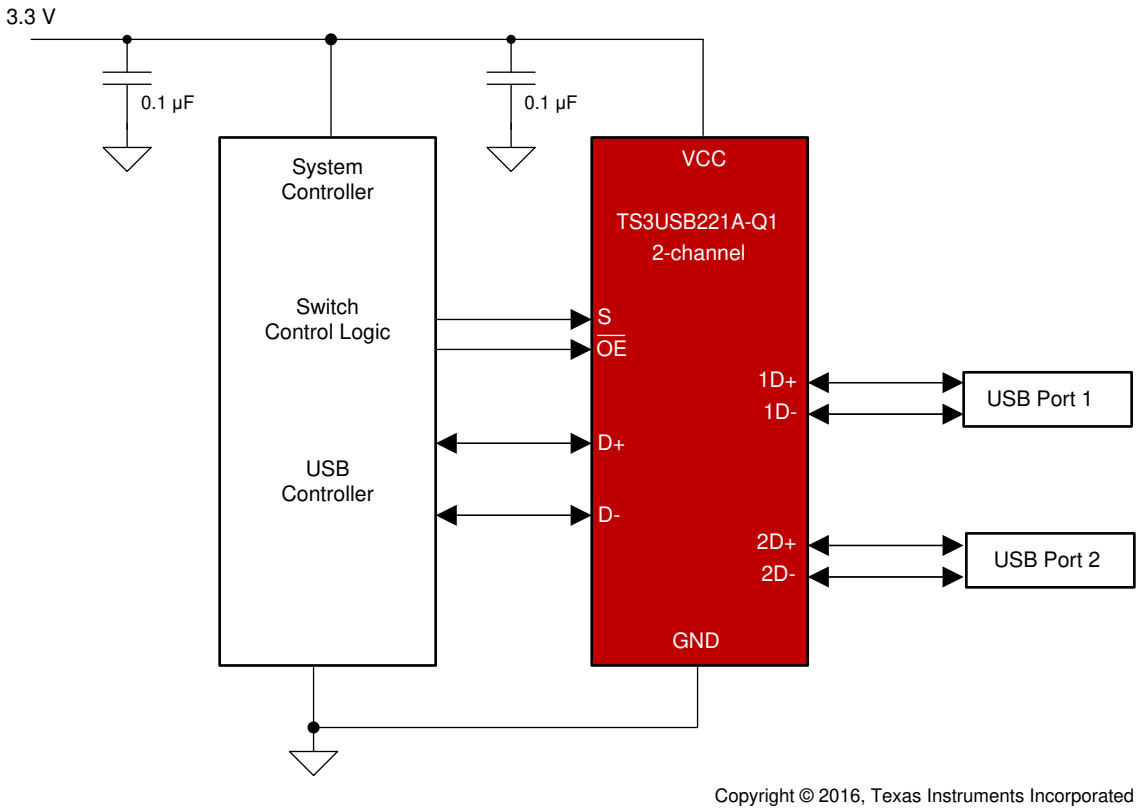


Figure 17. Application Schematic

9.2.1 Design Requirements

Design requirements of the USB 1.0,1.1, and 2.0 standards should be followed.

TI recommends pulling the digital control pins S and $\overline{OE}$ up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

The TS3USB221A-Q1 can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device.

Typical Application (continued)

9.2.3 Application Curves

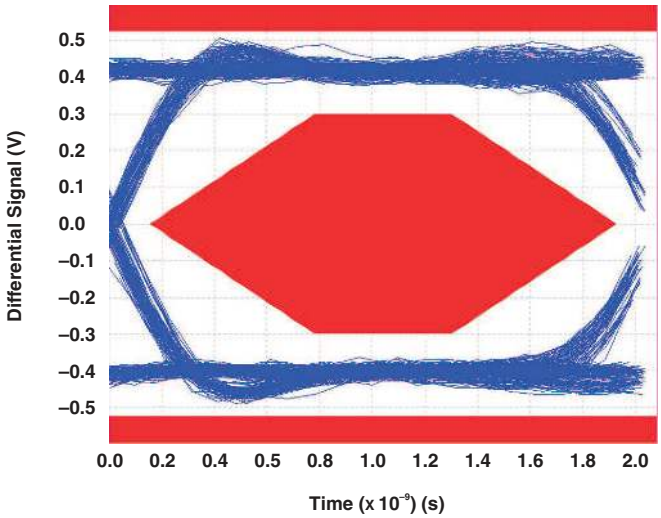


Figure 18. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

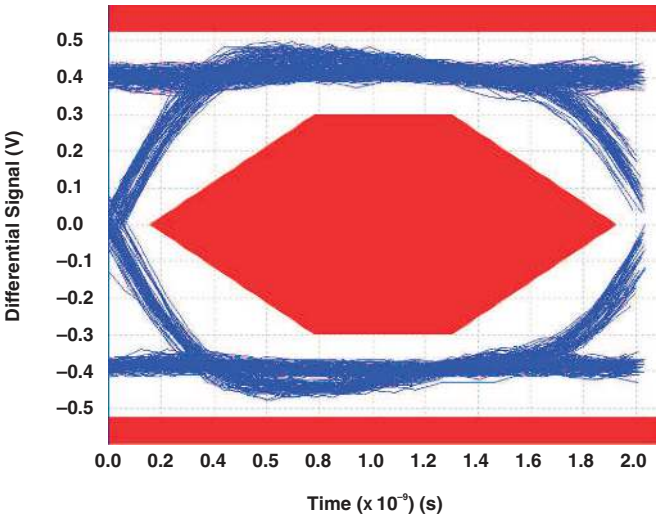


Figure 19. Eye Pattern: 480-Mbps USB Signal With Switch NC Path

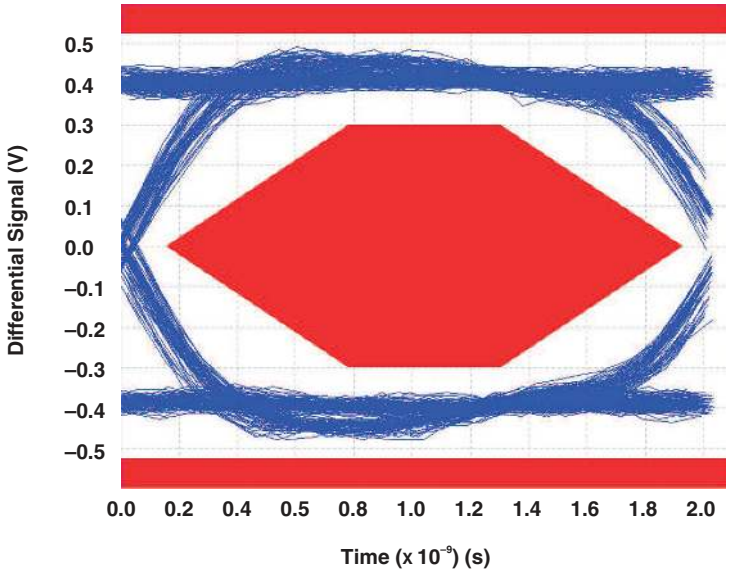


Figure 20. Eye Pattern: 480-Mbps USB Signal With Switch NO Path

10 Power Supply Recommendations

Power to the device is supplied through the VCC pin and should follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close to the supply pin VCC to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible, and avoid placing the bypass capacitors near the D+/D- traces.

The high speed D+/D- traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D- traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, TI recommends a printed-circuit board with at least four layers; two signal layers separated by a ground and power layer as shown in Figure 21.

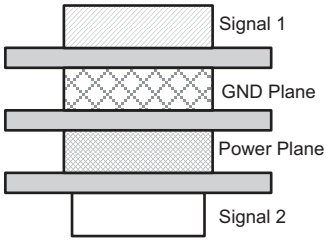


Figure 21. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

11.2 Layout Example

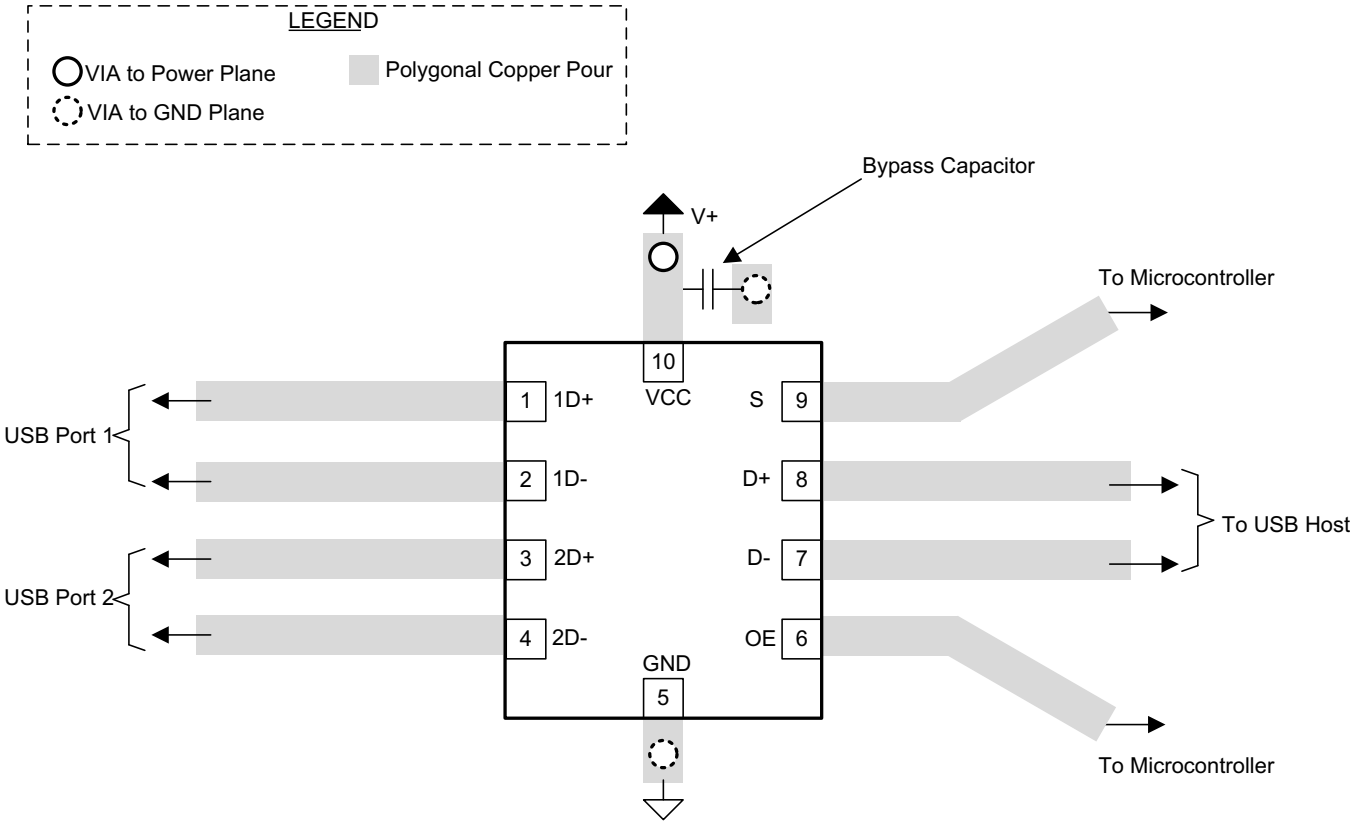


Figure 22. Package Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resource

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB221AQRSERQ1	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	OFW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

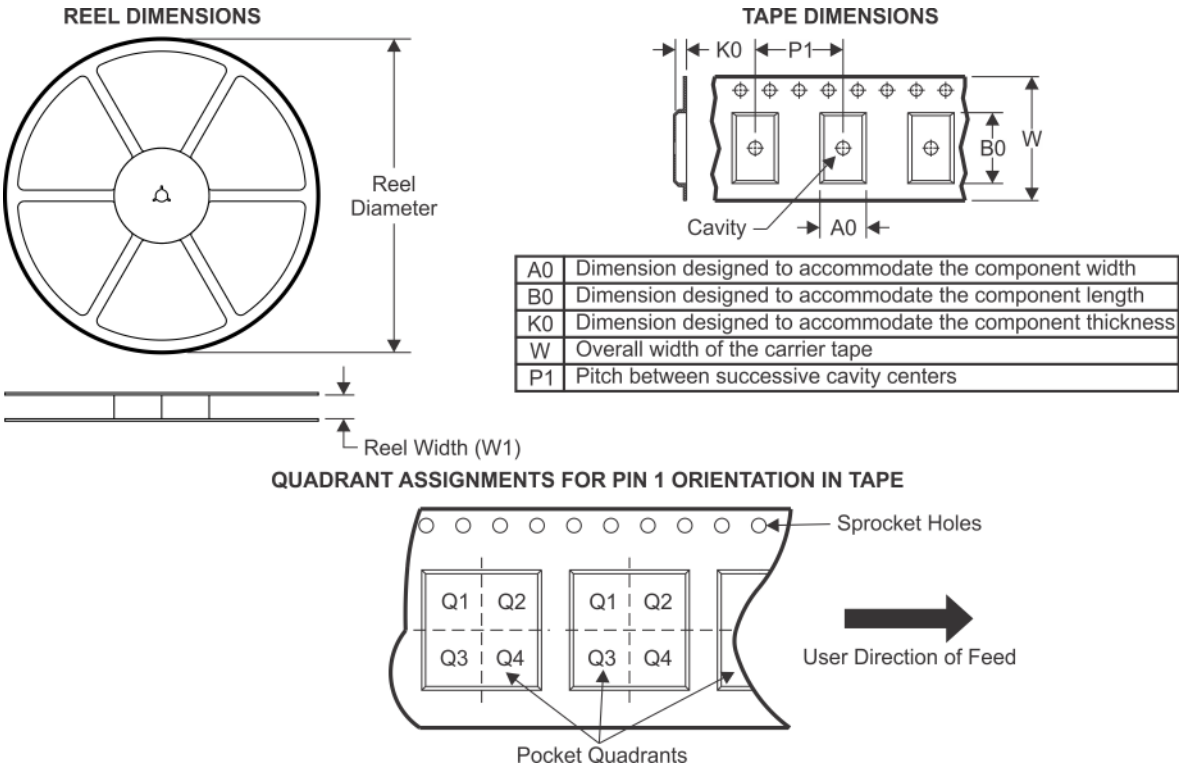
OTHER QUALIFIED VERSIONS OF TS3USB221A-Q1 :

- Catalog: TS3USB221A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

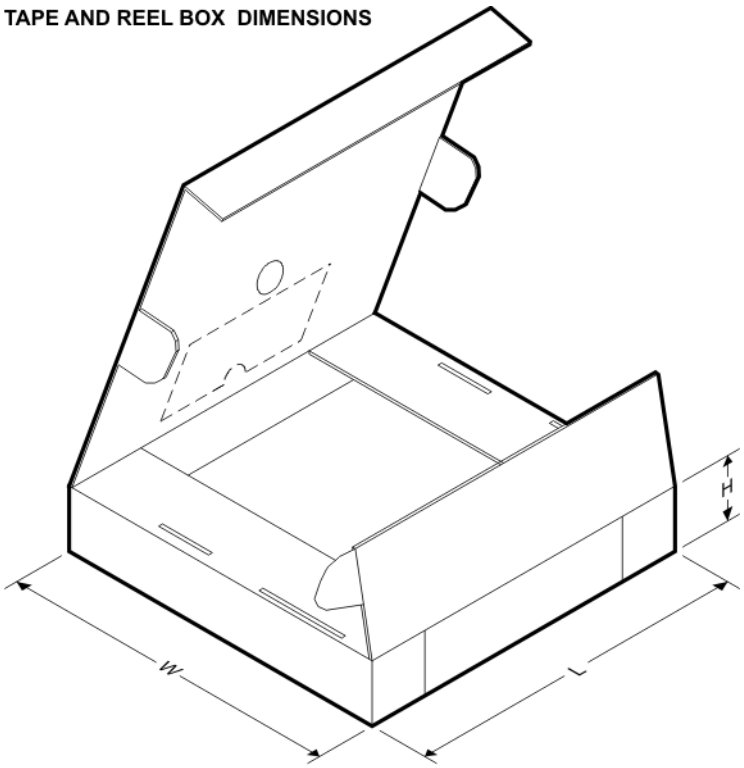


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB221AQRSERQ1	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

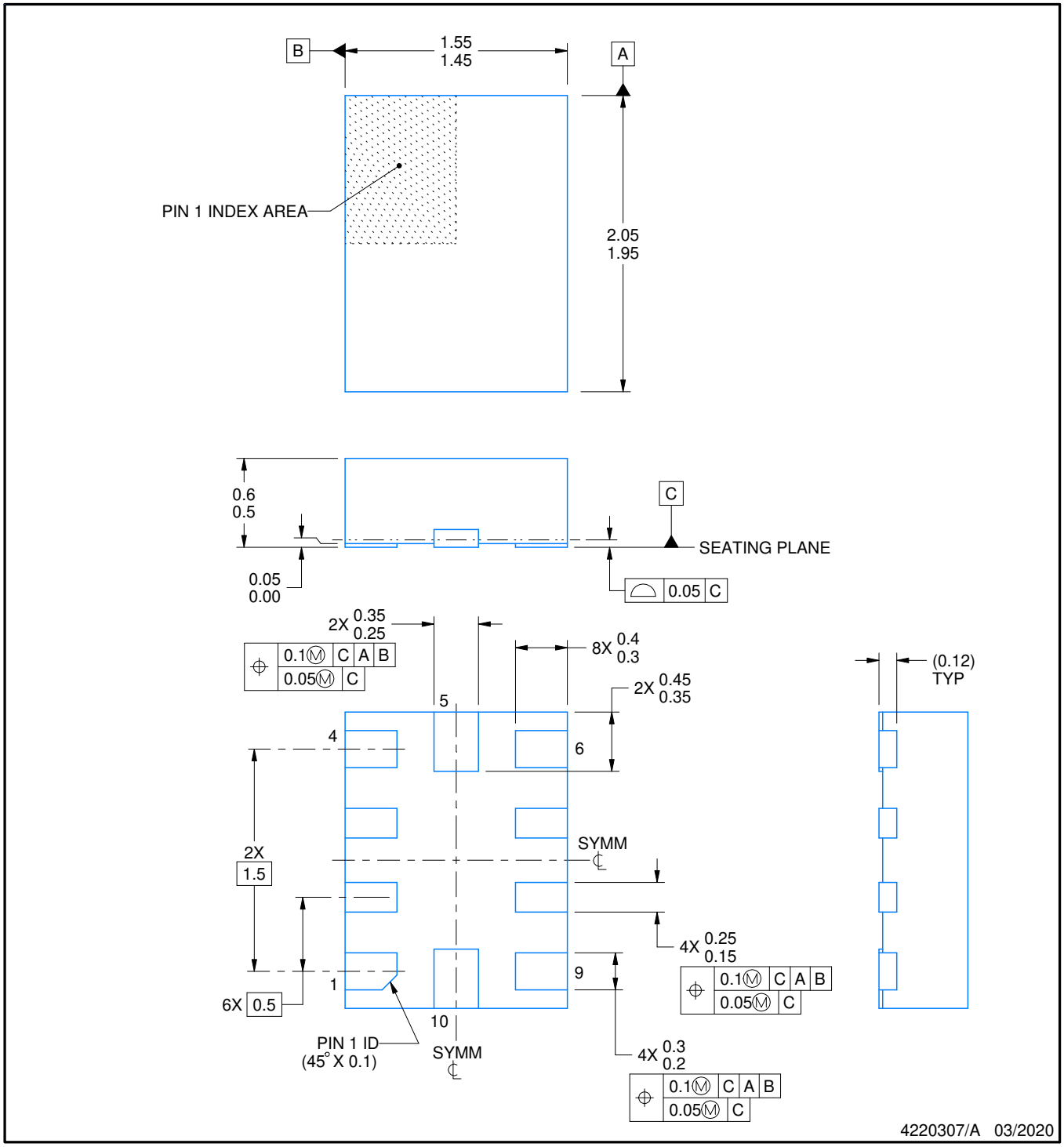
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB221AQRSERQ1	UQFN	RSE	10	3000	223.0	270.0	35.0

PACKAGE OUTLINE

RSE0010A

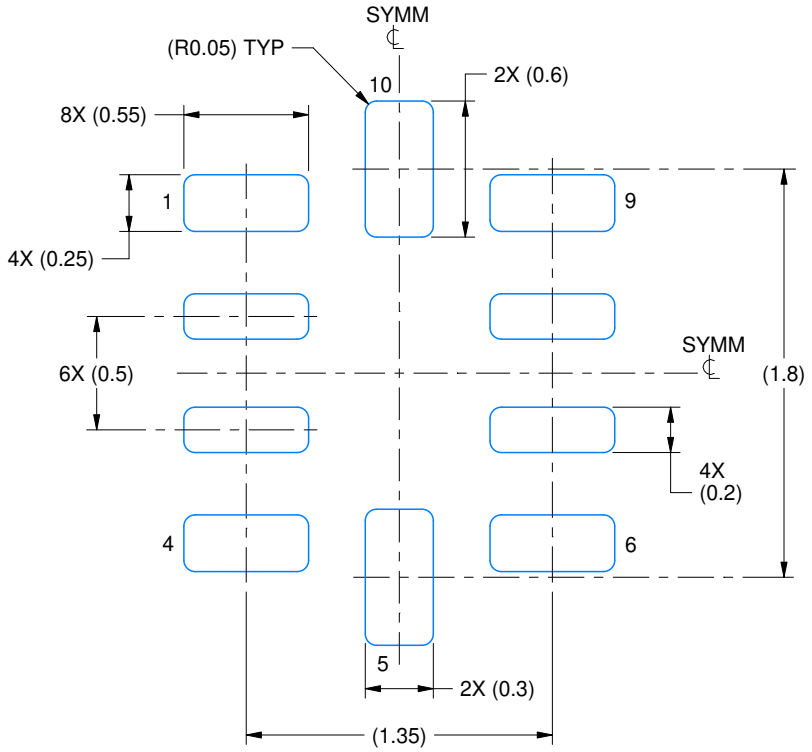
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

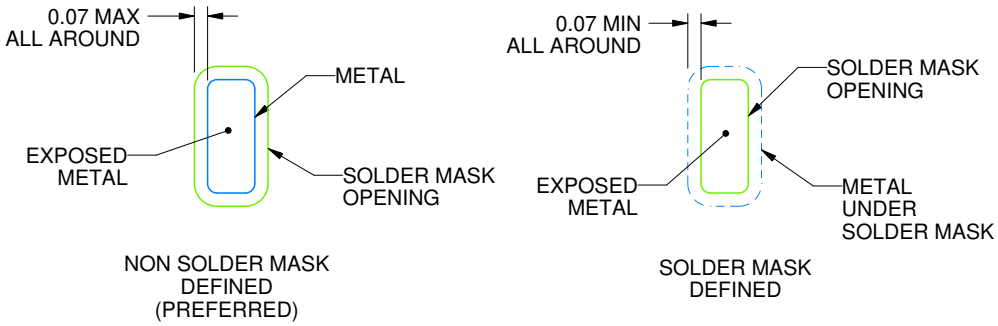


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

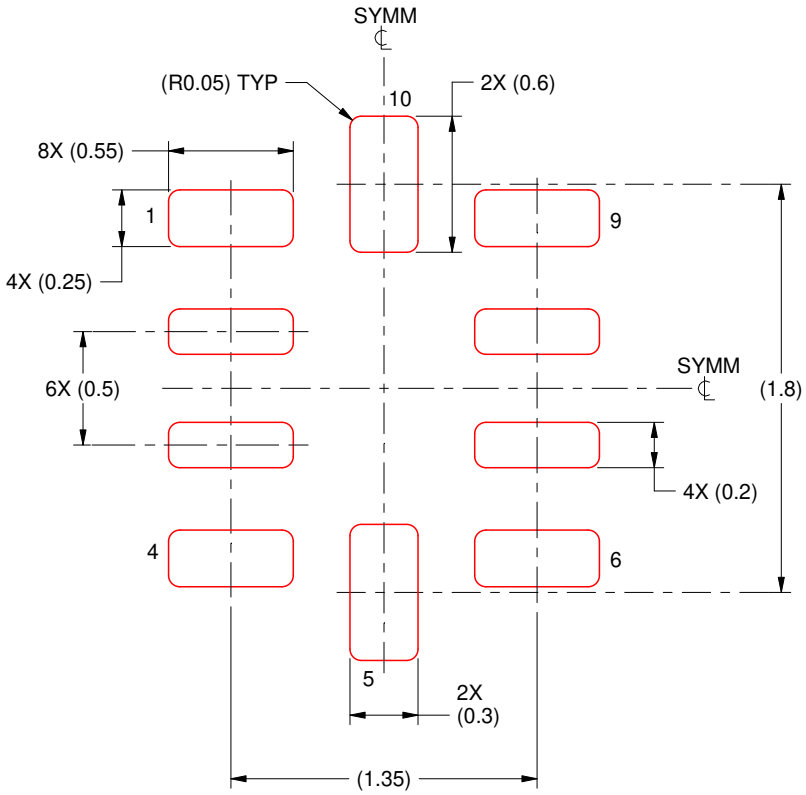


SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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