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5.5V Input, 2A, High-Efficiency Buck-Boost Converter

MAX77801

General Description

The MAX77801 is a high-efficiency, step-up/step-down (buck-boost) converter targeted for single-cell, Li-ion battery-powered applications. The device maintains a regulated output voltage from 2.6V to 4.18V across an input voltage range of 2.3V to 5.5V. The device supports up to 2A of output current in boost mode and up to 3A in buck mode.

The device seamlessly transitions between buck and boost modes. A unique control algorithm allows high-efficiency and outstanding load and line-transient response.

Dedicated enable and power-OK pins allow simple hardware control. An I²C serial interface is optionally used for dynamic voltage scaling, system power optimization, and fault read-back.

The MAX77801 is available in a 20-bump, 2.13mm x 1.83mm wafer-level package (WLP) and also 20-pin, 4mm x 4mm TQFN.

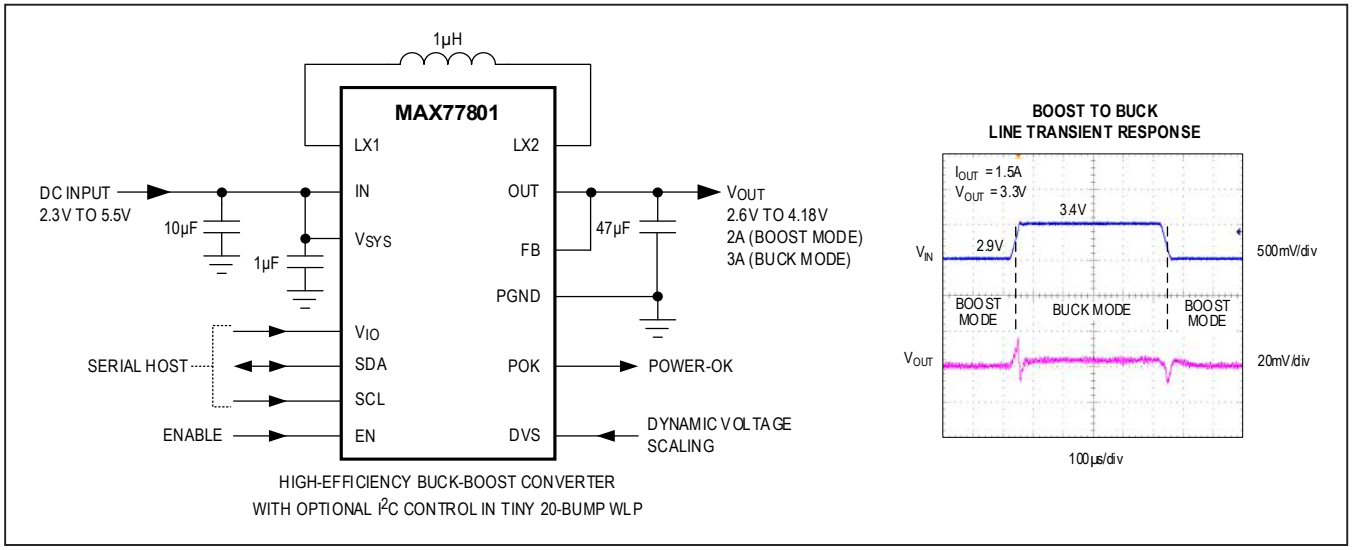
Applications

- Single-Cell, Li-Ion Battery-Powered Devices
- Handheld Scanners, Mobile Payment Terminals, Security Cameras
- AR/VR Headsets

Benefits and Features

- V_{IN} Range: 2.30V to 5.5V
- V_{OUT} Range: 2.60V to 4.18V (I²C Programmable in 12.5mV Steps)
- Up to 2A Output Current in Boost Mode (V_{IN} = 3.0V, V_{OUT} = 3.4V)
- Up to 3A Output Current in Buck Mode
- Up to 97% Peak Efficiency
- SKIP Mode for Optimal Light Load Efficiency
- 55µA (Typ) Low Quiescent Current
- 3.4MHz High-Speed I²C Serial Interface
- Dynamic Voltage Scaling (DVS) Function
- Power-OK Output
- 2.5MHz Switching Frequency
- Protection Features
  - Soft-Start
  - Thermal Shutdown
  - Overvoltage Protection
  - Overcurrent Protection
- 2.13mm x 1.83mm, 20-Bump WLP
- 4mm x 4mm, 20-Pin TQFN

Typical Application Circuit



Ordering Information ***appears at end of data sheet.***

19-7515; Rev 8; 6/23

Absolute Maximum Ratings

SYS, V_{IO} to AGND ..... -0.3V to +6.0V
IN, OUT to PGND ..... -0.3V to +6.0V
PGND to AGND ..... -0.3V to +0.3V
SCL, SDA to AGND ..... -0.3V to (V_{IO} + 0.3V)
EN, DVS, POK to AGND ..... -0.3V to (V_{SYS} + 0.3V)
FB to AGND ..... -0.3V to (V_{OUT} + 0.3V)
LX1 to PGND ..... -0.3V to (V_{IN} + 0.3V)
LX2 to PGND ..... -0.3V to (V_{OUT} + 0.3V)
LX1/LX2 Continuous RMS Current 3.3A
Operating Junction Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA})
20-Bump WLP ..... 55.49°C/W
20-Pin TQFN ..... 39°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Buck-Boost Electrical Characteristics

(V_{SYS} = V_{IN} = +3.8V, V_{FB} = V_{OUT} = +3.3V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{IN}		2.3		5.5	V
Shutdown Supply Current	I_{SHDN_25C}	EN = low, T_A = +25°C		0.1		µA
	I_{SHDN_125C}	EN = low, T_A = +125°C		1		
Input Supply Current	I_{Q_SKIP}	SKIP mode, no switching T_J = -40°C to +85°C		55	70	µA
	I_{Q_PWM}	FPWM mode, no load		6		mA
Active Discharge Resistance	R_{DISCHG}			100		Ω
Thermal Shutdown	T_{SHDN}	Rising, 20°C hysteresis		+165		°C
H-BRIDGE						
Output Voltage Range	V_{OUT}	I^2C programmable (12.5mV step)	2.60		4.1875	V
Default Output Voltage		VOUT_DVS_L[6:0] = 0x38		3.3		V
		VOUT_DVS_H[6:0] = 0x40, MAX77801EWP only		3.4		
		VOUT_DVS_H[6:0] = 0x5C, MAX77801ETP only		3.75		
Output Voltage Accuracy	V_{OUT_ACC1}	PWM mode, VOUT_DVS_x[6:0] = 0x40, no load T_J = +25°C	-1.0		+1.0	%
	V_{OUT_ACC2}	SKIP mode, VOUT_DVS_x[6:0] = 0x40, no load, T_J = +25°C	-1.0		+4.5	

Buck-Boost Electrical Characteristics (continued)

(V_{SYS} = V_{IN} = +3.8V, V_{FB} = V_{OUT} = +3.3V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Line Regulation		V_{IN} = 2.3V to 5.5V		0.200		%/V
Load Regulation		(Note 3)		0.125		%/A
Line Transient Response	V_{OS1} V_{US1}	I_{OUT} = 1.5A, V_{IN} changes from 3.4V to 2.9V in 25µs (20mV/µs), L = 1µH, C_{OUT_NOM} = 47µF (Note 3)		50		mV
Load Transient Response	V_{OS2} V_{US2}	V_{IN} = 3.4V, I_{OUT} changes from 10mA to 1.5A in 15µs, L = 1µH, C_{OUT_NOM} = 47µF (Note 3)		50		mV
Output Voltage Ramp-Up Slew Rate		RU_SR = 0		12.5		mV/µs
		RU_SR = 1		25		
Output Voltage Ramp-down Slew Rate		RD_SR = 0		3.125		mV/µs
		RD_SR = 1		6.25		
Typical Load Efficiency	η_{IOUT_TYP}	I_{OUT} = 100mA, V_{IN} = 3.6V (Note 3)		95		%
Peak Efficiency	η_{PK}	(Note 3)		97		%
Maximum Output Current	$I_{OUT(MAX)}$	2.8V ≤ V_{IN} ≤ 5.5V	2000			mA
	$I_{OUT(MAX)}$	2.3V ≤ V_{IN} < 2.8V	1000			
LX1/2 Current Limit	I_{LIM_LX}		3.70	4.70	5.70	A
High-Side PMOS ON Resistance	R_{DSON} (PMOS)	I_{LX} = 100mA per switch, WLP		40		mΩ
		I_{LX} = 100mA per switch, TQFN		50		
Low-Side NMOS ON Resistance	R_{DSON} (NMOS)	I_{LX} = 100mA per switch, WLP		55		mΩ
		I_{LX} = 100mA per switch, TQFN		65		
Switching Frequency	f_{SW}	PWM mode, T_A = +25°C	2.25	2.50	2.75	MHz
Turn-On Delay Time	t_{ON_DLY}	From EN asserting to LX switching with bias ON		100		µs
Soft-Start Time (Reduce I_{LIM_LX})	$t_{SS\_LOW\_ILIM}$	I_{OUT} = 10mA		120		µs
Soft-Start Time (Ramp V_{REF})	$t_{SS\_RAMP\_VREF}$	MAX77801HEWP+T, V_{OUT} from 10% to 90% of target, I_{OUT} = 0mA, C_{OUT} = 47µF, V_{IN} = 2.7V to 4.5V, T_A = 0°C to 40°C (Note 3)		300		µs
Minimum Soft-Start Time (Ramp V_{REF})		MAX77801HEWP+T, V_{OUT} from 10% to 90% of target, I_{OUT} = 0mA, C_{OUT} = 47µF, V_{IN} = 2.7V to 4.5V, T_A = 0°C to 40°C (Note 3)		150		µs
Maximum Soft-Start Time (Ramp V_{REF})		MAX77801HEWP+T, V_{OUT} from 10% to 90% of target, I_{OUT} = 0mA, C_{OUT} = 47µF, V_{IN} = 2.7V to 4.5V, T_A = 0°C to 40°C (Note 3)		450		µs

Buck-Boost Electrical Characteristics (continued)

(V_{SYS} = V_{IN} = +3.8V, V_{FB} = V_{OUT} = +3.3V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Effective Output Capacitance	$C_{EFF(MIN)}$	0A < I_{OUT} < 2000mA		16		µF
LX1, LX2 Leakage Current	I_{LK_25}	$V_{LX1/2}$ = 0V or 5.5V, V_{OUT} = 5.5V, V_{SYS} = V_{IN} = 5.5V, T_A = +25°C		0.1	1	µA
	I_{LK_125}	$V_{LX1/2}$ = 0V or 5.5V, V_{OUT} = 5.5V, V_{SYS} = V_{IN} = 5.5V, T_A = +125°C		0.2		
POWER-OK COMPARATOR						
Output POK Trip Level		Rising threshold		80		%
		Falling threshold		75		%
V_{SYS} UNDERVOLTAGE LOCKOUT						
V_{SYS} Undervoltage Lockout Threshold	V_{UVLO_R}	V_{SYS} rising	2.375	2.50	2.625	V
	V_{UVLO_F}	V_{SYS} falling (default)		2.05		V
LOGIC AND CONTROL INPUTS						
Input Low Level	V_{IL}	EN, DVS, V_{SYS} ≤ 4.5V, T_A = +25°C			0.4	V
Input High Level	V_{IH}	EN, DVS, V_{SYS} ≤ 4.5V, T_A = +25°C	1.2			V
POK Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
POK Output High Leakage	I_{OZH_25C}	T_J = +25°C	-1		+1	µA
	I_{OZH_125C}	T_J = +125°C		0.1		µA
INTERNAL PULLDOWN RESISTANCE						
EN, DVS	R_{PD}	Pulldown resistor to AGND	400	800	1600	kΩ

I²C Electrical Characteristics

(V_{SYS} = 3.8V, V_{IO} = 1.8V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7		3.6	V
SDA AND SCL I/O STAGES						
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Current	I_I	V_{IO} = 3.8V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
SCL, SDA Input Capacitance	C_I			10		pF
Output Fall Time from V_{IO} to 0.3 x V_{IO}	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST MODE PLUS) (Note 3)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		0.26			µs

I²C Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{IO} = 1.8V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
DATA Hold Time	t_{HD_DAT}		0			µs
DATA Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Capacitive Load for Each Bus Line	C_B				550	pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 100pF) (Note 3)						
Clock Frequency	f_{SCL}				3.4	MHz
Set-Up Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup Time	t_{SU_DAT}		10			ns
DATA Hold Time	t_{HD_DAT}			35		ns
SCL Rise Time (Note 3)	t_{RCL}	T_J = +25°C	10		40	ns
Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit	t_{RCL1}	T_J = +25°C	10		80	ns
SCL Fall Time	t_{FCL}	T_J = +25°C	10		40	ns
SDA Rise Time	t_{RDA}	T_J = +25°C			80	ns
SDA Fall Time	t_{FDA}	T_J = +25°C			80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				10		ns

I²C Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{IO} = 1.8V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 400pF) (Note 3)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
DATA Setup Time	t_{SU_DAT}		10			ns
DATA Hold Time	t_{HD_DAT}			75		ns
SCL Rise Time	t_{RCL}	T_J = +25°C	20		80	ns
Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit	t_{RCL1}	T_J = +25°C	20		160	ns
SCL Fall Time	t_{FCL}	T_J = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_J = +25°C			160	ns
SDA Fall Time	t_{FDA}	T_J = +25°C			160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter	t_{SP}			10		ns

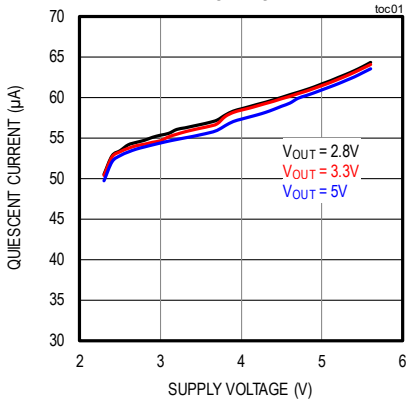
Note 2: Limits are 100% production tested at T_J = +25°C. The device is tested under pulsed load conditions such that $T_J \approx T_A$. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 3: Guaranteed by design. Not production tested.

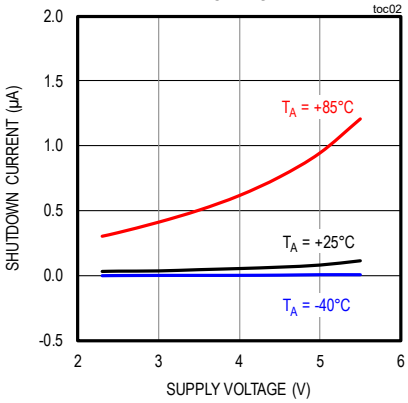
Typical Operating Characteristics

(V_{SYS} = V_{IN} = +3.8V, V_{FB} = V_{OUT} = +3.3V, T_A = +25°C.)

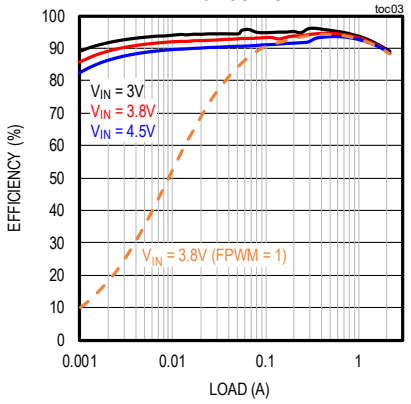
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



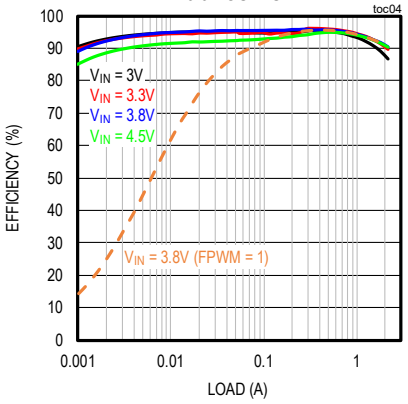
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



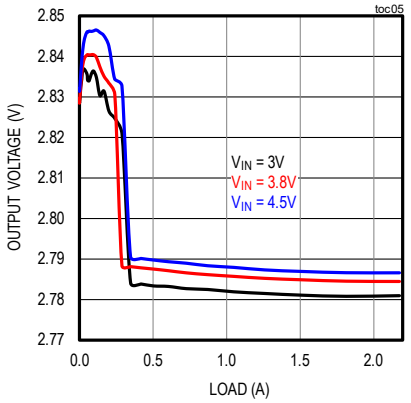
EFFICIENCY vs. LOAD 2.8V OUTPUT



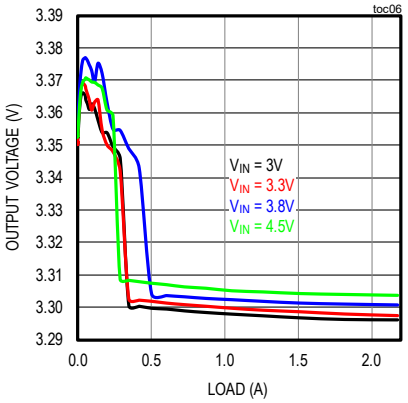
EFFICIENCY vs. LOAD 3.3V OUTPUT



LOAD REGULATION 2.8V OUTPUT



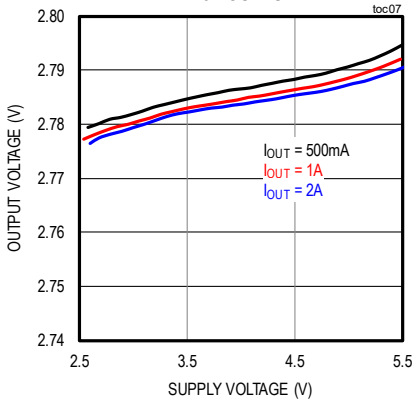
LOAD REGULATION 3.3V OUTPUT



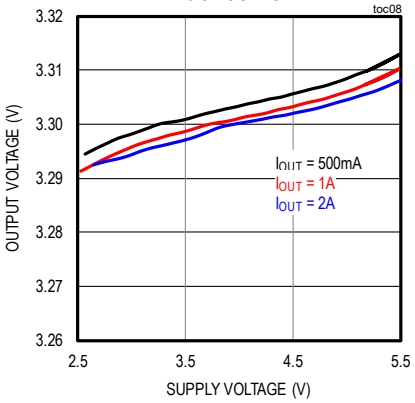
Typical Operating Characteristics (continued)

(V_{SYS} = V_{IN} = +3.8V, V_{FB} = V_{OUT} = +3.3V, T_A = +25°C.)

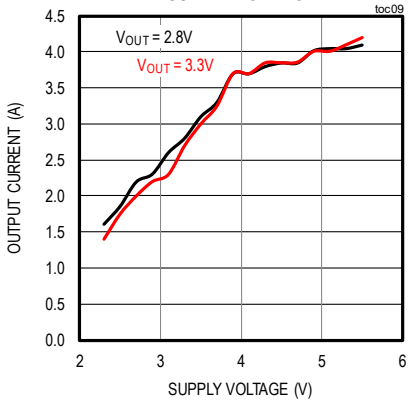
**LINE REGULATION
2.8V OUTPUT**



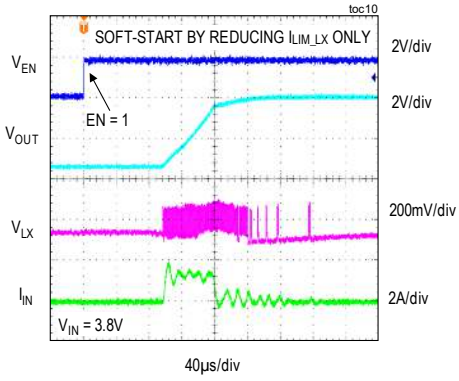
**LINE REGULATION
3.3V OUTPUT**



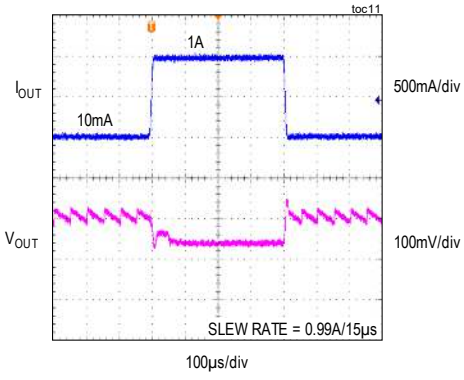
**MAXIMUM OUTPUT CURRENT vs.
SUPPLY VOLTAGE**



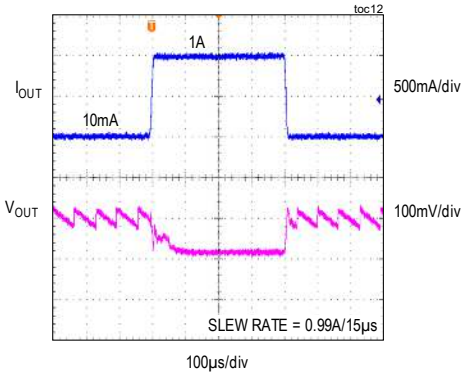
**STARTUP WAVEFORM
3.3V OUTPUT**



**LOAD TRANSIENT RESPONSE
2.8V OUTPUT**



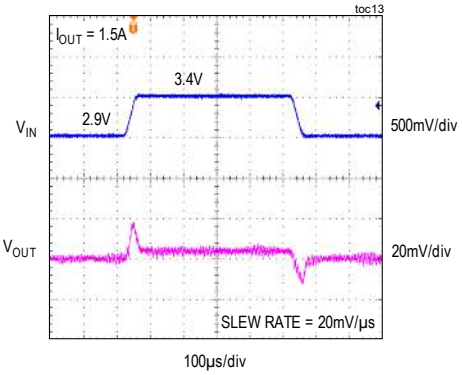
**LOAD TRANSIENT RESPONSE
3.3V OUTPUT**



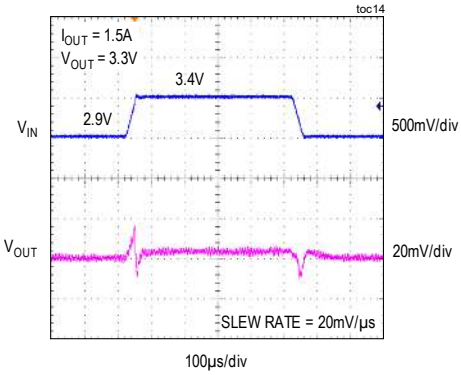
Typical Operating Characteristics (continued)

(V_{SYS} = V_{IN} = +3.8V, V_{FB} = V_{OUT} = +3.3V, T_A = +25°C.)

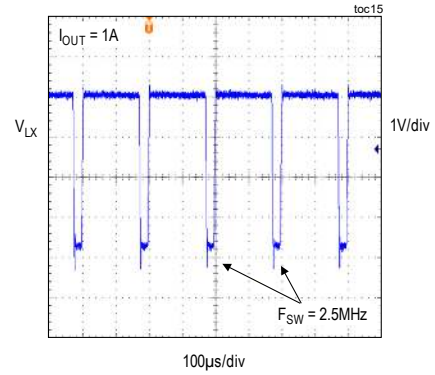
LINE TRANSIENT RESPONSE
2.8V OUTPUT



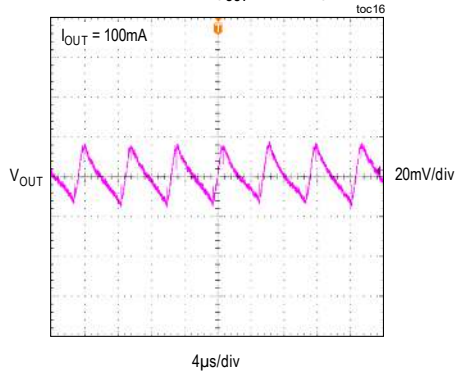
BOOST to BUCK
LINE TRANSIENT RESPONSE



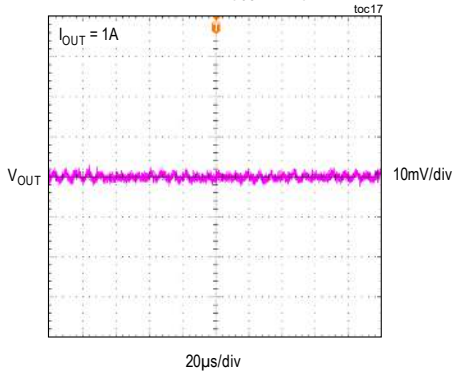
SWITCHING WAVEFORM
3.3V OUTPUT



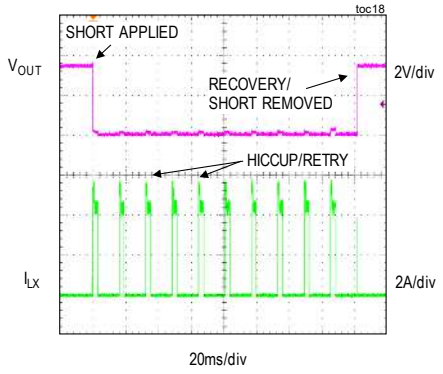
OUTPUT RIPPLE in SKIP MODE
3.3V OUTPUT (I_{OUT} = 100mA)



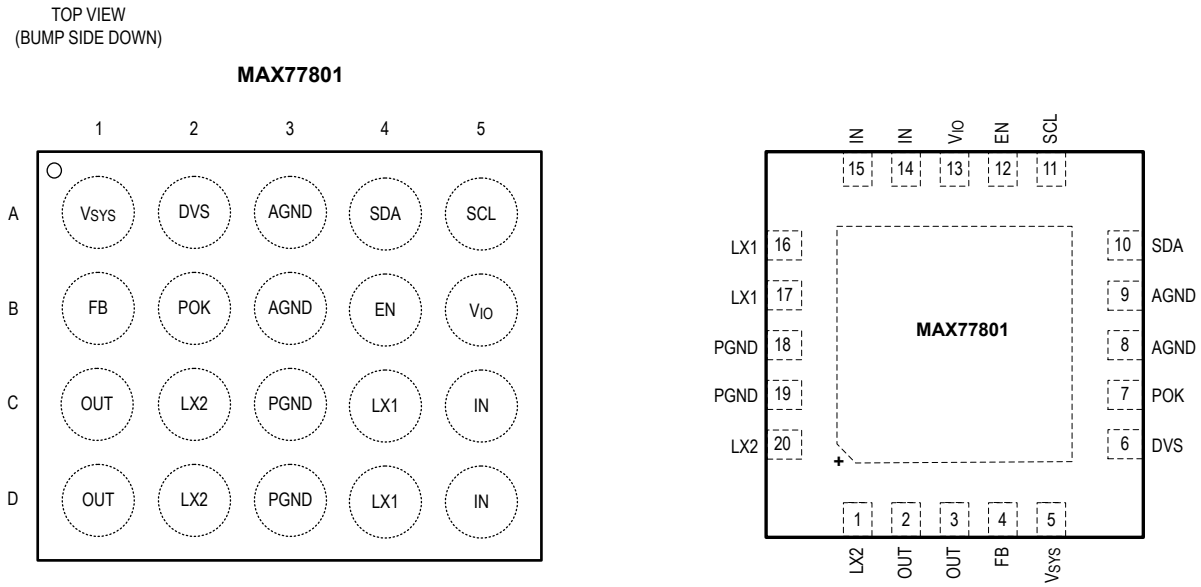
OUTPUT RIPPLE in PWM
3.3V OUTPUT (I_{OUT} = 1A)



SHORT-CIRCUIT AND RECOVERY
3.3V OUTPUT



Pin Configuration



20 WLP
(2.13mm x 1.83mm, 0.4mm PITCH)

20 TQFN
(4mm x 4mm, 0.75mm PITCH)

Pin Description

20-BUMP WLP	20-PIN TQFN	NAME	FUNCTION
A1	5	V_{SYS}	System (Battery) Voltage Input. Bypass to AGND with a 10V, 1µF capacitor.
A2	6	DVS	Dynamic Voltage Scaling Logic Input. Connect to AGND if not used.
A3, B3	8, 9	AGND	Analog Ground. Connect to PGND on the PCB. See the *PCB Layout Guideliness*.
A4	10	SDA	I^2C Serial Interface Data (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor. Connect to AGND if not used.
A5	11	SCL	I^2C Serial Interface Clock (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor. Connect to AGND if not used.
B1	4	FB	Output Voltage Sense.
B2	7	POK	Open-Drain Power-OK Output. Asserts high (high-Z) when buck-boost output reaches 80% of target.
B4	12	EN	Active-High Enable Input. This pin has an 800kΩ internal pulldown to AGND.
B5	13	V_{IO}	I^2C Supply Voltage Input. Bypass to AGND with a 0.1µF capacitor. Connect to AGND if not used.
C1, D1	2, 3	OUT	Output. Bypass to PGND with a 10V 47µF ceramic capacitor.
C2, D2	1, 20	LX2	Switching Node 2.
C3, D3	18, 19	PGND	Power Ground. Connect to AGND on the PCB. See the *PCB Layout Guideliness*.
C4, D4	16, 17	LX1	Switching Node 1.
C5, D5	14, 15	IN	Input. Bypass to PGND with a 10V 10µF ceramic capacitor.

Detailed Description

The MAX77801 is a synchronous step-up/step-down (buck-boost) DC-DC converter with integrated switches. The buck-boost operates on a supply voltage between 2.3V and 5.5V. Output voltage is configurable through I2C from 2.60V to 4.18V in 12.5mV steps. Factory-default startup voltage options of 3.3V, 3.4, and 3.75V are available (see the *Buck-Boost Electrical Characteristics* table).

Buck-Boost Control Scheme

The buck-boost converter operates using a 2.5MHz fixed-frequency pulse-width modulated (PWM) control scheme with current-mode compensation. The buck-boost utilizes an H-bridge topology using a single inductor and output capacitor.

The H-bridge topology has three switching phases. See Figure 1 for details.

- Φ1 switch period (Phase 1: HS1 = ON, LS2 = ON) stores energy in the inductor. Inductor current ramps up at a rate proportional to the input voltage divided by inductance: V_{IN}/L.
- Φ2 switch period (Phase 2: HS1 = ON, HS2 = ON) ramps inductor current up or down depending on the differential voltage across the inductor: $(V_{IN} - V_{OUT})/L$.
- Φ3 switch period (Phase 3: LS1 = ON, HS2 = ON) ramps inductor current down at a rate proportional to the output voltage divided by inductance: $-V_{OUT}/L$.

Boost operation ($V_{IN} < V_{OUT}$) utilizes phase 1 and phase 2 within a single clock period. See the representation of the inductor current waveform for boost mode operation in Figure 1.

Buck operation ($V_{IN} > V_{OUT}$) utilizes phase 2 and phase 3 within a single clock period. See the representation of the inductor current waveform for buck mode operation in Figure 1.

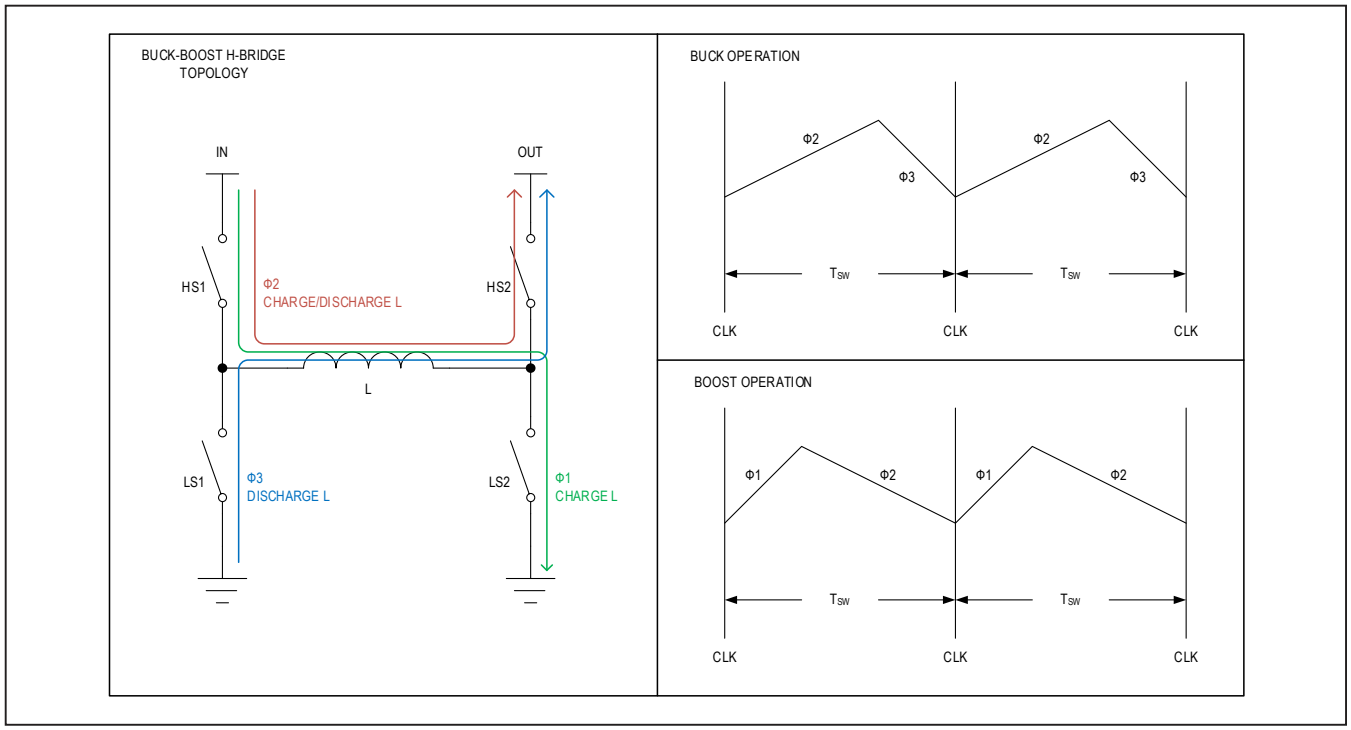


Figure 1. Buck-Boost H-Bridge Topology

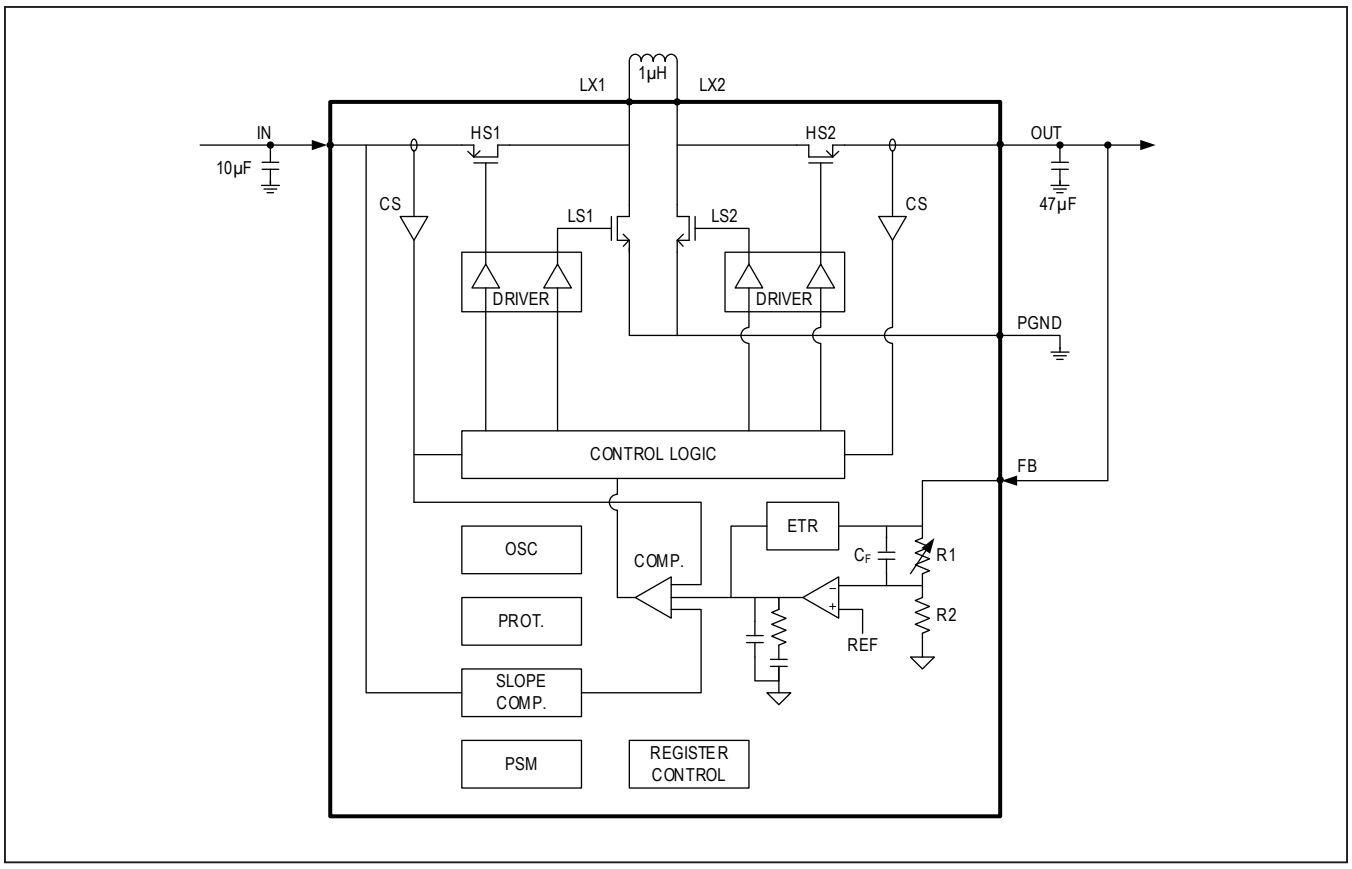


Figure 2. Buck-Boost Block Diagram

Enable Control (EN)

Raise the EN pin voltage above V_{IH} threshold to enable the buck-boost output. Lower EN pin below the V_{IL} threshold to disable it. EN pin has an internal 800kΩ (typ) pulldown resistor to AGND. Clear the EN_PD bit using the I²C interface to disable the internal pulldown (making EN pin high-impedance). The EN_PD bit reset value is 1 (pulldown enabled). Therefore, the internal pulldown resistor is present whenever the MAX77801 starts up.

After the initial buck-boost startup, clear the EN bit through I²C to disable the buck-boost output. Table 1 details the interaction between the EN pin and the EN bit.

Provide a valid V_{IO} and set the EN pin logic-high to enable the I²C serial interface. Serial reads and writes to the EN bit may happen only while V_{IO} is valid and EN pin is logic-high. Setting EN pin to logic-low disables the buck-boost (regardless of EN bit) and causes all registers to reset to default values.

Table 1. EN Logic

EN PIN	EN BIT	I²C SERIAL INTERFACE	BUCK-BOOST OUTPUT
Low	X	Disabled	Disabled
High	0	Enabled	Disabled
High	1 (default)	Enabled	Enabled

Dynamic Voltage Scaling (DVS)

The MAX77801 includes a DVS feature that allows output voltage to change dynamically. The DVS pin status dictates whether the buck-boost regulates to $V_{OUT\_DVS\_L}$ or $V_{OUT\_DVS\_H}$. When EN pin or EN bit goes high, the DVS pin status latches until soft-start completes, so changes on DVS are ignored. Internal logic sets V_{OUT} based on DVS input only after soft-start completion.

The buck-boost converter supports a programmable slew-rate control feature when increasing and decreasing the output voltage. The ramp-up slew rate can be set to 12.5mV/µs or 25mV/µs through RU_SR bit. Also, the ramp-down slew rate can be set to 3.125mV/µs or 6.25mV/µs through RD_SR bit.

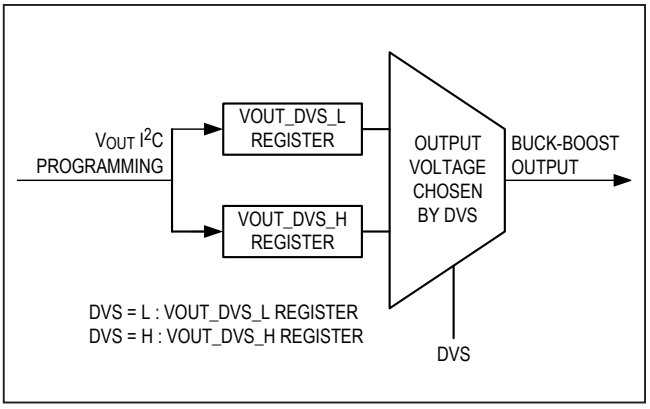


Figure 3. DVS Functional Block Diagram

Soft-Start

The IC implements a soft-start for a fixed time to control inrush current from the supply input (I_{IN}) and prevents droop caused by upstream source impedance. The implementation of soft-start is different among variants. See Table 2 for a summary. The soft-start time begins immediately after the startup delay (t_{ON_DLY}).

MAX77801EWP+T and MAX77801ETP+T achieve soft-start by reducing the peak inductor current limit (I_{LIM_LX}) for a fixed time $t_{SS\_LOW\_ILIM}$ after the buck-boost enables through either the EN pin or EN bit (Figure 4).

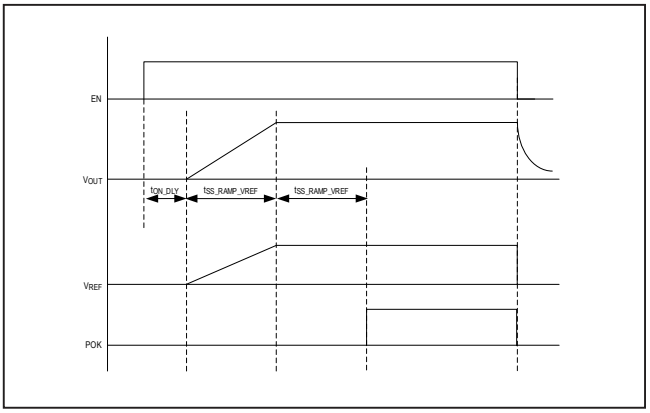


Figure 4. Startup Waveform (Reduce I_{LIM_LX} only)

Table 2. Soft-Start Behavior

PART	SOFT-START IMPLEMENTATION	$t_{SS\_RAMP\_VREF}$ SOFT- START TIME (µs)	$t_{SS\_LOW\_ILIM}$ SOFT- START TIME (µs)	$I_{LIM\_LX\_SS}$ DURING $t_{SS\_LOW\_ILIM}$ (A)	I_{LIM_LX} AFTER $t_{SS\_LOW\_ILIM}$ (A)
MAX77801EWP+ T	Reduce I_{LIM_LX}	N/A	120	1.8	4.5
MAX77801ETP+ T					
MAX77801HEWP+ T	Ramp V_{REF} and Reduce I_{LIM_LX}	300			

MAX77801HEWP+T achieves soft-start by slowly ramping internal reference (V_{REF}) to the target value in a fixed time $t_{SS\_RAMP\_VREF}$, while also reducing the peak inductor current limit (I_{LIM_LX}) for a fixed time $t_{SS\_LOW\_ILIM}$ after the buck-boost enables through either the EN pin or EN bit (Figure 5).

Burst Mode (Enhanced Load Response)

The device implements a burst mode to service short-duration heavy load transients (burst loads). A summary of burst mode operation follows:

- If a heavy load transient happens that requires peak inductor current > I_{LIM_LX} to maintain regulation, then the buck-boost temporarily increases the peak inductor current limit from I_{LIM_LX} to $I_{LIM\_LX\_HIGH}$. (See Table 3.)
- If the heavy load causes a peak inductor current > I_{LIM_LX} for longer than 800µs (typ), then burst mode deactivates and the peak inductor current limit returns to I_{LIM_LX}.

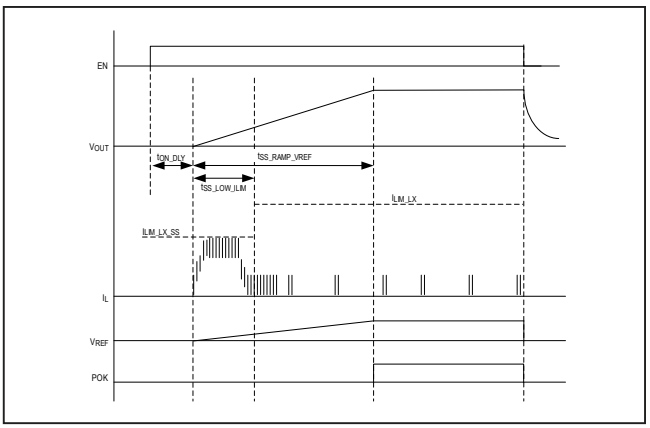


Figure 5. Startup Waveform (Ramp V_{REF} and Reduce I_{LIM_LX})

Table 3. I_{LIM} Levels

INDUCTOR CURRENT LIMIT DURING NORMAL OPERATION I_{LIM_LX} (A)	INDUCTOR CURRENT LIMIT DURING BURST MODE $I_{LIM\_LX\_HIGH}$ (A)
4.5	5.5

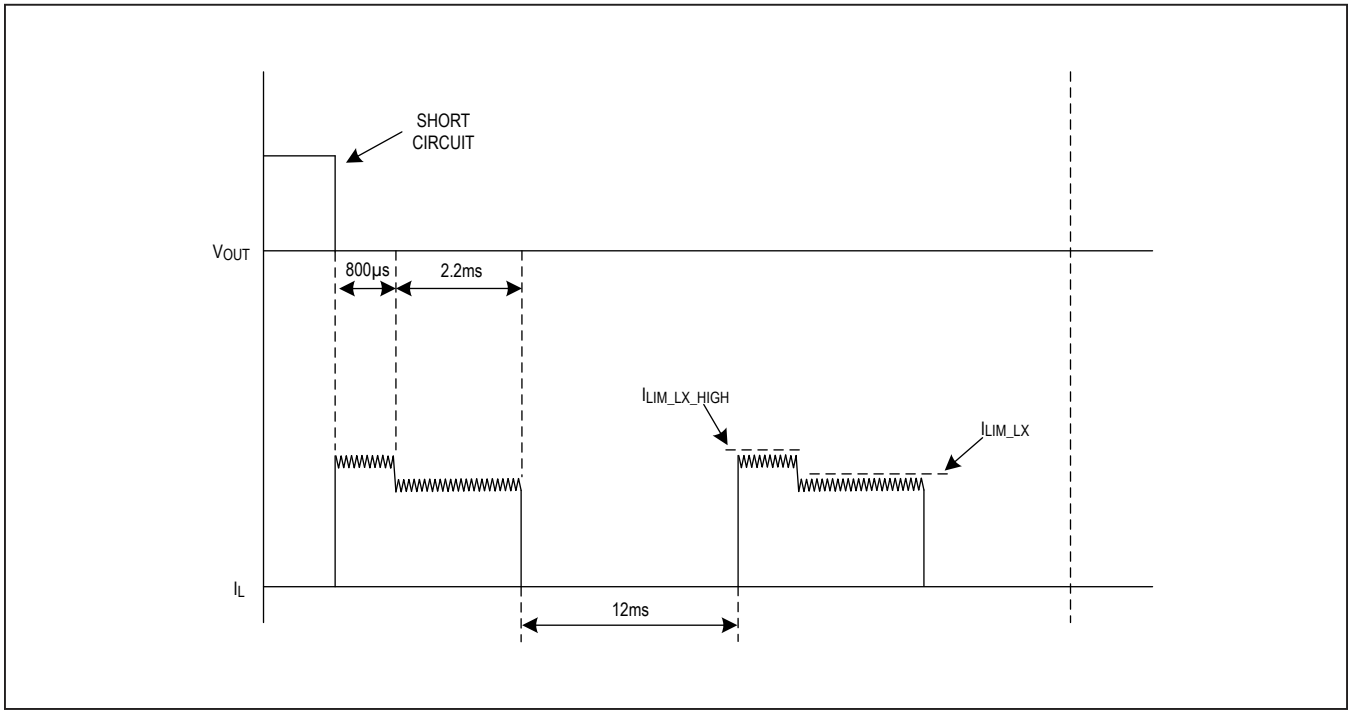


Figure 6. Short-Circuit Waveform

Power-OK (POK) Output

The device features an open-drain POK output to monitor the output voltage. POK requires an external pullup resistor (typically 10kΩ to 100kΩ).

POK is active-high by default. Use the POK_POL bit to change the POK polarity to active-low. See the *Register Map* for details.

While POK_POL = 1 (active-high, default state), POK goes high (high-impedance) after the buck-boost output increases above 80% of the target regulation voltage. POK goes low when the output drops below 75% of the target or when the buck-boost is disabled.

Output Voltage Selection and Slew-Rate Control

Write the VOUT_DVS_L[6:0] or VOUT_DVS_H[6:0] bit field through I²C to configure the target output voltage (V_{OUT}) between 2.60V and 4.18V in 12.5mV steps. The default value of the bit fields is factory programmable. See the *Buck-Boost Electrical Characteristics* table for the default V_{OUT} associated with each orderable part number. Overwriting the default value through I²C sets a new target V_{OUT} until registers reset.

Changing the bit fields while the buck-boost output is enabled causes the device to respond in the following way:

- V_{OUT} ramps up at a rate set by RU_SR (12.5mV/µs or 25mV/µs) when the V_{OUT} target is *increased*.
- V_{OUT} ramps down at a rate set by RD_SR (3.125mV/µs or 6.25mV/µs) when the V_{OUT} target is *decreased*.

See the *Register Map* for details about the RU_SR and RD_SR bits.

Output Overvoltage Protection (OVP)

The device has an internal output overvoltage protection (OVP) circuit that monitors V_{OUT} for overvoltage faults. The buck-boost disables if the output exceeds the overvoltage threshold set by the OVP_TH[1:0] bit field.

Disable OVP by programming OVP_TH[1:0] to 0b00 using I²C. The default OVP threshold is 0b11 (120% of the target V_{OUT}).

The OVP status bit continuously mirrors the status of the OVP circuit. See the *Register Map* for details.

Thermal Shutdown

The device has an internal thermal protection circuit that monitors die temperature. The buck-boost disables if the die temperature exceeds T_{SHDN} (+165°C typ). The buck-boost enables again after the die temperature cools by approximately 20°C.

The TSHDN status bit continuously mirrors the status of the thermal protection circuit. See the *Register Map* for details.

I²C Serial Interface

The device features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77801 is a slave-only device that that relies on an external bus master to generate SCL. SCL clock rates from 0Hz to 3.4MHz are supported. I²C is an open-drain bus, and therefore, SDA and SCL require pullups (of 500Ω or greater).

The device's I²C communication controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. The slave address of the device is shown in Table 4.

The device uses 8-bit registers with 8-bit register addressing. They support standard communication protocols:

- Writing to a single register
- Writing to multiple sequential registers with an automatically incrementing data pointer
- Reading from a single register
- Reading from multiple sequential registers with an automatically incrementing data pointer

For additional information on the I²C protocols, refer to the *Serial Interface* section.

Table 4. I²C Slave Address

7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
0x18 0b 001 1000	0x30 0b 0011 0000	0x31 0b 0011 0001

Applications Information

Inductor Selection

Choose a 1µH inductor with a saturation current of 7A or higher. Table 5 recommends inductors for the MAX77801. Always choose the inductor carefully by consulting the manufacturer's latest released data sheet.

Input Capacitor Selection

Choose the input capacitor (C_{IN}) to be a 10µF ceramic capacitor that maintains at least 2µF of effective capacitance at its working voltage. Larger values improve the decoupling of the buck-boost. C_{IN} reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily as compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required to keep the output-voltage ripple small and the regulation loop stable. Choose the effective C_{OUT} to be 16µF minimum. Considering the DC bias characteristic of ceramic capacitors, a 47µF 10V capacitor is recommended for most applications.

Effective C_{OUT} is the actual capacitance value seen by the buck-boost output during operation. Choose effective C_{OUT} carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily as compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. For the WLP package, an HDI (high density interconnect) PCB is required. Figure 7 shows an example HDI PCB layout for the MAX77801 WLP package. Figure 9 shows an example PCB layout for the MAX77801 FC2QFN package.

When designing the PCB, follow these guidelines:

1) Place the input capacitors (C_{IN}) and output capacitors (C_{OUT}) immediately next to the IN pin and OUT pin, respectively, of the IC. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high-voltage spikes and may damage the internal switching MOSFETs. See Figure 8 for an illustration.
2) Place the inductor next to the LX bumps/pins (as close as possible) and make the traces between the LX bumps/pins and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not make LX traces take up an excessive amount of area. The voltage on this node switches very quickly, and additional area creates more radiated emissions.

Table 5. Suggested Inductors

MFGR.	SERIES	NOMINAL INDUCTANCE (µH)	TYPICAL DC RESISTANCE (mΩ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT = 40°C RISE	DIMENSIONS L x W x H (mm)
Coilcraft	XAL4020-102MEB	1.0	13	8.7	9.6	4.0 x 4.0 x 2.1
Sumida	CDMT40D20HF-1R0NC	1.0	13	8.7	9.6	4.3 x 4.3 x 2.1

3) Prioritize the low-impedance ground plane of the PCB directly underneath the IC, C_{OUT}, C_{IN}, and inductor. Cutting this ground plane risks interrupting the switching current loops.
4) AGND must carefully connect to PGND on the PCB's low-impedance ground plane. Connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) away from any critical loops.
5) The IC requires a quiet supply input (SYS) which is often the same net as IN. Carefully bypass SYS to AGND with a dedicated capacitor (C_{SYS}) as close as possible to the IC. Route a dedicated trace between C_{SYS} and the SYS bump/pin. Avoid connecting SYS directly to the nearest IN bumps/pins without dedicated bypassing.
6) Connect the FB bump/pin to the regulating point with a dedicated trace away from noisy nets such as LX1 and LX2.
7) Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
8) Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to **Tutorial 5527** for more information.

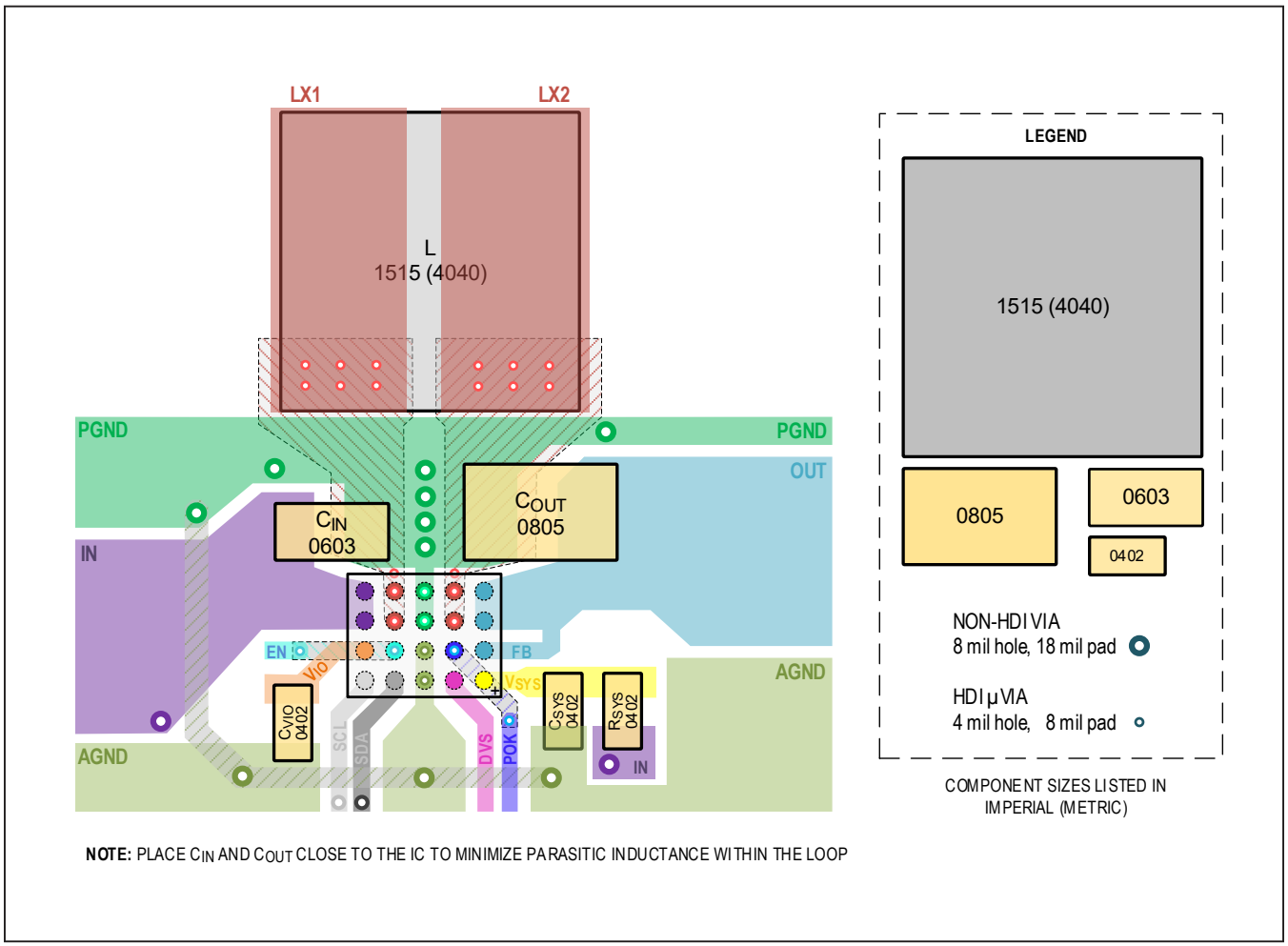


Figure 7. PCB Layout Example (WLP)

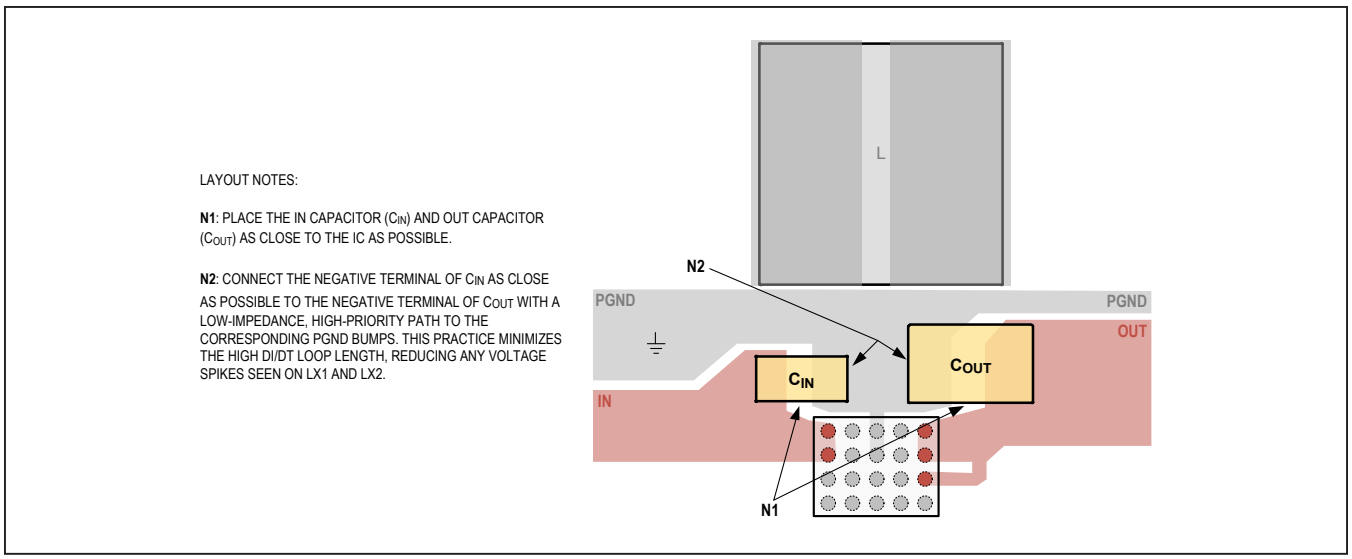


Figure 8. Recommended Capacitor Placement

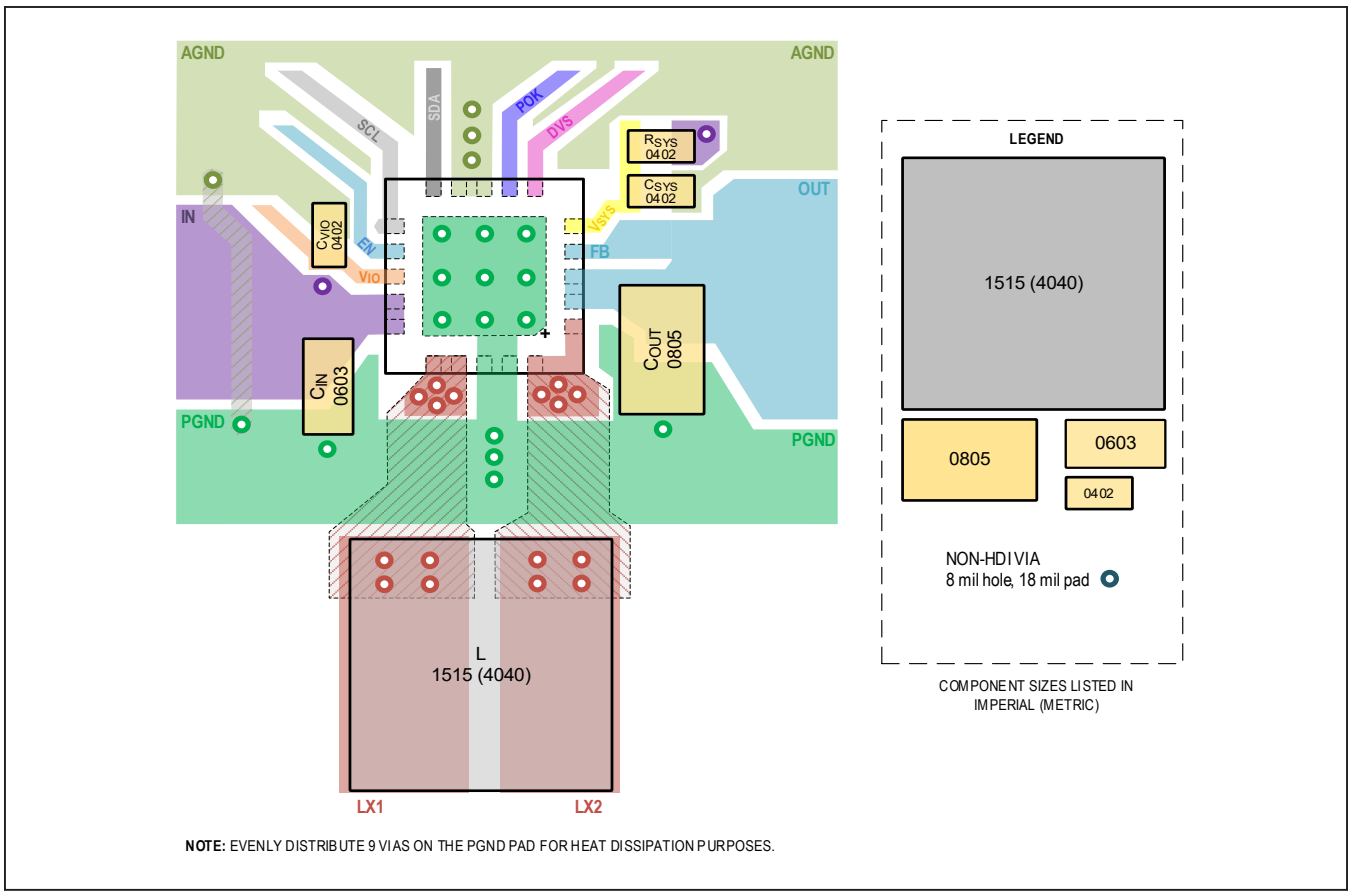


Figure 9. PCB Layout Example (TQFN)

Serial Interface

The I2C-compatible, 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the *Register Map* section for details.

The I2C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I2C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 10 shows an example of a typical I2C system. A device on I2C bus that sends data to the bus is called a “transmitter”. A device that receives data from the bus is called a “receiver”. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is called a “master”. Any device that is being addressed by the master is called a “slave”. When the MAX77801 I2C-compatible interface is operating, it is a slave on I2C bus, and it can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

START and STOP Conditions

When the I2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition (S). A START condition (S) is a high-to-low transition on SDA with SCL high. A STOP condition (P) is a low-to-high transition on SDA with SCL high.

A START condition (S) from the master signals the beginning of a transmission. The master terminates transmission by issuing a NOT-ACKNOWLEDGE (nA) followed by a STOP condition (P).

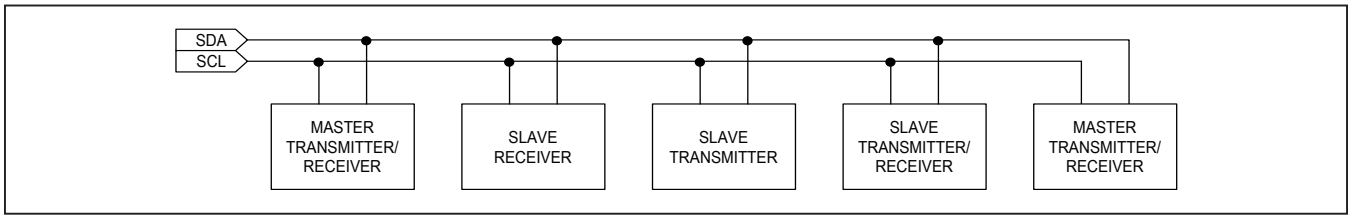


Figure 10. Functional Logic Diagram for Communications Controller

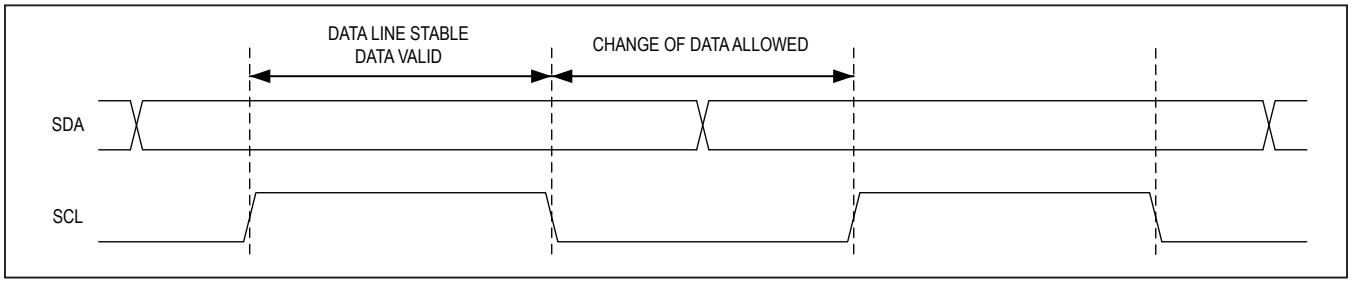


Figure 11. I2C Bit Transfer

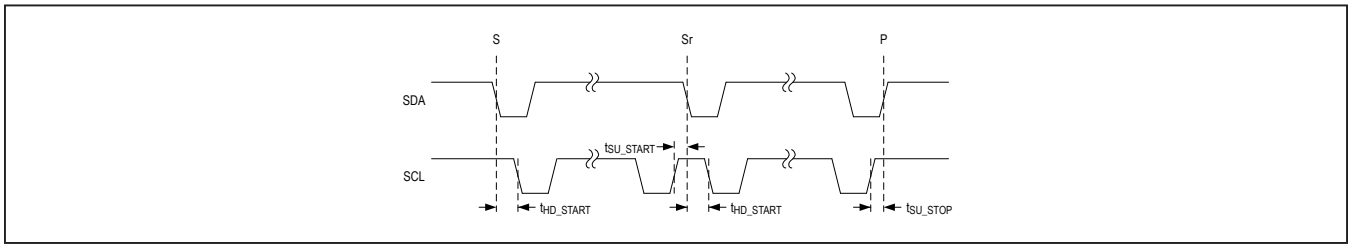


Figure 12. START and STOP Conditions

A STOP condition (P) frees the bus. To issue a series of commands to the slave, the master may issue REPEATED START (Sr) conditions instead of a STOP condition (P) in order to maintain control of the bus. In general, a REPEATED START (Sr) condition is functionally equivalent to a regular START condition (S).

When a STOP condition (P) or incorrect address is detected, the MAX77801 internally disconnects SCL from I2C serial interface until the next START condition (S), minimizing digital noise and feedthrough.

Acknowledge

Both the I2C bus master and the MAX77801 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high portion of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high portion of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The I2C slave address of the MAX77801 is shown in Table 6.

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77801 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77801 does not implement the I2C specification “General Call Address.” If the MAX77801 detects a general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

Communication Speed

The MAX77801 supports the following I2C revision 3.0-compatible communication speeds:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Table 6. I2C Slave Address

SLAVE ADDRESS (7 BIT)	SLAVE ADDRESS (WRITE)	SLAVE ADDRESS (READ)
0x18 (001 1000)	0x30 (0011 0000)	0x31 (0011 0001)

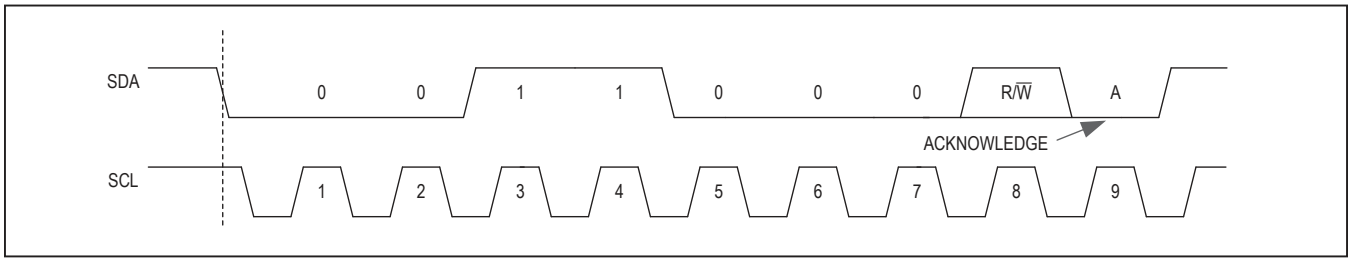


Figure 13. Slave Address Byte Example

Operating in high-speed mode requires some special considerations. For the full list of considerations, refer to the I²C revision 3.0 specification. The major considerations with respect to the MAX77801 are:

- The master device shall use current source pullups to shorten the signal rise times.
- The slave device must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition (P), the MAX77801 input filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the protocol described in the *Engaging in High-Speed Mode* section.

Communication Protocols

The MAX77801 supports both writing and reading from its registers. The following sections show the I²C communication protocols available.

Writing to a Single Register

Figure 14 shows the protocol for writing to a single register. This protocol is the same as SMBus specification's "Write Byte" protocol.

The "Write Byte" protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

Writing to Sequential Registers

Figure 15 shows the protocol for writing to sequential registers. This protocol is similar to the "Write Byte" protocol, except the master continues to write after the slave device receives the first byte of data. When the master is done writing, it issues a STOP condition (P) or a REPEATED START condition (Sr).

The "Writing to Sequential Registers" protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires. During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
9. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

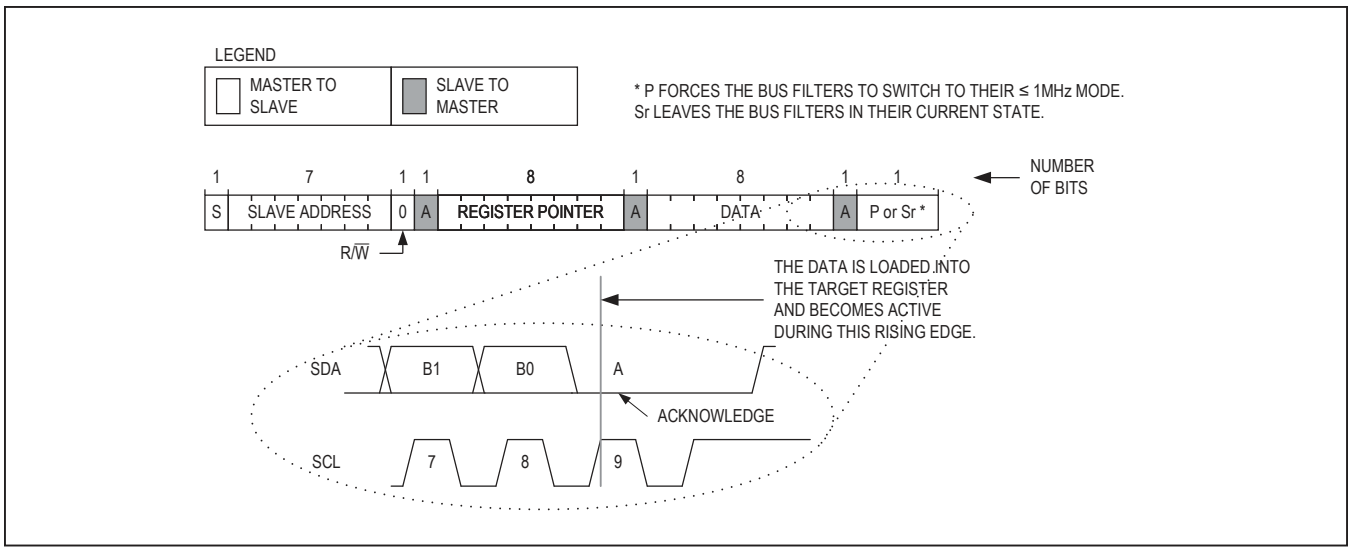


Figure 14. Writing to a Single Register

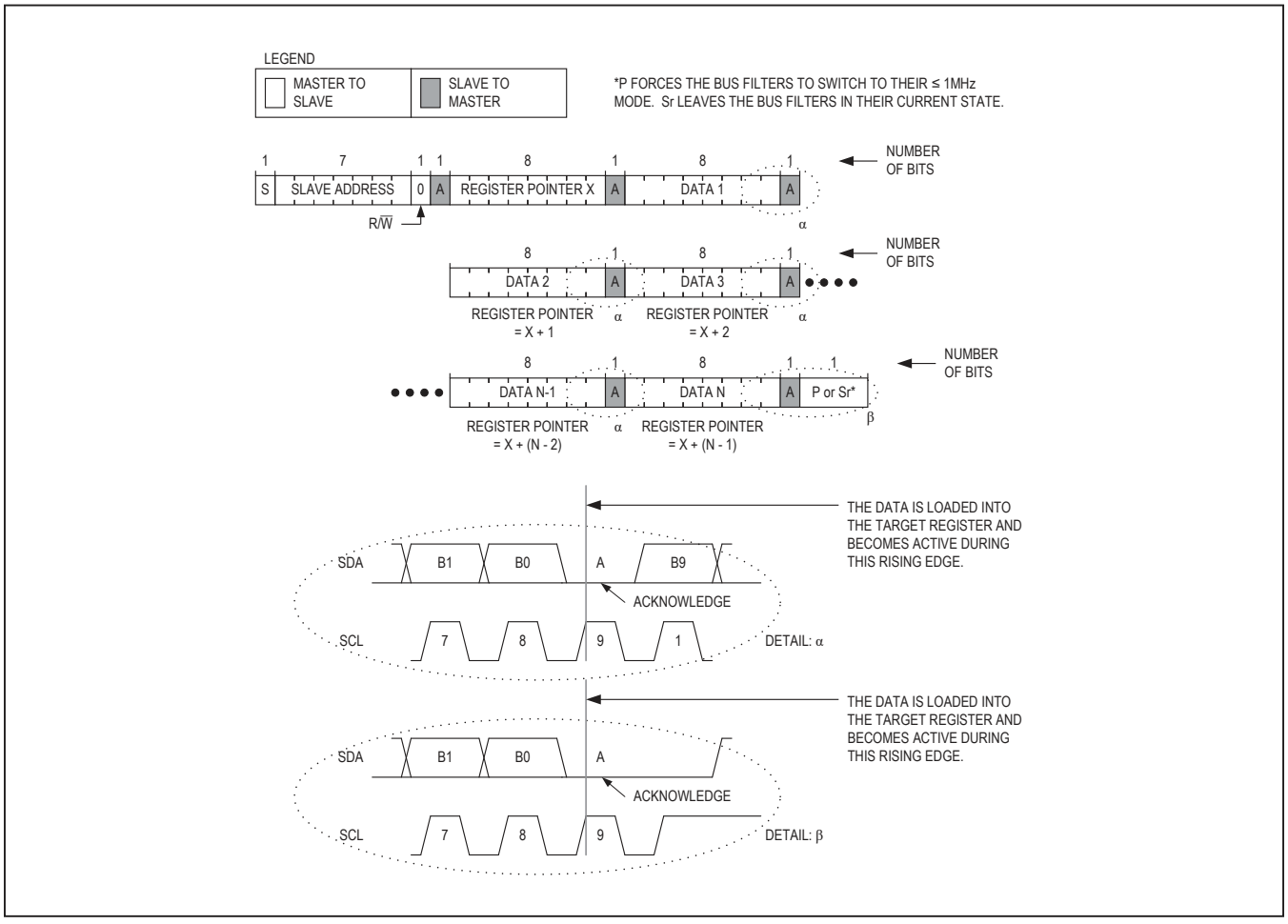


Figure 15. Writing to Sequential Registers

Reading from a Single Register

Figure 16 shows the protocol for reading from a single register. This protocol is the same as SMBus specification's "Read Byte" protocol.

The "Read Byte" protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START condition (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

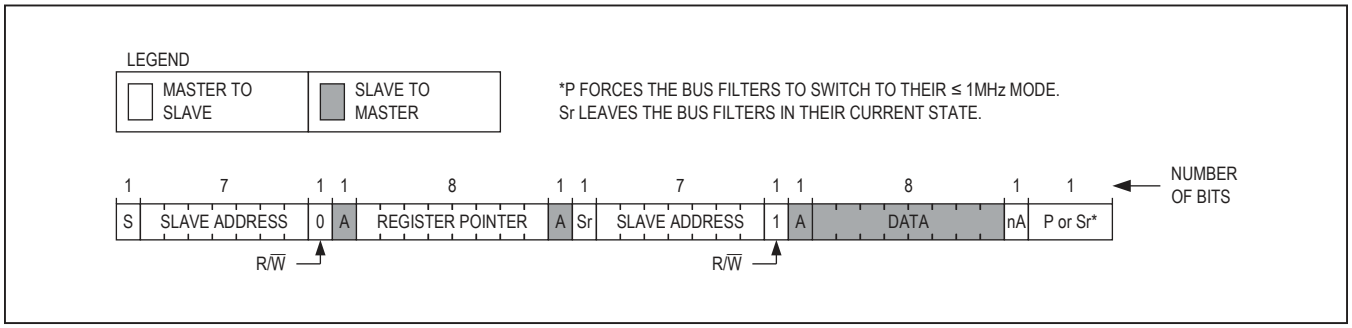


Figure 16. Reading from a Single Register

Reading from Sequential Registers

Figure 17 shows the protocol for reading from sequential registers. This protocol is similar to the “Read Byte” protocol, except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data. When the master has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP condition (P) to end the transmission.

The “Continuous Read from Sequential Registers” protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START condition (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

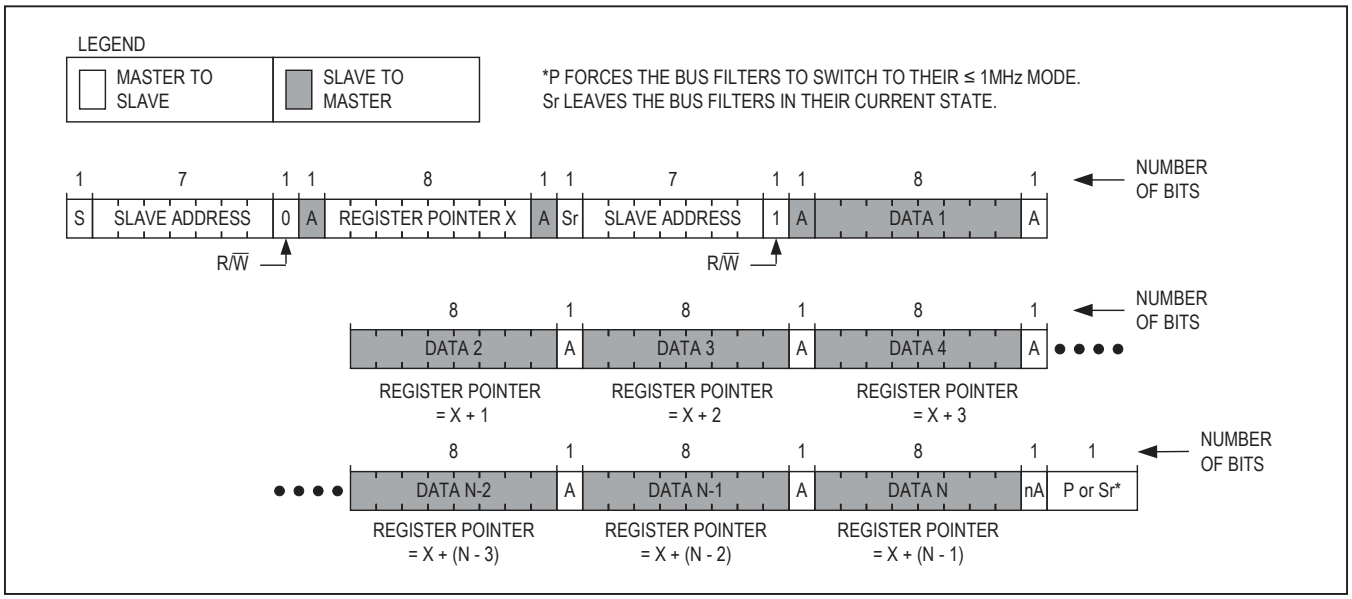


Figure 17. Reading Continuously from Sequential Registers

Engaging in High-Speed Mode

Figure 18 shows the protocol for engaging in high-speed mode operation, which allows the bus to operate at speed up to 3.4MHz.

The “Engage in High-Speed Mode” protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower
2. The master sends a START condition (S).
3. The master sends the 8-bit master code of 0000 1xxx where “xxx” are don’t care bits.
4. The addressed slave issues a NOT-ACKNOWLEDGE (nA).
5. The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a STOP condition (P) is issued. Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation.

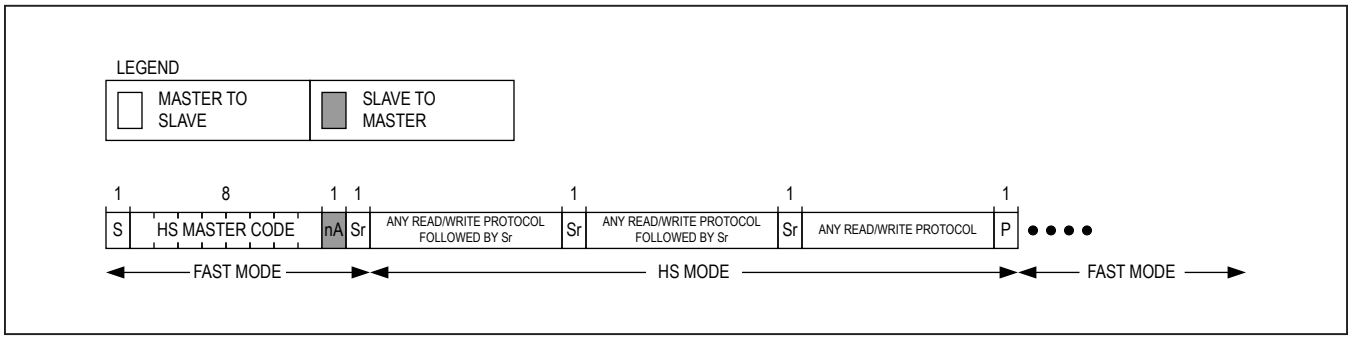


Figure 18. Engaging in High-Speed Mode

Register Map

Register Reset Conditions

Registers reset to their default values when either of the following conditions become true:

- Undervoltage Lockout ($V_{SYS} < V_{UVLO\_F}$)
- Device Disabled (EN pin = logic low)

MAX77801 Registers

I^2C Device Address: 0x18 (7-bit)

ADDRESS	NAME	ACCESS	MSB							LSB	RESET
0x00	DEVICE_ID	R	RESERVED								–
0x01	STATUS	R	RESERVED				TSHDN	POKn	OVP	OCP	0x00
0x02	CONFIG1	R/W	RESERVED	RESERVED	RU_SR	RD_SR	OVP_TH[1:0]		AD	FPWM	0x0E
0x03	CONFIG2	R/W	RESERVED	EN	EN_PD	POK_POL	RESERVED				0x70
0x04	VOUT_DVS_L	R/W	RESERVED	VOUT_DVS_L[6:0]							0x38
0x05	VOUT_DVS_H	R/W	RESERVED	VOUT_DVS_H[6:0]							varies

Register Details

DEVICE ID (0x00)

BIT	7	6	5	4	3	2	1	0
FIELD	RESERVED[7:0]							
RESET	–							
ACCESS	Read Only							

BIT FIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:0	Reserved. Bits for internal use only.	N/A

STATUS (0x01)

BIT	7	6	5	4	3	2	1	0
FIELD	RESERVED[7:4]				TSHDN	POKn	OVP	OCP
RESET	0b0000				0b0	0b0	0b0	0b0
ACCESS	Read Only				Read Only	Read Only	Read Only	Read Only

BIT FIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:4	Reserved. Reads are *don't care.*	N/A
TSHDN	3	Thermal Shutdown Status	0 = Junction temperature OK ($T_J < T_{SHDN}$) 1 = Thermal shutdown ($T_J \geq T_{SHDN}$)
POKn	2	Power-OK Status	0 = Output OK (V_{OUT} > 80% of target) 1 = Output not OK (V_{OUT} < 75% of target) or disabled.
OVP	1	Output Overvoltage Status	0 = Output OK (V_{OUT} < the OVP threshold set by OVP_TH[1:0]) or disabled. 1 = Output overvoltage. V_{OUT} > the OVP threshold set by OVP_TH[1:0].
OCP	0	Overcurrent Status	0 = Current OK 1 = Overcurrent

CONFIG1 (0x02)

BIT	7	6	5	4	3	2	1	0
FIELD	RESERVED		RU_SR	RD_SR	OVP_TH[1:0]		AD	FPWM
RESET	0b00		0b0	0b0	0b11		0b1	0b0
ACCESS	Read, Write		Read, Write	Read, Write	Read, Write		Read, Write	Read, Write

BIT FIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Bits are *don't care*.	N/A
RU_SR	5	V_{OUT} Rising Ramp Rate Control. V_{OUT} increases with this slope whenever the output voltage target is modified upwards while the converter is enabled.	0 = +12.5mV/µs 1 = +25mV/µs
RD_SR	4	V_{OUT} Falling Ramp Rate Control. V_{OUT} decreases with this slope whenever the output voltage target is modified downwards while the converter is enabled.	0 = -3.125mV/µs 1 = -6.25mV/µs
OVP_TH[1:0]	3:2	V_{OUT} Overvoltage Protection (OVP) Threshold Control	00 = No OVP (protection disabled) 01 = 110% of V_{OUT} target 10 = 115% of V_{OUT} target 11 = 120% of V_{OUT} target
AD	1	Output Active Discharge Resistor Enable	0 = Disabled 1 = Enabled
FPWM	0	Converter Mode Control	0 = SKIP Mode 1 = Forced PWM (FPWM) mode

CONFIG2 (0x03)

BIT	7	6	5	4	3	2	1	0
FIELD	RESERVED	EN	EN_PD	POK_POL	RESERVED			
RESET	0b0	0b1	0b1	0b1	0b0000			
ACCESS	Read, Write	Read, Write	Read, Write	Read, Write	Read, Write			

BIT FIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved. Bit is a *don't care*.	N/A
EN	6	Buck-boost Output Software Enable Control. See Table 1.	While EN (pin) = logic low: 0 or 1 = Output disabled While EN (pin) = logic high: 0 = Output disabled 1 = Output enabled
EN_PD	5	EN Pin Input Pulldown Resistor Enable Control	0 = Pulldown disabled 1 = Pulldown enabled
POK_POL	4	Power-OK (POK) Output Pin Polarity Control	0 = Active-low 1 = Active-high
RESERVED	3:0	Reserved. Bits are *don't care*.	N/A

VOUT_DVS_L (0x04)

BIT	7	6	5	4	3	2	1	0
FIELD	RESERVED	VOUT_DVS_L[6:0]						
RESET	0b0	0b0	0b1	0b1	0b1	0b0	0b0	0b0
ACCESS	Read, Write	Read, Write						

BIT FIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved. Bit is a *don't care*.	N/A
VOUT_DVS_L	6:0	Output Voltage Control (DVS Logic Low). Sets the V_{OUT} target when DVS pin is logic low. Configurable in 12.5mV per LSB from 0x00 (2.60V) to 0x7F (4.1875V). The default value of this register is pre-set. See the *Ordering Information* table. Overwriting the default value sets a new target output voltage.	0x00 = 2.60V 0x01 = 2.6125V 0x02 = 2.6250V … **0x38 = 3.30V** … 0x40 = 3.40V … 0x7E = 4.1750V 0x7F = 4.1875V

VOUT_DVS_H (0x05)

BIT	7	6	5	4	3	2	1	0
FIELD	RESERVED	VOUT_DVS_H[6:0]						
RESET (WLP)	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
RESET (TQFN)	0b0	0b1	0b0	0b1	0b1	0b1	0b0	0b0
ACCESS	Read, Write	Read, Write						

BIT FIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved. Bit is a *don't care*.	N/A
VOUT_DVS_H	6:0	Output Voltage Control (DVS Logic High). Sets the V_{OUT} target when DVS pin is logic high. Configurable in 12.5mV per LSB from 0x00 (2.60V) to 0x7F (4.1875V). The default value of this register is pre-set. See the *Ordering Information* table. Overwriting the default value sets a new target output voltage.	0x00 = 2.60V 0x01 = 2.6125V 0x02 = 2.6250V … **0x40 = 3.40V** … **0x5C = 3.75V** … 0x7E = 4.1750V 0x7F = 4.1875V

Ordering Information

PART	DEFAULT V_{OUT}	SOFT-START TIME[1]	PIN-PACKAGE
MAX77801EWP+T	3.3V/3.4V	120µs	20 WLP
MAX77801ETP+T	3.3V/3.75V	120µs	20 TQFN
MAX77801HEWP+T	3.3V/3.4V	300µs	20 WLP

[1]See the Soft-Start section for more information.
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 WLP	W201F2+1	**21-0771**	Refer to **Application Note 1891**
20 TQFN	T2044-3C	**21-0139**	**90-0037**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/15	Initial release	—
1	4/17	Added MAX77801ETP TQFN package information, updated *Benefits and Features* section, updated *Communication Protocals* sections, updated Figures 10–12, updated tables for *Package Thermal Characteristics*, *Buck-Boost Electrical Characteristics*, *Register Map*, *VOUT_DVS_H*, *Ordering Information*, and *Package Information*	1–3, 8, 14–19, 23, 24
2	2/18	Corrected a typo in Figure 5	11
3	3/18	Added MAX77801ETP default V_{OUT} to *Electrical Characteristics* table	2
4	10/19	Updated front page, *Typical Operating Characteristics*, *Bump/Pin Configuration*, *Detailed Description*, *Applications Information*, *PCB Layout Guidelines*, Figures 1-8, *Register Map*, *Ordering Information* table, deleted original Note 1 and renumbered remaining Notes	1–3, 7–11, 19–24
5	11/19	Replaced *Typical Application Circuit* Figure, updated *Absolute Maximum Ratings*, updated EC Globals, *Buck-Boost Electrical Characteristics* table and *I^2C Electrical Characteristics* table, updated Note 2, updated sub title for *Typical Operating Characteristics,* updated *Bump/Pin Configurations* figure and *Bump/Pin Description* table, updated Figure 2, replaced OUTS with FB in the *PCB Layout Guideline* section, updated Figures 6 and 8	1–10, 12, 17, 18
6	7/22	*Updated Register Map*	26–28
7	1/23	Updated *General Description, Benefits and Features, Absolute Maximum Ratings, Buck-Boost Electrical Characteristics, Pin Configuration, Pin Description, Enable Control (EN),* Table 1*, Dynamic Voltage Scaling (DVS),* Figure 5*, Output Voltage Selection and Slew-Rate Control, Output Overvoltage Protection (OVP), Thermal Shutdown, I^2C Serial Interface, Input Capacitor Selection, Output Capacitor Selection, PCB Layout Guidelines,* Table 5*, System Configuration, START and STOP Conditions, Acknowledge, Slave Address, General Call Address, Communication Speed,* Table 6*, Communication Protocols, Writing to a Single Register, Writing to Sequential Registers,* Figures 13, 14, and 15*, Reading from a Single Register, Reading from Sequential Registers,* Figure 16*, Engaging in High-Speed Mode,* Figure 17*, Register Map*	1, 2, 4, 10, 12–17, 19–29
8	6/23	Updated *Buck-Boost Electrical Characteristics* table, TOC10, and *Soft-Start* section, renumbered Figures 5 to 17, updated *START and STOP Conditions* section, *Register Map*, and *Ordering Information* table	3, 8, 13, 14, 16–25, 28, 30