NCP1339

High-Voltage, Quasi-Resonant Controller featuring Valley Lock-Out and Power Saving Mode

The NCP1339 is a highly integrated quasi−resonant flyback controller capable of controlling rugged and high−performance off−line power supplies as required by adapter applications. With an integrated active X−cap discharge feature and power savings mode, the NCP1339 can enable no−load power consumption below 10 mW for 45 W notebook adapters.

The quasi−resonant current−mode flyback stage features a proprietary valley−lockout circuitry, ensuring stable valley switching. This system works down to the 6th valley and toggles to a frequency foldback mode to eliminate switching losses. When the loop tends to force below 25−kHz frequencies, the NCP1339 skips cycles to contain the power delivery.

To help build rugged converters, the controller features several key protective features: an internal brown−out, a non−dissipative Over Power Protection for a constant maximum output current regardless of the input voltage, a latched over−voltage protection through a dedicated pin.

Features

- High−voltage Current Source for Lossless Start−up Sequence
- X2 Capacitors Discharge Capability
- Power Savings Mode (PSM) for Extremely Low No−Load Power:
- Wide V_{CC} Range from 10 V to 28 V
- Latching−off 28−V V_{CC} Over−Voltage Protection
- Abnormal Overcurrent Fault Protection for Winding Short Circuit or Inductor Saturation Detection
- Integrated High−Voltage Startup Circuit with Brown−Out Detection
- Fault Input for Severe Fault Conditions, NTC Compatible for OTP
- Circuit Latching Off In Severe Fault Detection (OVP or OTP)
- Internal Temperature Shutdown
- Valley Switching Operation with Valley−Lockout for Noise−Free Operation
- Frequency Fold−back for Highest Performance in Standby Mode
- 25−kHz Clamp and Skip Mode
- Timer−Based Overload Protection (Latched or Auto−Recovery Options)
- Adjustable Overpower Protection
- 4−ms Soft−Start Timer
- ZCD Blanking Time to Ignore Leakage Ringing at Turn−Off: 3 μs for C, D and E versions and 0.7 μs for F, G, H, I and J versions
- Ready for High−Density QR design (F, G, H, I and J versions)
- These Devices are Pb−Free and are RoHS Compliant

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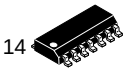
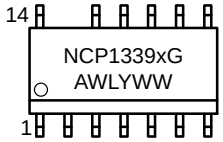


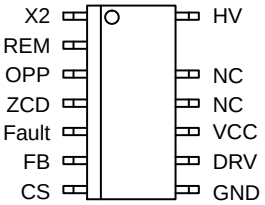
SOIC−14 NB
(LESS PIN 13)
D SUFFIX
CASE 751AN

MARKING DIAGRAM

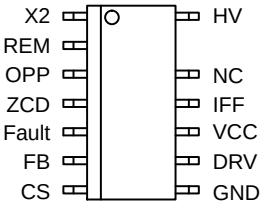


NCP1339 = Specific Device Code
x = C, D, E, F, G, H, I or J
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



(For C, D, E, F, G, and H versions)



(For I and J versions)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 31 of this data sheet.

PART NUMBER MATRIX

Device	Version	Overload Protection	Abnormal Overcurrent Fault	ZCD Blanking Time	Jittering Function	Adjustable Frozen Peak Current (IFF pin)
NCP1339CDR2G	NCP1339C	Auto−recovery	Auto−recovery	3 μs	Disabled	Disabled
NCP1339DDR2G	NCP1339D	Latching−off	Latching−off	3 μs	Disabled	Disabled
NCP1339EDR2G	NCP1339E	Latching−off	Latching−off	3 μs	Enabled	Disabled
NCP1339FDR2G	NCP1339F	Latching−off	Latching−off	0.7 μs	Enabled	Disabled
NCP1339GDR2G	NCP1339G	Auto−recovery	Auto−recovery	0.7 μs	Enabled	Disabled
NCP1339HDR2G	NCP1339H	Auto−recovery	Auto−recovery	0.7 μs	Disabled	Disabled
NCP1339IDR2G	NCP1339I	Latching−off	Latching−off	0.7 μs	Enabled	Enabled
NCP1339JDR2G	NCP1339J	Auto−recovery	Auto−recovery	0.7 μs	Enabled	Enabled

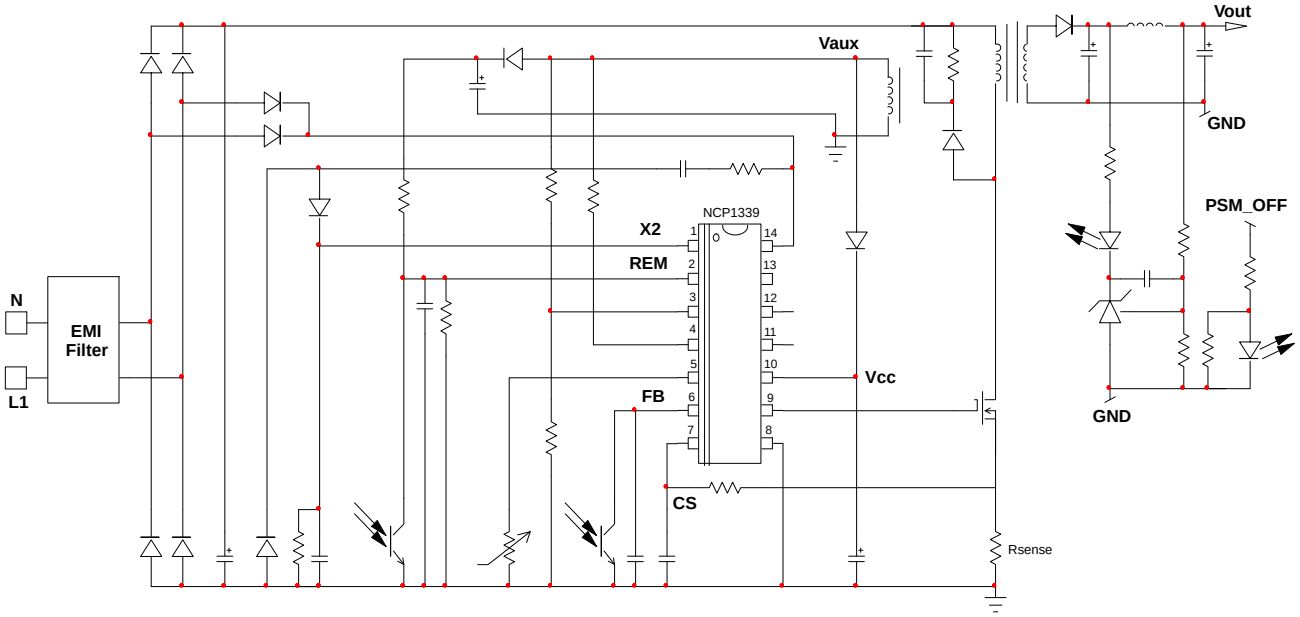


Figure 1. NCP1339 Typical Application Circuit (without IFF pin)

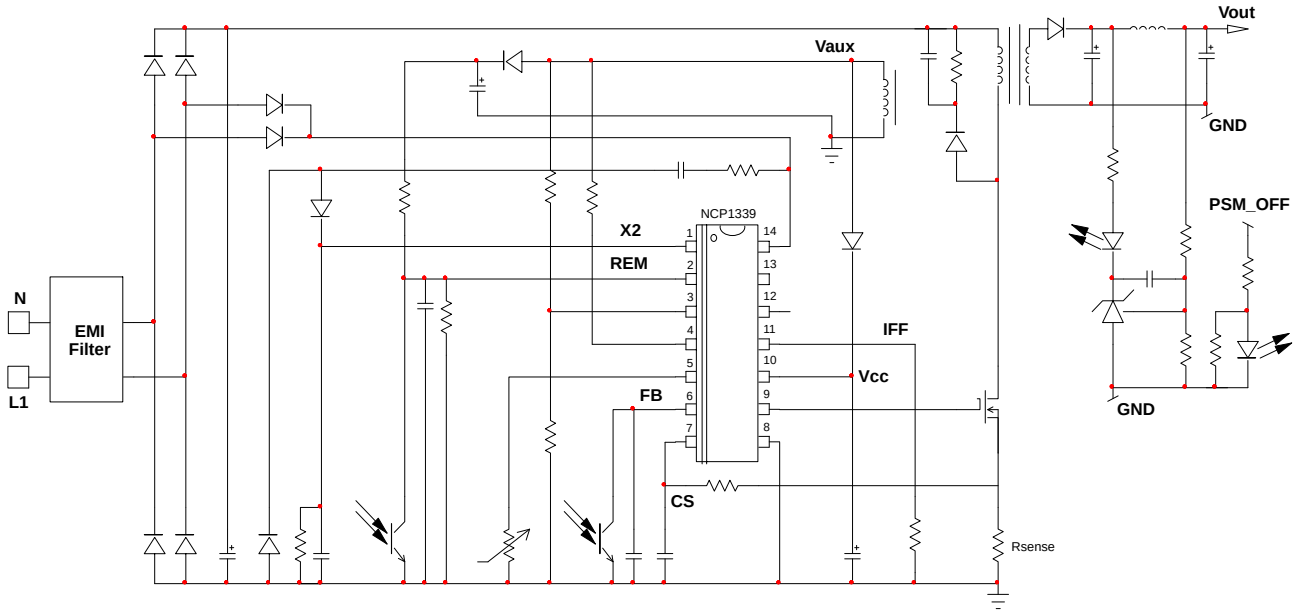


Figure 2. NCP1339 Typical Application Circuit (with IFF pin)

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Function
1	X2	When the voltage on this pin disappears, the controller ensures the X2−capacitors discharge.
2	REM	The part operates when the REM pin is forced lower than a certain level and enters the Power Savings Mode (PSM) otherwise.
3	OPP	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level.
4	ZCD	Input to the demagnetization detection comparator for the QR Flyback controller.
5	Fault	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor. Fault detection triggers a latch.
6	FB	Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler.
7	CS	Input to the cycle−by−cycle current limit comparator for the QR Flyback section.
8	GND	Ground reference.
9	DRV	This is the drive pin of the circuit. The DRV high−current capability (−0.5 /+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
10	VCC	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 15 V and turns off when V_{CC} goes below 9 V (typical values). After start−up, the operating range is 10 V up to 28 V. An OVP comparator monitors this pin and offers a means to latch the converter in fault conditions.
11	NC or IFF	The external resistor connected to this pin adjusts the frozen peak current during frequency foldback mode and the power gap between different valley lockouts.
12	NC	
13		Removed for creepage distance.
14	HV	This pin provides a charging current during start−up and auto−recovery faults but also a means to efficiently discharge the input X2 capacitors.

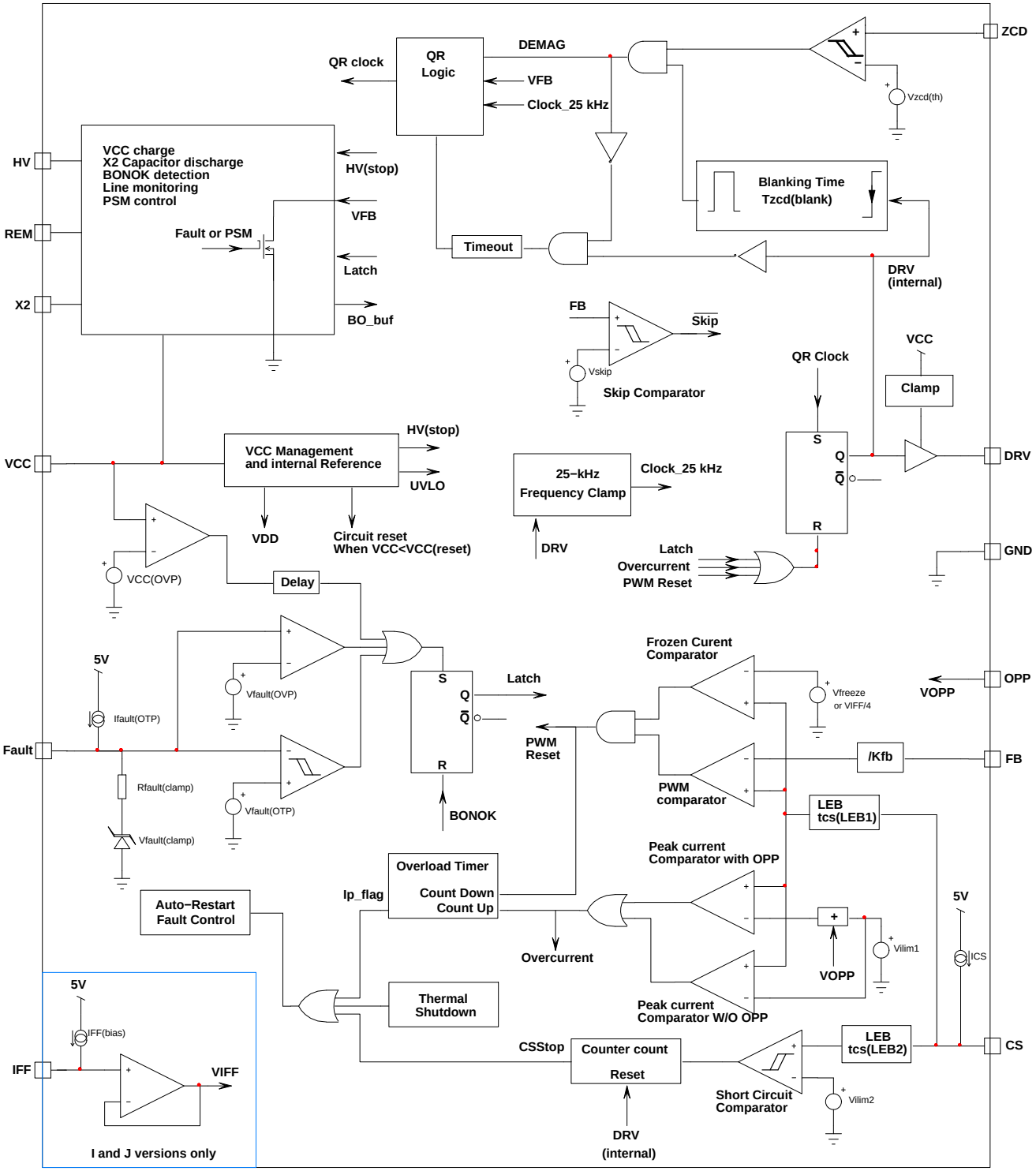


Figure 3. NCP1339 Functional Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage	V_{HV}	−0.3 to 500	V
High Voltage Startup Circuit Input Current	I_{HV}	20	mA
Supply Input Voltage	$V_{CC(MAX)}$	−0.3 to 30	V
Supply Input Current	$I_{CC(MAX)}$	30	mA
Supply Input Voltage Slew Rate	dV_{CC}/dt	1	V/μs
Fault and IFF Input Voltage	V_{i1}	−0.3 to (V_{CC} + 1)	V
Fault and IFF Input Current	I_{i1}	10	mA
REM and X2 Input Voltage	V_{i2}	−0.3 to 10	V
REM and X2 Input Current	I_{i2}	10	mA
Zero Current Detection and OPP Input Voltage	V_{ZCD}	−0.3 to (V_{CC} + 1)	V
Zero Current Detection and OPP Input Current	I_{ZCD}	−2/+5	mA
Current Sense Input Voltage	V_{CS}	−0.3 to 5	V
Current Sense Input Current	I_{CS}	10	mA
Feedback Input Voltage	V_{FB}	−0.3 to 9	V
Feedback Input Current	I_{FB}	10	mA
Driver Maximum Voltage (Note 1)	V_{DRV}	−0.3 to $V_{DRV(high)}$	V
Driver Maximum Current	$I_{DRV(SRC)}$ $I_{DRV(SNK)}$	500 800	mA
Operating Junction Temperature	T_J	−40 to 125	°C
Maxim Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature Range	T_{STG}	–60 to 150	°C
Thermal Resistance, Junction to Ambient 2 Oz Cu Printed Circuit Copper Clad With a 100 mm^2 copper heat spreader area	$R_{\theta JA}$	132	°C/W
ESD Capability Human Body Model per JEDEC Standard JESD22−A114F (All pins except HV) Human Body Model per JEDEC Standard JESD22−A114F (HV Pin) Machine Model per JEDEC Standard JESD22−A115C Charge Device Model per JEDEC Standard JESD22−C101E Latch−Up Protection per JEDEC Standard JESD78		 2000 1000 200 500 ±100	 V V V V mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 3 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF , C_{DRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage Startup Threshold Minimum Operating Voltage Operating Hysteresis Transition from I_{start1} to I_{start2}	dV/dt = 0.1 V/ms V_{CC} increasing V_{CC} decreasing $V_{CC(on)} - V_{CC(off)}$ V_{CC} increasing, I_{HV} = 650 μA	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(inhibit)}$	 14.0 8.0 5.6 0.55	 15.0 9.0 – 1.00	 16.0 10.0 – 1.20	V
Blanking Duration After $V_{CC(off)}$	V_{CC} above $V_{CC(reset)}$	$t_{UVLO(blank)}$	2	–	15	μs
Startup Delay	Delay from $V_{CC(on)}$ to QR Enable	$t_{delay(start)}$	–	–	725	μs
Minimum voltage for current source operation		VHV_{min}	–	30	60	V
Current flowing out of V_{cc}	V_{cc} = 0 V	IC1	−0.8	−0.5	−0.3	mA
Current flowing out of V_{cc} pin	V_{cc} = $V_{cc(on)}$ – 0.5 V	IC2	−15	−10	−6	mA
Off−state leakage current	V_{HV} = 500 V, V_{cc} = 15 V, V_{REM} = 0 V	I_{leak1}	–	–	25.5	μA
HV pin leakage current when PSM is active	V_{HV} = 141 V	I_{leak2}	–	–	11	μA
HV pin leakage current when PSM is active	V_{HV} = 325 V	I_{leak3}	–	–	18	μA
V_{cc} level during a fault		$V_{CC(bias)}$	4.7	5.5	6.3	V
Supply Current Before Startup, Fault or Latch Flyback in Skip switching at 70 kHz	 V_{CC} = $V_{CC(on)}$ – 0.5 V V_{FB} = 0.35 V C_{DRV} open	 I_{CC2} I_{CC3}	 0.05 0.2 1.0	 0.10 0.68 1.6	 0.54 1.0 3.0	mA
V_{CC} Overvoltage Protection Threshold		$V_{CC(OVP)}$	27	28	29.5	V
V_{CC} Overvoltage Protection Delay		$t_{delay(VCC\_OVP)}$	22.5	30.0	37.5	μs
INPUT FILTER DISCHARGE						
X2 timer disable switch threshold voltage		V_{th_X2}	1.0	1.5	2.0	V
Hysteresis on the X2 pin		$V_{th\_X2\_hyst}$	–	150	–	mV
X2 input clamp voltage		$V_{\_X2\_clamp}$	–	4	–	V
X2 timer duration		X2_timer	50	–	170	ms
X2 input leakage current	V_{X2} = 2.5 V	$I_{\_X2\_leak}$	–	–	0.3	μA
Maximum discharge switch current	V_{CC} = 10V	$I_{\_X2\_dis}$	7	10	14	mA
REMOTE INPUT – POWER SAVINGS MODE						
Remote pin voltage below which PSM is deactivated	V_{REM} increasing	V_REM_on	1	1.5	2	V
Remote pin voltage above which PSM is activated	V_{REM} decreasing	V_REM_off	7.2	8	8.8	V
Remote input leakage current	V_REM = 10 V	I_REM_leak	–	20	1000	nA
Remote timer duration		REM_timer	50	–	170	ms
Resistance of the Remote Pin Internal pull−down Switch		R_SW_REM	1000	–	3000	Ω
BROWN OUT DETECTION						
Brown−Out Start Level	HV pin voltage increasing	$V_{BO(start)}$	90	101	110	V
System Shutdown Threshold	HV pin voltage decreasing	$V_{BO(stop)}$	84	93	104	V
Brown−out Detection Blanking Time	V_{HV} decreasing, delay from $V_{BO(stop)}$ to drive disable	$t_{BO(stop)}$	30	–	100	ms
GATE DRIVE						
Rise Time (10−90%)	V_{DRV} from 10 to 90%	$t_{DRV(rise)}$	–	40	80	ns

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 3 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF , C_{DRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
GATE DRIVE						
Fall Time (90−10%)	90 to 10% of V_{DRV}	$t_{DRV(fall)}$	–	20	–	ns
Current Capability Source Sink	 V_{DRV} = 2 V V_{DRV} = 10 V	 $I_{DRV(SRC)}$ $I_{DRV(SNK)}$	 – –	 500 800	 – –	mA
High State Voltage	V_{CC} = $V_{CC(off)}$ + 0.2 V, R_{DRV} = 10 kΩ V_{CC} = 26 V, R_{DRV} = 10 kΩ	$V_{DRV(high1)}$ $V_{DRV(high2)}$	8 10	– 12	– 14	V
Low Stage Voltage	V_{Fault} = 4 V	$V_{DRV(low)}$	–	–	0.25	V
FEEDBACK						
Feedback Input Open Voltage		$V_{FB(open)}$	4.48	4.7	5.0	V
V_{FB} to Internal Current Setpoint Division Ratio		K_{FB}	3.8	4.0	4.2	–
FB Pull Up Resistor	V_{FB} = 0.4 V	R_{FB}	17	20	23	kΩ
Valley Thresholds Transition from 1st to 2nd valley Transition from 2nd to 3rd valley Transition from 3rd to 4th valley Transition from 4th to 5th valley Transition from 5th to 6th valley Transition from 6th to FF Transition from FF to 6th valley Transition from 6th to 5th valley Transition from 5th to 4th valley Transition from 4th to 3rd valley Transition from 3rd to 2nd valley Transition from 2nd to 1st valley	 V_{FB} decreasing, V_{IFF} = 0.8 V V_{FB} decreasing, V_{IFF} = 0.8 V V_{FB} decreasing, V_{IFF} = 0.8 V V_{FB} decreasing, V_{IFF} = 0.8 V V_{FB} decreasing, V_{IFF} = 0.8 V V_{FB} decreasing, V_{IFF} = 0.8 V V_{FB} increasing, V_{IFF} = 0.8 V V_{FB} increasing, V_{IFF} = 0.8 V V_{FB} increasing, V_{IFF} = 0.8 V V_{FB} increasing, V_{IFF} = 0.8 V V_{FB} increasing, V_{IFF} = 0.8 V V_{FB} increasing, V_{IFF} = 0.8 V	 V_{H2D} V_{H3D} V_{H4D} V_{H5D} V_{H6D} V_{HVCOD} V_{HVCOI} V_{H6I} V_{H5I} V_{H4I} V_{H3I} V_{H2I}	 1.316 1.128 1.034 0.940 0.846 0.760 0.900 1.410 1.504 1.598 1.692 1.880	 1.400 1.200 1.100 1.000 0.900 0.800 1.000 1.500 1.600 1.700 1.800 2.000	 1.484 1.272 1.166 1.060 0.954 0.830 1.060 1.590 1.696 1.802 1.908 2.120	V
Maximum On Time		$t_{on(MAX)}$	27	32	40	µs
DEMAGNETIZATION INPUT						
ZCD threshold voltage	V_{ZCD} decreasing	$V_{ZCD(th)}$	35	55	90	mV
ZCD hysteresis	V_{ZCD} increasing	$V_{ZCD(HYS)}$	15	35	55	mV
Demagnetization Propagation Delay	V_{ZCD} step from 4.0 V to −0.3 V	t_{DEM}	–	150	250	ns
Input Voltage Excursion Upper Clamp Negative Clamp	 I_{QZCD} = 5.0 mA I_{QZCD} = −2.0 mA	 $V_{ZCD(MAX)}$ $V_{ZCD(MIN)}$	 12.4 −0.9	 12.7 −0.7	 13 0	V
Blanking Delay After Turn−Off	(C, D and E versions) (F, G, H, I and J versions)	$t_{ZCD(blank)}$	2 0.5	3 0.7	4 0.9	µs
Timeout After Last Demagnetization Detection	Timeout while in soft−start Timeout after soft−start complete	$t_{(out1)}$ $t_{(out2)}$	80 5.1	100 6	120 6.9	µs
CURRENT SENSE						
Current Sense Voltage Threshold (V_{ILIM1})	V_{CS} increasing V_{CS} increasing, V_{OPP} = 1 V	V_{ILIM1a} V_{ILIM1b}	0.760 0.760	0.800 0.800	0.840 0.840	V
Cycle by Cycle Leading Edge Blanking Duration	Minimum on time minus $t_{CS(delay1)}$	$t_{CS(LEB1)}$	220	275	330	ns
Cycle by Cycle Current Sense Propagation Delay	V_{CS} dv/dt = 1 V/µs, measured from V_{ILIM1} to DRV falling edge	$t_{CS(delay1)}$	–	125	175	ns
Internal peak current setpoint freeze	V_{IFF} = 0.8 V	V_{freeze}	−	200	−	mV
I_{FF} pin current source	V_{IFF} = 0.8 V (I and J versions)	$I_{FF(bias)}$	−110	−100	−85	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 3 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF , C_{DRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Abnormal Overcurrent Fault Threshold	V_{CS} increasing, V_{FB} = 4 V	V_{ILIM2}	1.125	1.200	1.275	V
Abnormal Overcurrent Fault Blanking Duration	Step V_{CS} 0 V to V_{ILIM2} + 0.5 V to DRV falling edge, dV/dt = 10 V/μs	$t_{CS(LEB2)}$	90	120	150	ns
Abnormal Overcurrent Fault Propagation Delay	Step V_{CS} 0 V to V_{ILIM2} + 0.5 V to DRV falling edge, dV/dt = 10 V/μs	$t_{CS(delay2)}$	–	125	175	ns
Set point decrease for V_{OPP} = − 250 mV	V_{CS} Increasing, V_{FB} = 4 V	$V_{OPP(MAX)}$	27	31.25	33	%
Overpower Protection Delay	V_{CS} dv/dt = 1 V/μs, measured from $V_{OPP(MAX)}$ to DRV falling edge	$t_{OPP(delay)}$	–	125	175	ns
Overpower Signal Blanking Delay		$t_{OPP(blank)}$	100	120	200	ns
Pull−up Current Source	V_{CS} = 1.5 V	I_{CS}	−1.5	1.0	−0.5	μA
JITTERING (For E, F, G, I and J versions only)						
Frequency of the Jittering CS Pin Source Current	CS pin being grounded)	F_{jit}	1.0	1.3	1.6	kHz
Amplitude of the CS Source Current	CS pin being grounded	I_{jit}	85	100	110	μA
HV Pin Voltage for jittering activation	HV pin voltage rising	$(V_{in,jit})_H$	210	250	290	V
HV Pin Voltage below which the jittering Timer activated	HV pin voltage falling	$(V_{in,jit})_L$	185	220	255	V
Blanking Time before Jittering disabling	V_{HV} < 184 V	$T_{jit(blank)}$	25	40	55	ms
FAULT PROTECTION						
Soft−Start Period (Done digitally with 63 steps)	Measured from 1st DRV pulse to V_{CS} = V_{ILIM1}	t_{SSTART}	2.8	4.0	5.0	ms
Flyback Overload Fault Timer	V_{CS} = V_{ILIM1}	t_{OVLD}	120	160	200	ms
Overvoltage Protection (OVP) Threshold	V_{Fault} increasing	$V_{Fault(OVP)}$	2.79	3.00	3.23	V
Delay Before Fault Confirmation Used for OVP Detection Used for OTP Detection	 V_{Fault} increasing V_{Fault} decreasing	 $t_{delay(Fault\_OVP)}$ $t_{delay(Fault\_OTP)}$	 20 20	 27.5 27.5	 35 35	μs
Overtemperature Protection (OTP) Threshold (Note 2)	V_{Fault} decreasing	$V_{Fault(OTP\_in)}$	0.395	0.40	0.435	V
OTP Pull−up Current Source (Note 2)	V_{Fault} = $V_{Fault(OTP\_in)}$ + 0.2 V T_J = 110 °C	 $I_{Fault(OTP)}$ $I_{Fault(OTP\_110)}$	 42.5 –	 45.5 45.5	 48.5 –	μA
Fault Input Clamp Voltage	V_{Fault} = open	$V_{Fault(clamp)}$	1.15	1.7	2.25	V
Fault Input Clamp Series Resistor		$R_{Fault(clamp)}$	1.32	1.55	1.78	kΩ
Auto−recovery Timer		T_{A-rec_timer}	1.1	2		s
STAND−BY MANAGEMENT						
Frequency clamp Threshold		F_{Clamp}	23.5	25	27.5	kHz
Skip Threshold	V_{FB} decreasing	V_{SKIP}	0.35	0.40	0.45	V
Skip Hysteresis	V_{FB} increasing	$V_{SKIP(HYS)}$	35	60	85	mV
THERMAL PROTECTION						
Thermal Shutdown	(Note 3)	T_{SHDN}	140	150	170	°C
Thermal Shutdown Hysteresis	(Note 3)	$T_{SHDN(HYS)}$	20	40	60	°C
Thermal Shutdown Delay	(Note 3)	$t_{delay(TSHDN)}$	−	30.0	−	μs

2. NTC with R_{110} = 8.8 kΩ (TTC03−474).
3. The value is not subjected to production test − verified by design/characterization.

TYPICAL CHARACTERISTICS

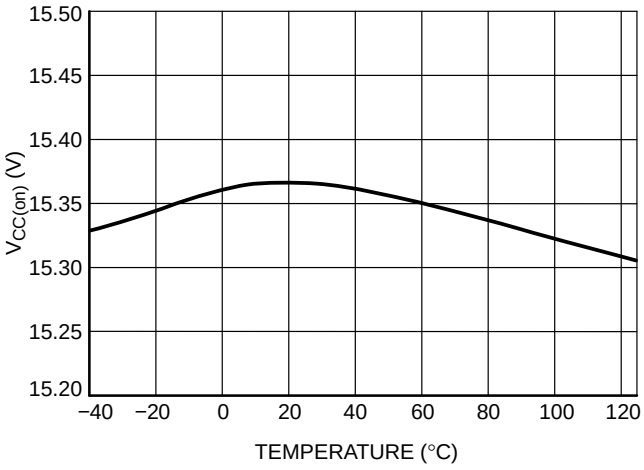


Figure 4. $V_{CC(on)}$ vs. Junction Temperature

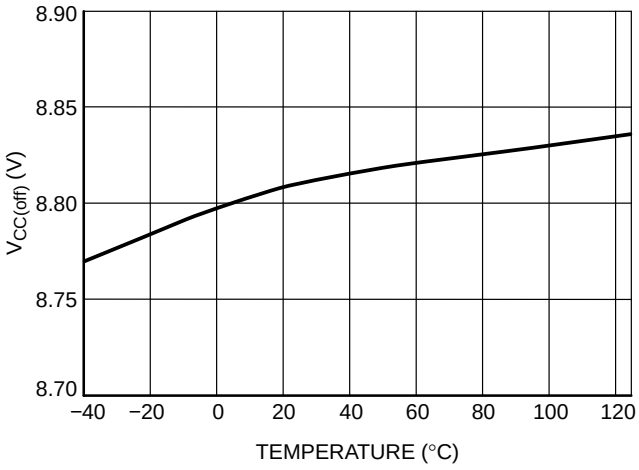


Figure 5. $V_{CC(off)}$ vs. Junction Temperature

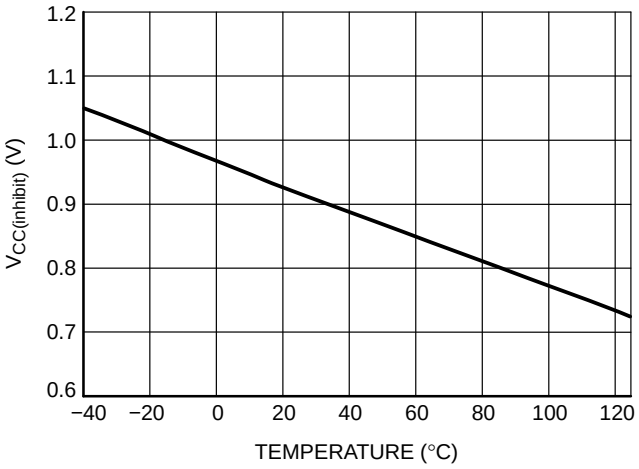


Figure 6. $V_{CC(inhibit)}$ vs. Junction Temperature

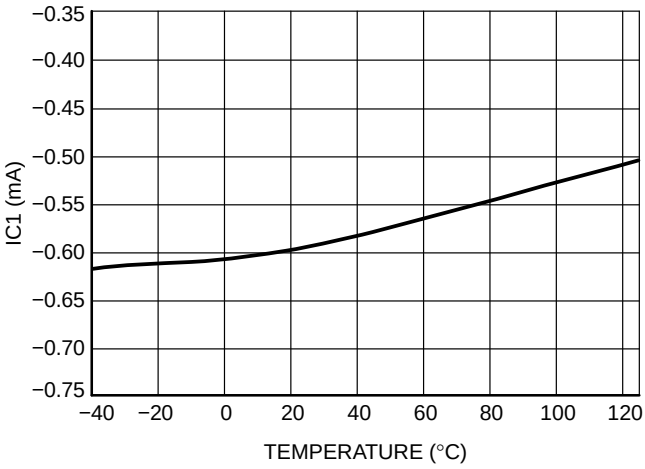


Figure 7. IC1 vs. Junction Temperature

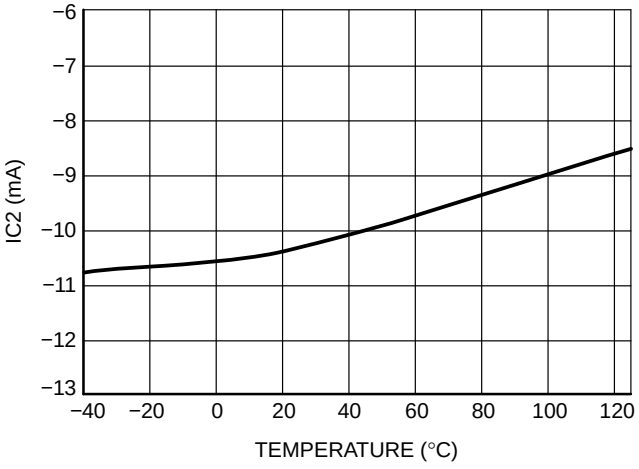


Figure 8. IC2 vs. Junction Temperature

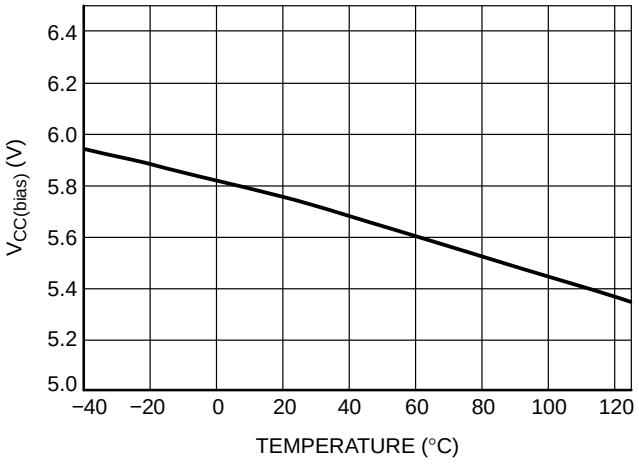


Figure 9. $V_{CC(bias)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

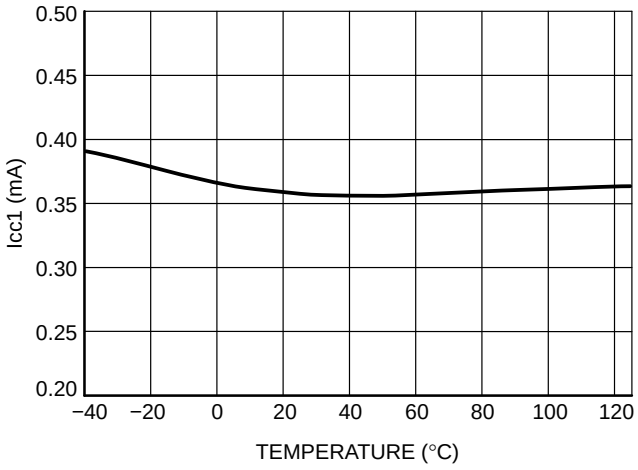


Figure 10. ICC1 vs. Junction Temperature

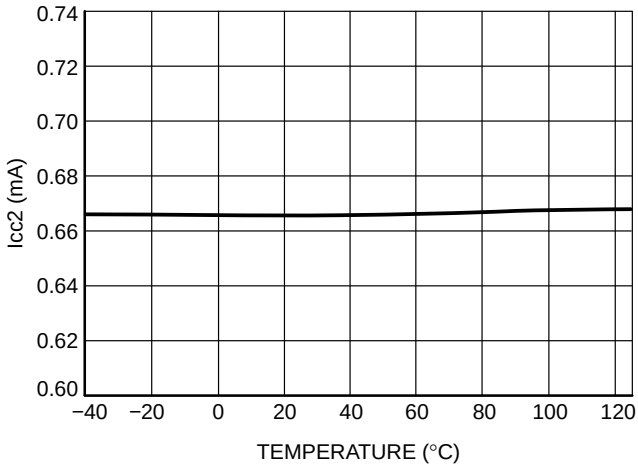


Figure 11. ICC2 vs. Junction Temperature

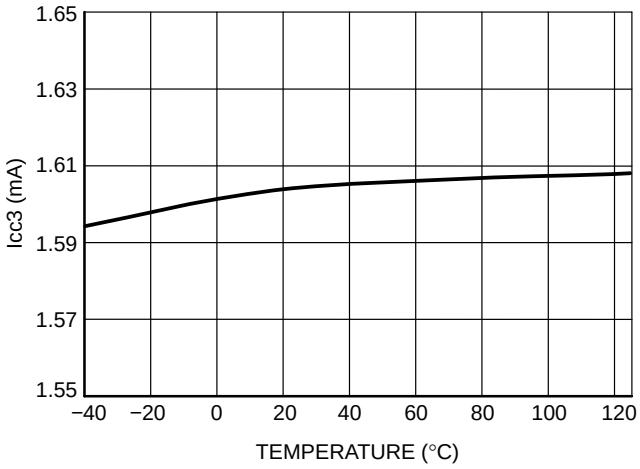


Figure 12. ICC3 vs. Junction Temperature

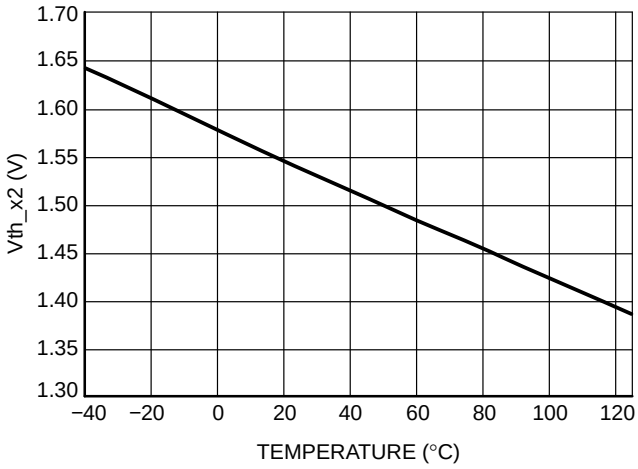


Figure 13. V_{th_x2} vs. Junction Temperature

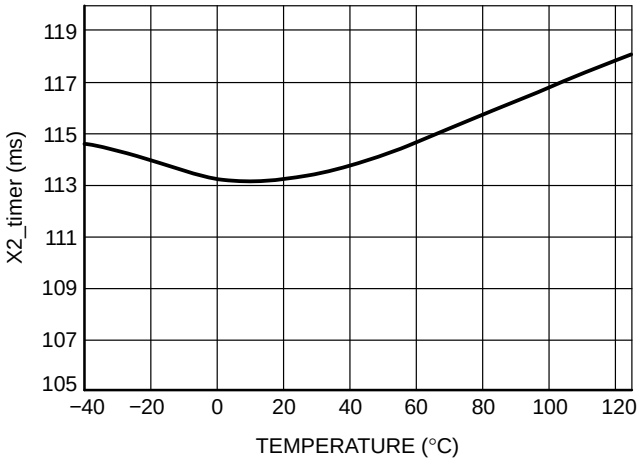


Figure 14. X2_timer vs. Junction Temperature

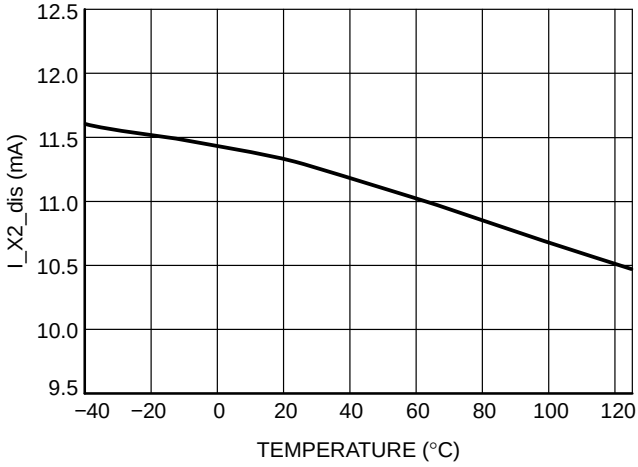


Figure 15. T_{LEB} vs. Junction Temperature

TYPICAL CHARACTERISTICS

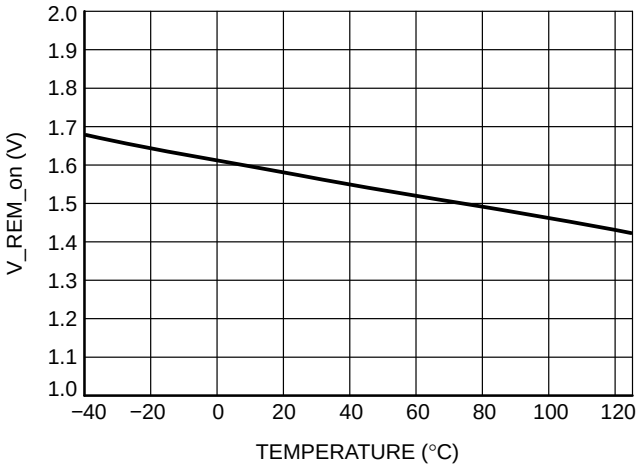


Figure 16. V_REM_on vs. Junction Temperature

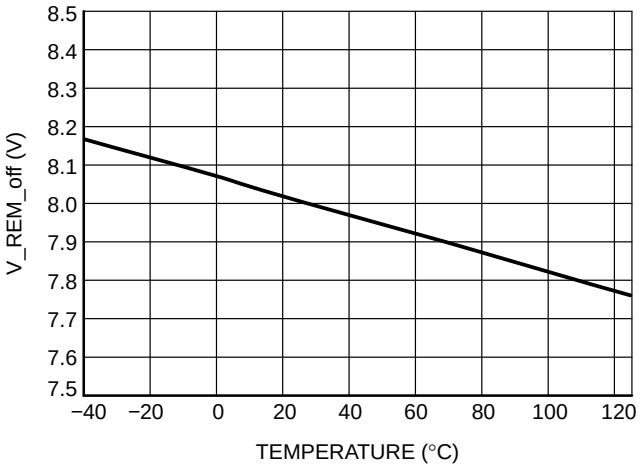


Figure 17. V_REM_off vs. Junction Temperature

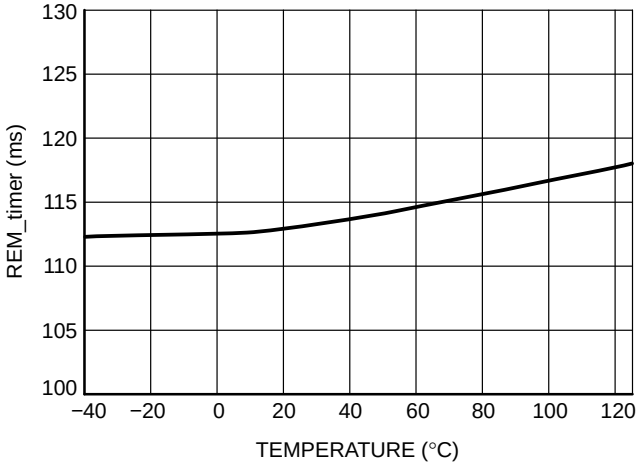


Figure 18. REM_timer vs. Junction Temperature

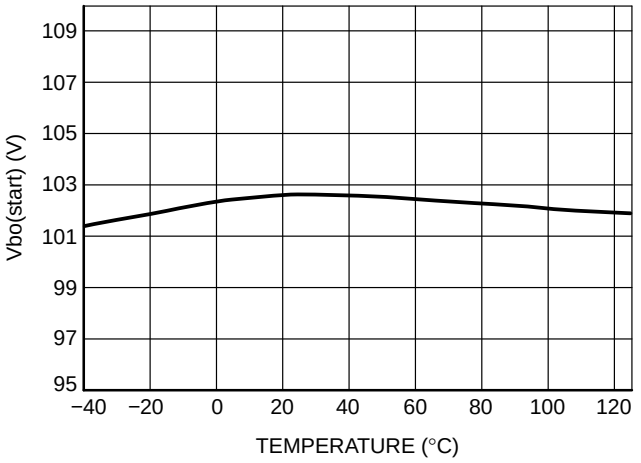


Figure 19. $V_{BO(start)}$ vs. Junction Temperature

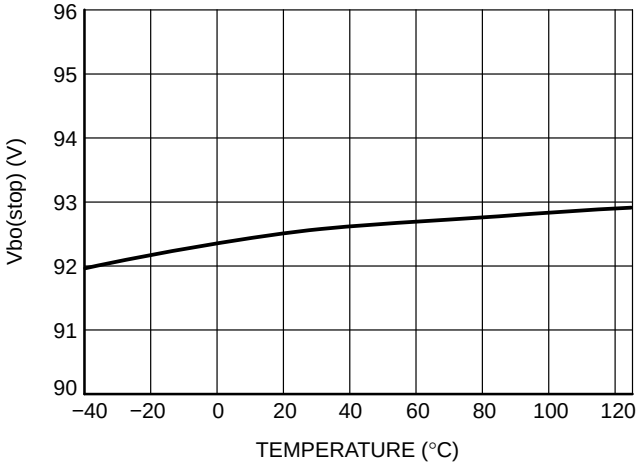


Figure 20. $V_{BO(stop)}$ vs. Junction Temperature

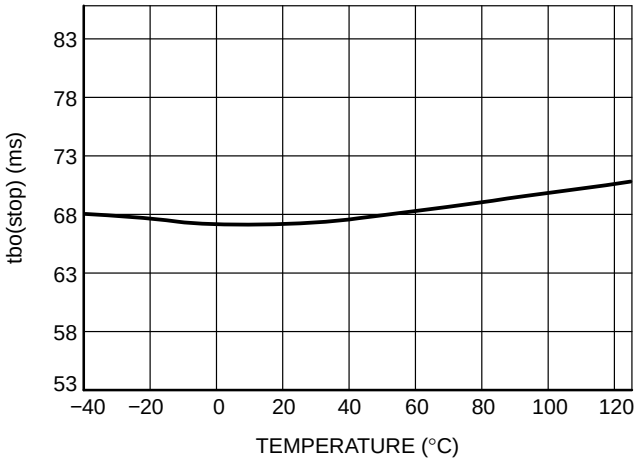


Figure 21. $t_{BO(stop)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

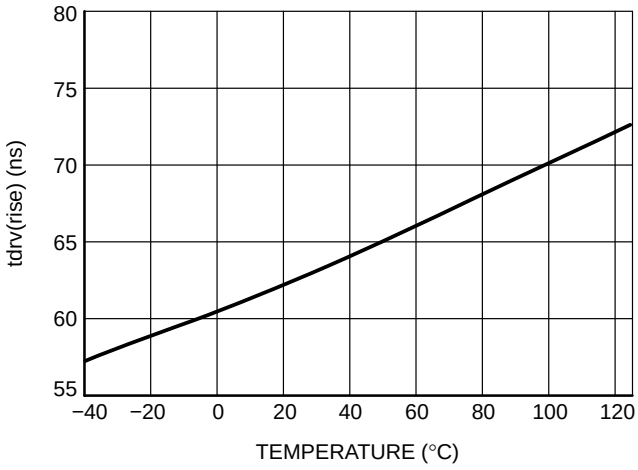


Figure 22. $t_{DRV(rise)}$ vs. Junction Temperature

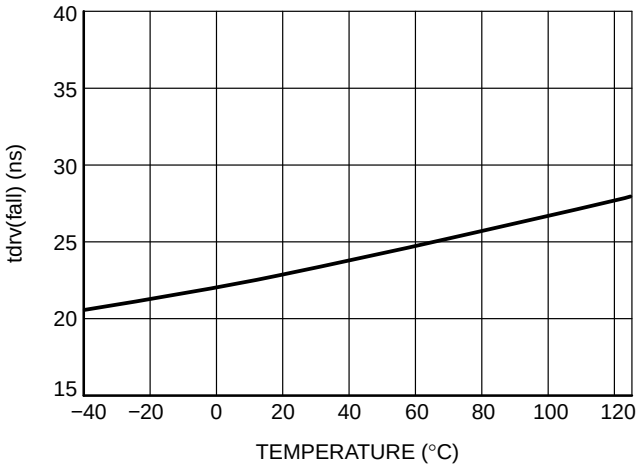


Figure 23. $t_{DRV(fall)}$ vs. Junction Temperature

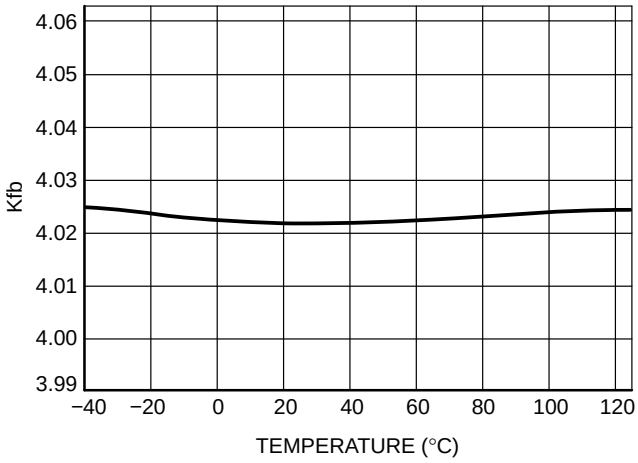


Figure 24. K_{FB} vs. Junction Temperature

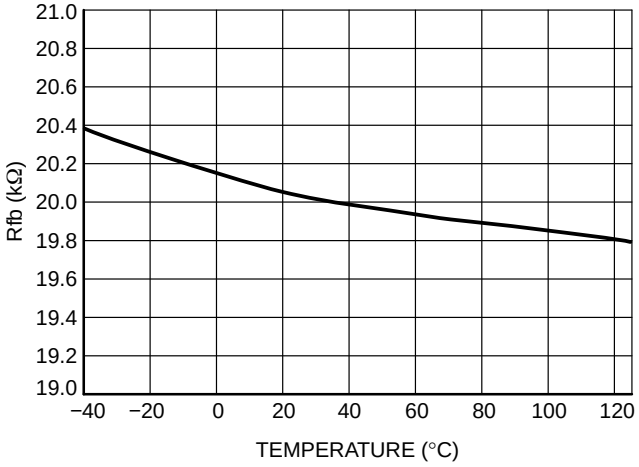


Figure 25. R_{FB} vs. Junction Temperature

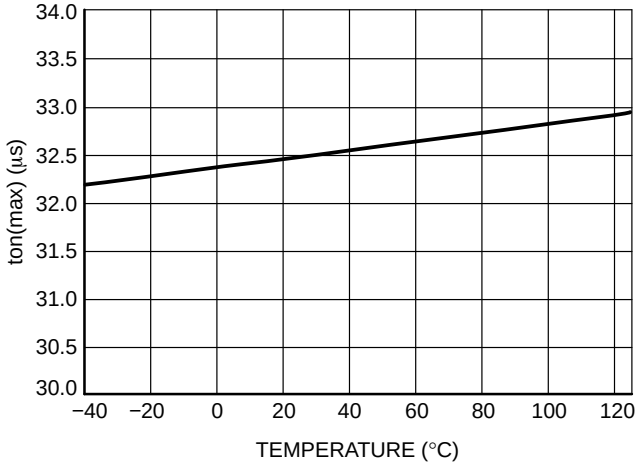


Figure 26. $t_{on(MAX)}$ vs. Junction Temperature

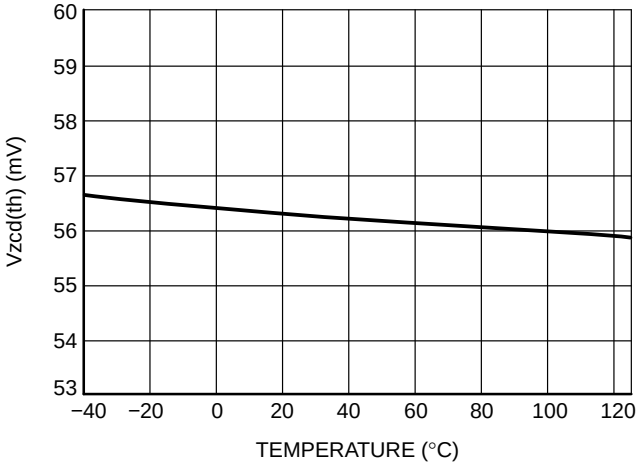


Figure 27. $V_{ZCD(th)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

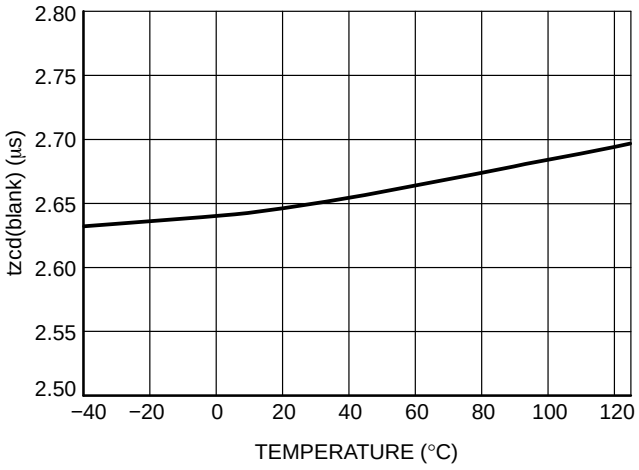


Figure 28. $t_{ZCD(blank)}$ vs. Junction Temperature

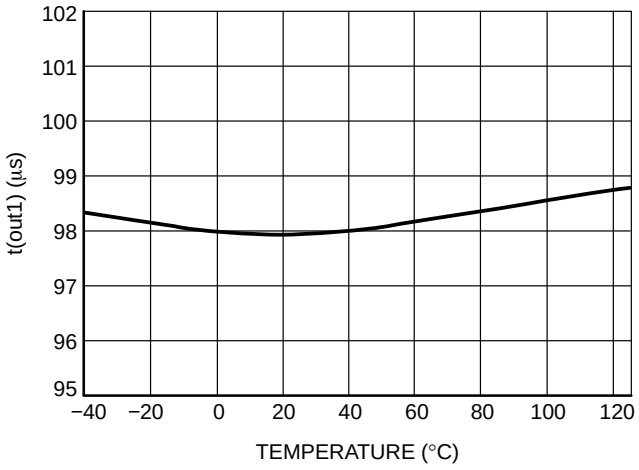


Figure 29. $t_{(out1)}$ vs. Junction Temperature

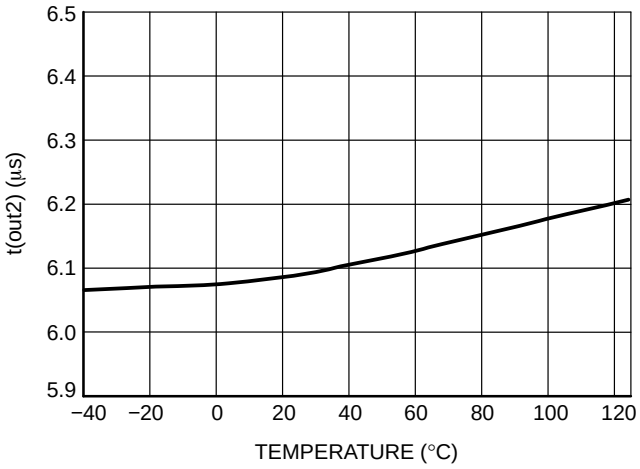


Figure 30. $t_{(out2)}$ vs. Junction Temperature

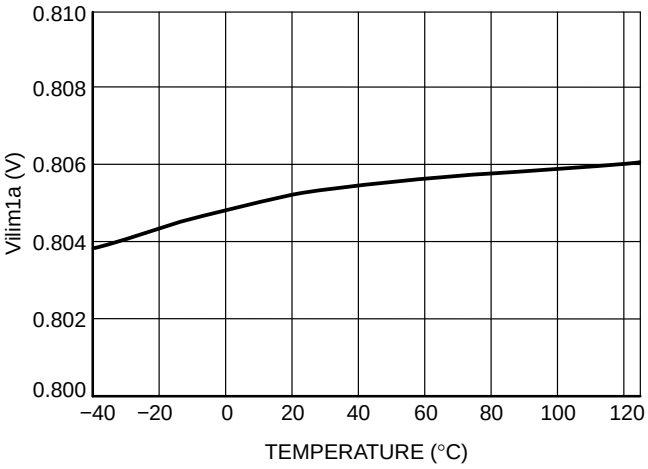


Figure 31. V_{ilim1a} vs. Junction Temperature

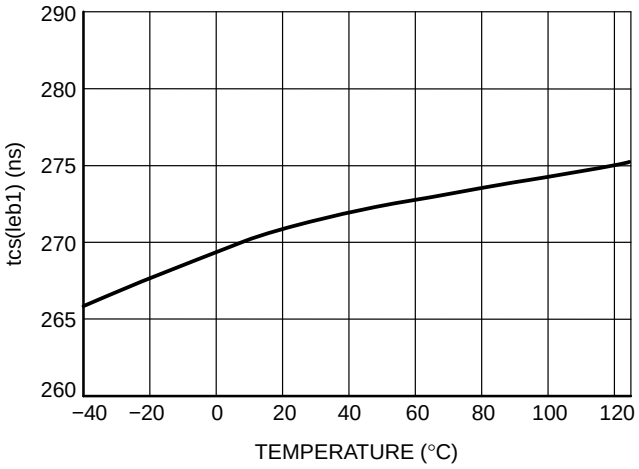


Figure 32. $t_{CS(LEB1)}$ vs. Junction Temperature

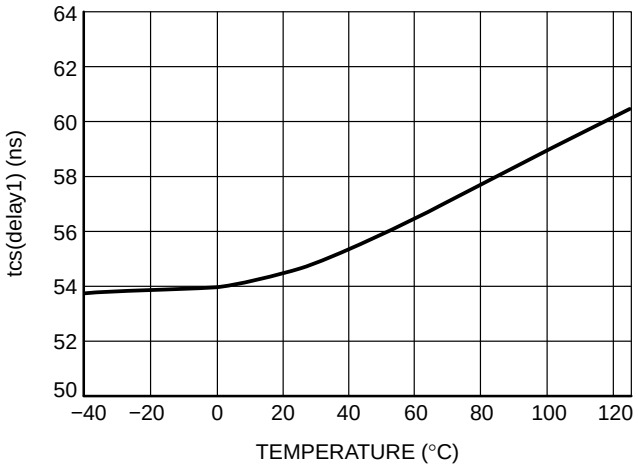


Figure 33. $t_{CS(delay1)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

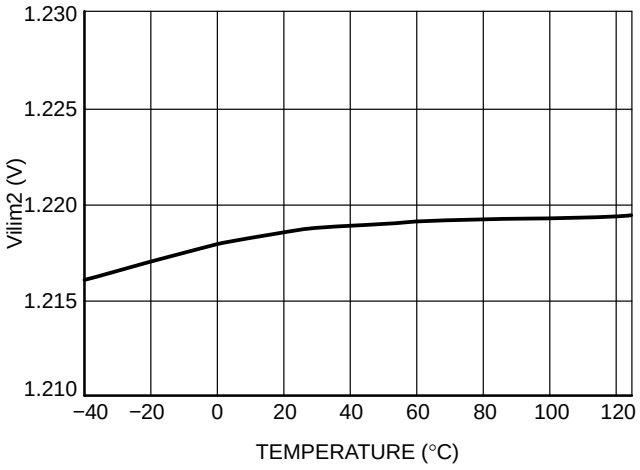


Figure 34. V_{ilim2} vs. Junction Temperature

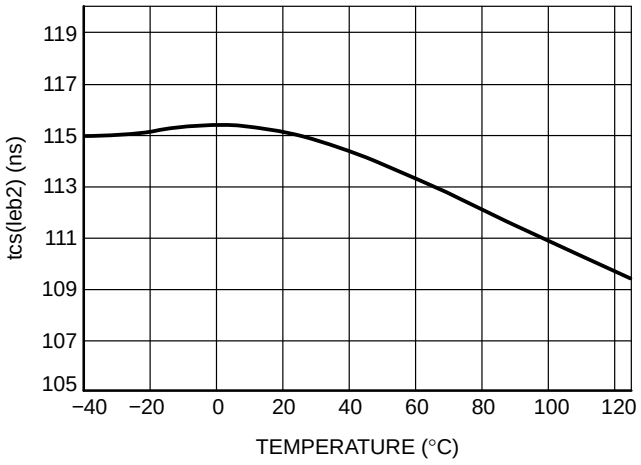


Figure 35. $t_{CS(LEB2)}$ vs. Junction Temperature

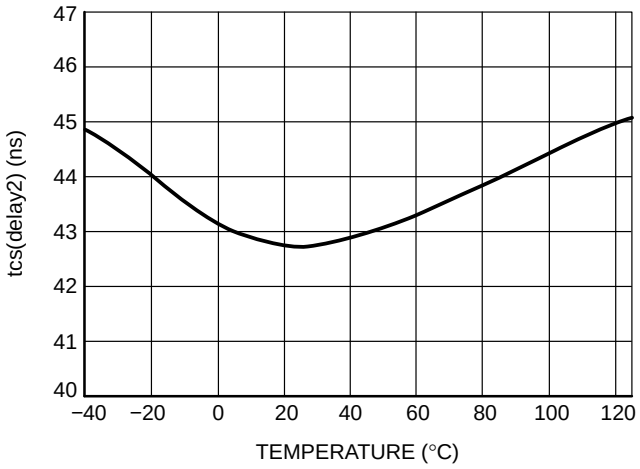


Figure 36. $t_{CS(delay2)}$ vs. Junction Temperature

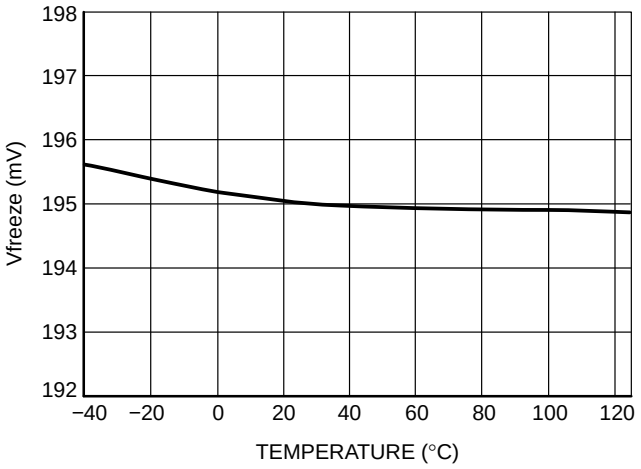


Figure 37. V_{freeze} vs. Junction Temperature

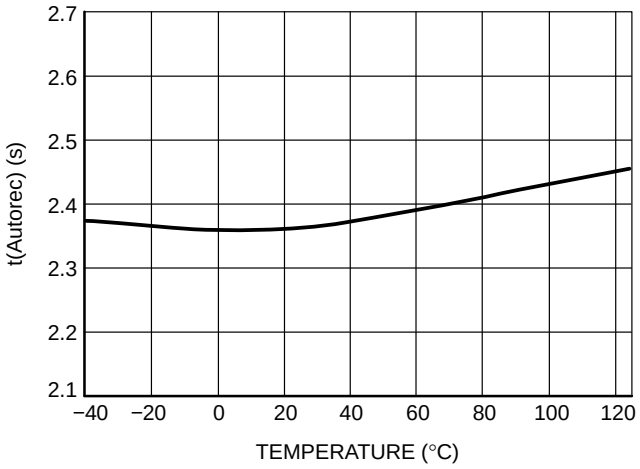


Figure 38. T_{A-rec_timer} vs. Junction Temperature

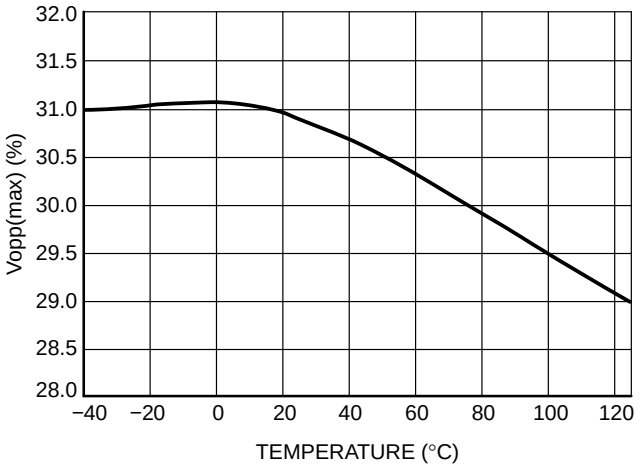


Figure 39. $V_{OPP(MAX)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

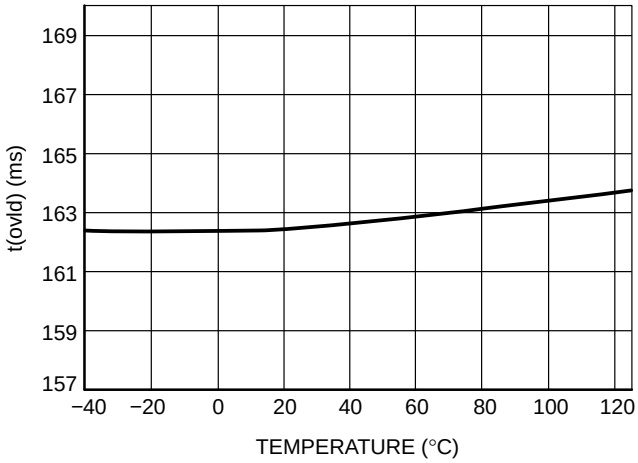


Figure 40. t_{OVLD} vs. Junction Temperature

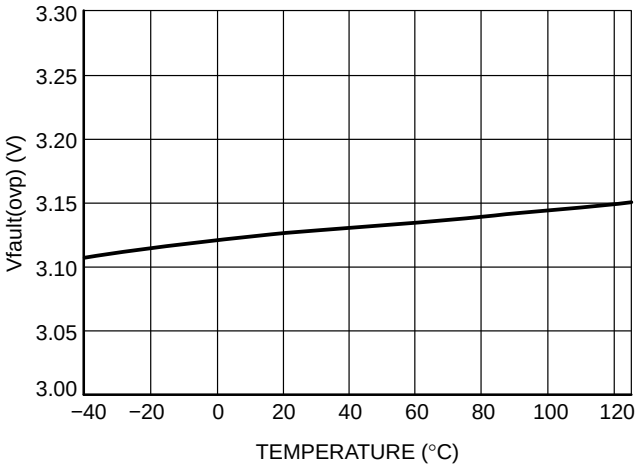


Figure 41. $V_{fault(OVP)}$ vs. Junction Temperature

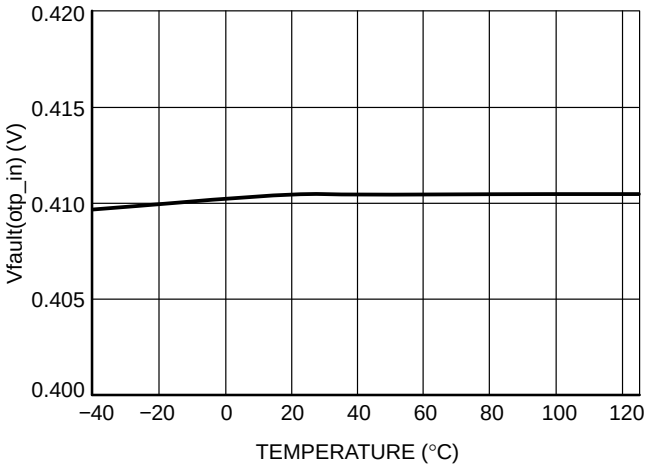


Figure 42. $V_{Fault(OTP\_in)}$ vs. Junction Temperature

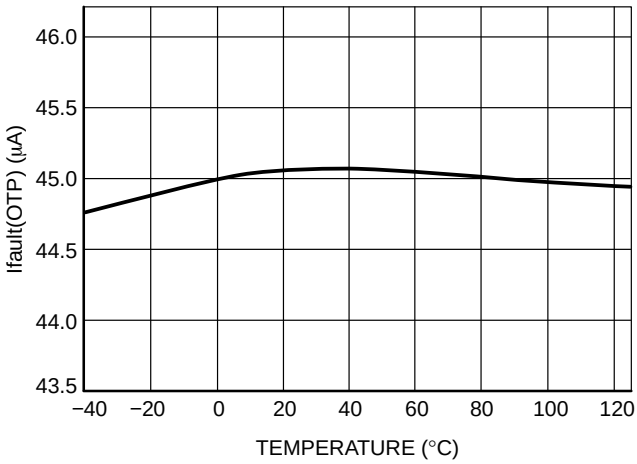


Figure 43. $I_{Fault(OTP)}$ vs. Junction Temperature

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1339 implements a standard quasi−resonant current−mode architecture. This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. The NCP1339 brings all the necessary components normally needed in modern power supply designs, bringing several enhancements such as non−dissipative OPP, brown−out protection or sophisticated frequency reduction management for an optimized efficiency over the power range. Accounting for the new needs of extremely low standby power requirements, the part includes an automatic X2−capacitor discharge circuitry which can save the power−consuming resistors otherwise needed across the front−end filtering capacitors. The controller is also able to enter Power Savings Mode (PSM) that is, a deep sleep mode via its dedicated remote (“REM”) pin.

- High−Voltage start−up: low standby power results cannot be obtained with the classical resistive start−up network. In this part, a high−voltage current−source provides the necessary current at start−up and turns off afterwards.
- Internal Brown−Out protection: the bulk voltage is internally sensed via the high−voltage pin monitoring (pin 14). When V_{pin14} is too low, the part stops pulsing. No re−start attempt is made until V_{pin14} recovers its normal range. At that moment, the brown−out comparator sends a general reset to the controller (de−latch occurs) and authorizes to re−start.
- X2−capacitors discharge capability: per IEC−950 standard, the time constant of the front−end filter capacitors and their associated discharge resistors must be less than 1 s. This is to avoid electrical stress when users unplug the converter and inadvertently touch the power cord terminals. The circuitry for discharging the X2 capacitors can save the need for discharge resistors, helping to further save power.
- PSM control: a dedicated pin allows the IC to enter a deep sleep mode when the REM input pin is brought above a certain level. This option offers an efficient means to operate the adapter in a power savings mode and draw the least input power from the mains in this mode. When the REM is actively pulled down via a dedicated optocoupler, the adapter immediately re−starts. The component that controls PSM is then active in normal operation (active−ON) and OFF in PSM (wasting no energy).
- Quasi−resonant, current−mode operation: QR operation is an efficient mode where the MOSFET turns on when its drain−source is at the minimum (valley). However, at light load, the switching frequency tends to get high. The NCP1339 valley lock−out and frequency foldback technique eliminate this drawback so that the efficiency remains at the highest over the power range.
- Valley Lockout: a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback pin voltage (FB) and when it reaches a level of 1.4 V, the circuit enters a valley lockout mode where the circuit skips a valley. If FB further decreases, more valleys are skipped until 6th valley is reached.
- Frequency Fold−back: if FB continues declining and reaches 0.8 V, the current setpoint is frozen to V_{freeze} and the circuit regulates by modulating the switching frequency until it reaches 25 kHz (For C, D, E, F, G and H versions). For I and J versions, the current setpoint is frozen to (V_{IFF}/4) when FB falling and reaches the IFF voltage (V_{IFF}) set on the IFF pin.
- Skip cycle: to avoid acoustic noise, the circuit prevents the switching frequency from decaying below 25 kHz. Instead, the circuit contains the power delivery by entering skip cycle mode when the system would otherwise need to further lower the switching frequency below 25 kHz.
- Internal OPP (Over Power Protection): by routing a portion of the negative voltage present during the on−time on the auxiliary winding to the OPP pin (pin 3), the user has a simple and non−dissipative means to alter the maximum current setpoint as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs.
- Internal soft−start: a 4−ms soft−start precludes the main power switch from being stressed upon start−up. It is activated whenever a startup sequence occurs including autorecovery hiccup.
- Fault input: the NCP1339 includes a dedicated fault input (pin 5). It can be used to sense an overvoltage condition and latch off the controller by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. The controller is also disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP\_in)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault (by the means of an NTC).
- Short−circuit/Overload protection: short−circuit and especially overload protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8−V maximum peak current limit is activated (or less when OPP is used), an error flag is asserted and a 160−ms timer begins counting. When the timer has

elapsed, the fault is validated. An internal timer keeps the pulses off for 2 s typically which, associated to the 160−ms pulsing re−try period, ensures a duty−cycle in fault mode of 10%, independent from the line level. As soon as the fault disappears, the SMPS resumes operation. Please note that some versions (C, G, H and J) offer an auto−recovery mode as we just described, versions D, E, F and I do not and latch off in case of a short circuit.

- EMI jittering (Disabled for C and D versions): in high−line conditions, a low−frequency triangular current is sourced by the CS pin. The resistor placed between the CS pin and the current sense resistor adjusts the jittering amount that is applied to the power supply. This helps spreading out energy in conducted noise analysis. Jittering is disabled in frequency foldback mode and in low line conditions.

HV Current Source Pin

The NCP1339 HV circuitry provides three features:

- Start−up current source to charge the V_{CC} capacitor at start−up.
- Brown−out protection: when the HV pin voltage is below 93 V for the 50−ms blanking time, the NCP1339 stops operating and recovers when the HV pin voltage exceeds 101 V (typical values)
- X2 capacitor discharge: when circuit X2 pin detects that the power supply is no more powered, the start−up current source turns on to discharge the X2 capacitors.

Because of this last feature, ***it is firmly recommended to wire it according to* Figure 44 *sketch***. The HV pin is not connected to the bulk voltage but directly to the line terminals through diodes (D_1 and D_2 of Figure 44). It is further recommended to implement one or two 2.2−kΩ resistors to reduce the noise that can be picked−up by the HV pin.

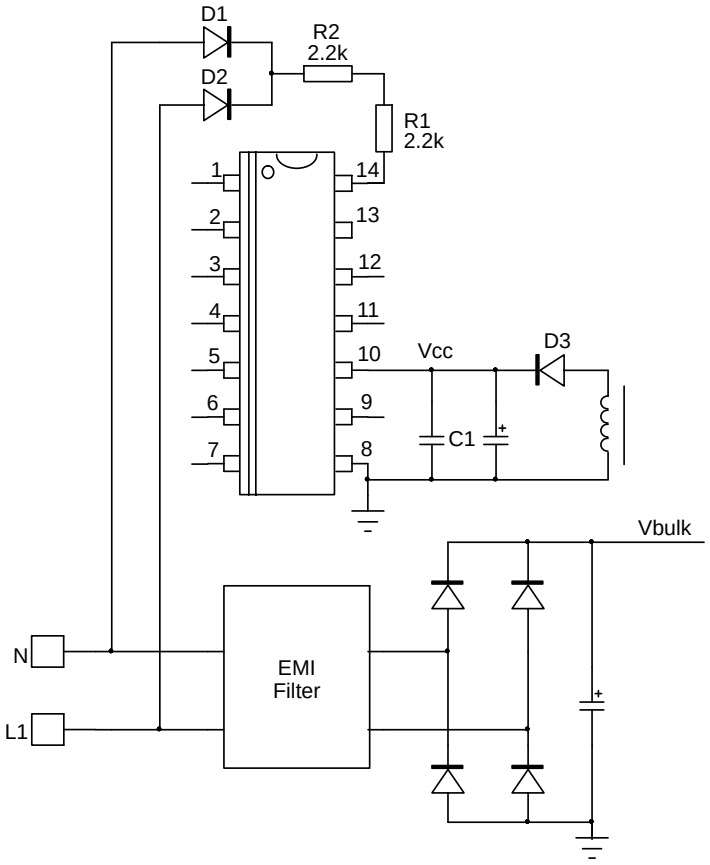


Figure 44. Two Diodes Route the Full−wave Rectified Mains to the HV Pin

Start−up Sequence:

The start−up time of a power supply largely depends on the time necessary to charge the V_{CC} capacitor to the controller V_{CC} start−up threshold ($V_{CC(on)}$ which is 15 V typically). The NCP1339 high−voltage current−source provides the necessary current for a prompt start−up and turns off afterwards. The delivered current (IC1) is reduced to less than 500 μA when the V_{CC} voltage is below $V_{CC(inhibit)}$ (1 V typically). This feature reduces the die stress if the V_{CC} pin happens to be accidentally grounded. When V_{CC} exceeds $V_{CC(inhibit)}$, a 10−mA current (IC2) is provided that charges the V_{CC} capacitor.

The V_{CC} charging time is then the total of the two following durations:

- Charge from 0 V to $V_{CC(inhibit)}$:

$$t_{start1} = \frac{V_{CC(inhibit)} C_{Vcc}}{IC1} \qquad \text{(eq. 1)}$$

- Charge from $V_{CC(inhibit)}$ to $V_{CC(on)}$:

$$t_{start2} = \frac{\left(V_{CC(on)} - V_{CC(inhibit)}\right)C_{Vcc}}{IC2} \quad \text{(eq. 2)}$$

Assuming a 100−μF V_{CC} capacitor is selected and replacing IC1, IC2, $V_{CC(inhibit)}$ and $V_{CC(on)}$ by their typical values, it comes:

$$t_{start1} = \frac{1\ V \times 100\ \mu F}{500\ \mu A} = 200\ ms \quad \text{(eq. 3)}$$

$$t_{start2} = \frac{(15 - 1) \times 100\ \mu F}{10\ mA} = 140\ ms$$

$$t_{start} = t_{start1} + t_{start2} = 340\ ms$$

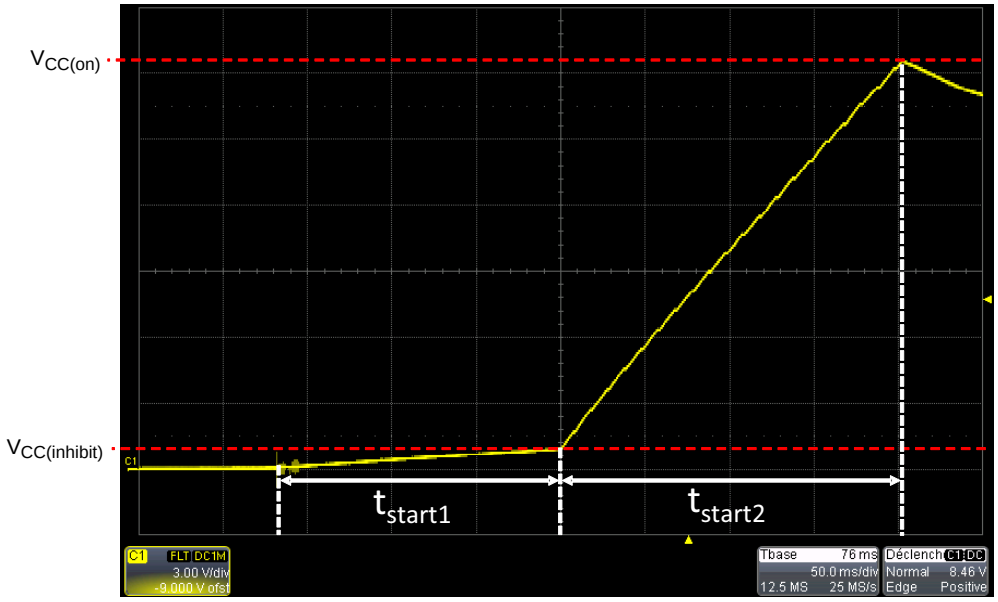


Figure 45. V_{cc} at Start−up is made of Two Segments given the Short−circuit Protection Implemented on the HV Source

If the V_{CC} capacitor is first dimensioned to supply the controller for the traditional 5 to 50 ms until the auxiliary winding takes over, no−load standby requirements usually cause it to be larger. The HV start−up current source is then a key feature since it allows keeping short start−up times with large V_{CC} capacitors (the total start−up sequence duration is often required to be less than 1 s).

Brown−out Circuitry

For the vast majority of controllers, input line sensing is performed via a resistive network monitoring the bulk voltage or the incoming ac signal. When in the quest of low standby power, the external network adds a consumption burden and deteriorates the standby power performance of the power supply. Owing to its proprietary high−voltage technology, ON Semiconductor now offers onboard line sensing without using an external sensing network. The brown−out thresholds are fixed (101 V line rising, 93 V falling, typically). Respectively correponding to about 72 V rms and 66 V rms, these levels are designed to fit most of standard ac−dc converter applications. The simplified internal schematic appears in Figure 46 while typical operating waveforms are drawn in Figure 47.

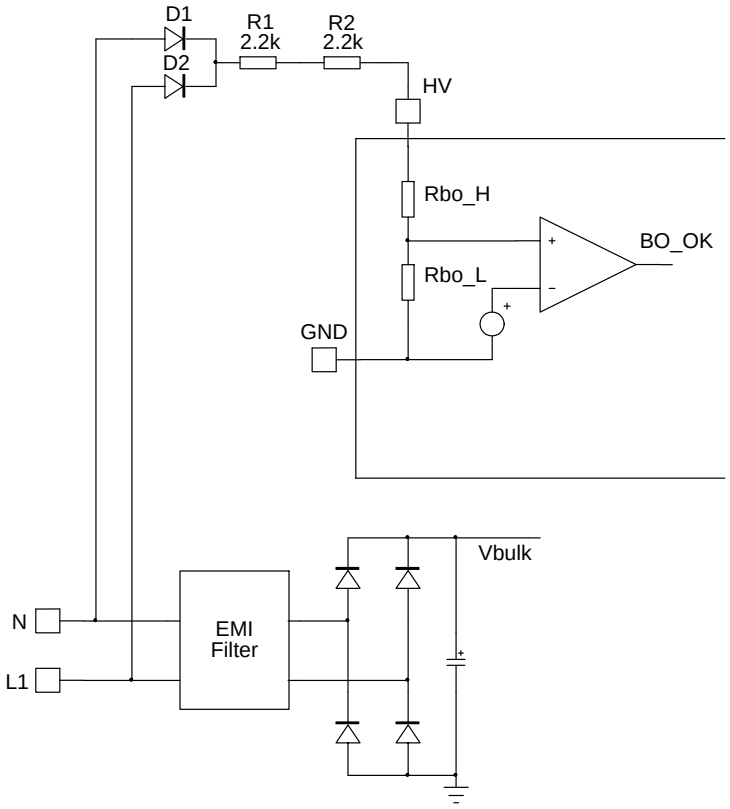


Figure 46. Simplified View of the Brown−out Circuitry

When the HV pin voltage drops below the $V_{BO(stop)}$ threshold (93 V typically) for more than the 50−ms blanking time ($T_{BO(stop)}$), the brown−out protection trips: the controller stops generating DRV pulses and maintains V_{cc} to the 5.5−V $V_{CC(bias)}$ level. This state is maintained by the high−voltage current−source until the input voltage happens to exceed the brown−out upper threshold ($V_{BO(start)}$ that is 101 V typically). At that moment, the controller briefly grounds the V_{cc} capacitor to make a fresh start−up sequence with soft−start.

Please note that the HV start−up current is not reduced for the time when V_{CC} is below $V_{CC(inhibit)}$ (as it happens when the power supply is first plugged in) not to delay the power supply recovery.

If a brown−out event occurs during the V_{cc} capacitor charge phase, the start−up phase is interrupted but the V_{cc} pin is not grounded to make a fresh restart. The start−up resumes as soon as the line recovers (terminating the brown−out situation).

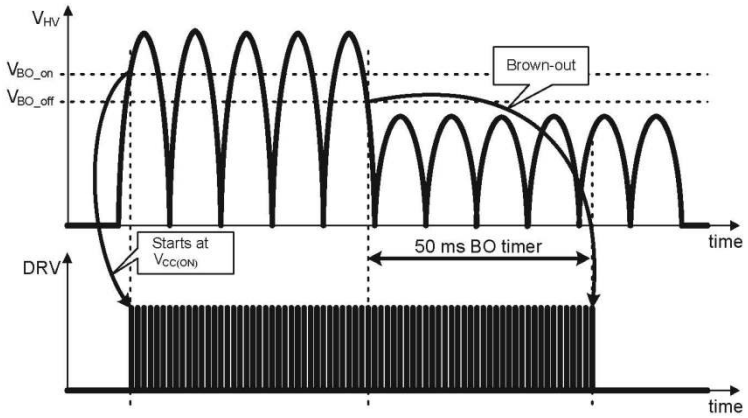


Figure 47. Internal Circuit Implements a 50−ms Timeout to Accommodate with Full−wave Rectification

X2 Discharge Circuitry

The NCP1339 X2 discharge circuitry in Figure 48 uses a dedicated pin (X2) together with an external charge pump−based sensing network to detect the presence or the absence of the mains. Owing to this simple external source, the X2 circuitry is independent from the rest of the controller that can be fully disabled in the off mode. A 100−ms timeout block makes sure the X2 discharge switch is only activated upon a real mains loss (when the user unplugs the converter) and not when a parasitic ac line dropout occurs. The internal V_{cc} discharge switch is activated once the X2 timer elapses. At that moment, the HV startup current source is enabled and pumps out the energy stored by the X2 capacitors.

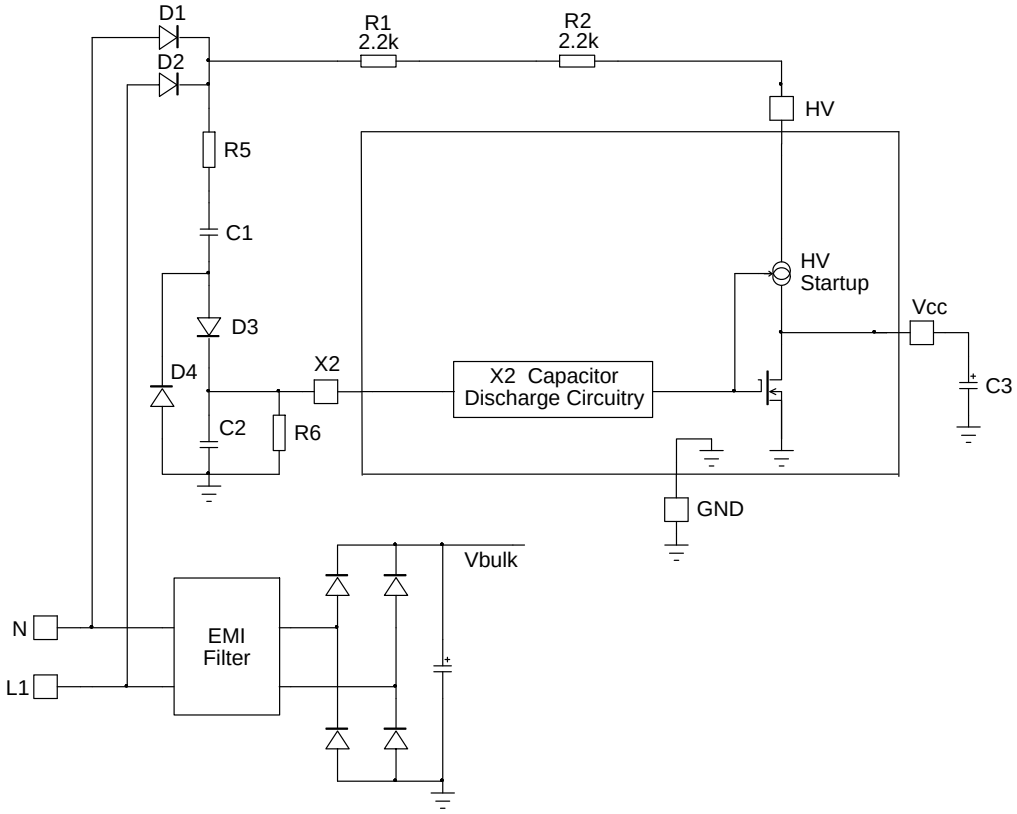


Figure 48. Simplified Block Diagram of X2 Capacitor Discharge Circuitry

An over temperature protection block monitors the junction temperature during the discharge process and avoids thermal runaway, in particular during open/short pins safety tests. Please note that the X2 discharge capability is also active during off−mode but also before the controller actually starts to pulse (e.g. if the user unplugs the converter during the start−up sequence).

Power Savings Mode

The NCP1339 features a dedicated input (remote pin) that allows the user to activate an ultra−low consumption mode. Figure 49 describes the internal arrangement of the remote circuitry. In normal operation, the optocoupler is biased from the secondary side and pulls the remote pin to ground. When the secondary−side circuitry decides to release the optocoupler, the remote pin level starts to grow. It is lifted up by R_1 connected to the auxiliary V_{cc}. C_3, R_1 and R_2 introduce a time constant that prevents the converter from entering the off mode immediately, in case spurious noise would appear on the opto LED bias current. When the voltage across C_2 eventually reaches 8 V, the controller enters the off mode. In the absence of pulses, the auxiliary no longer maintains V_{cc} that slowly vanishes to 0. At this moment, the X2 monitoring circuit is the only living block and the IC power consumption is reduced to an extremely low level. The voltage on the REM pin starts to fall. When it reaches the re−start level (1.5 V), the controller resumes operation and initiates a fresh start−up sequence. If no secondary−side signal appears to bias the optocoupler LED, a new self−relaxing cycle takes place when the REM pin voltage reaches 8 V. If a secondary−side signal biases optocoupler before the REM pin voltage has reached 8 V, the power supply operates normally.

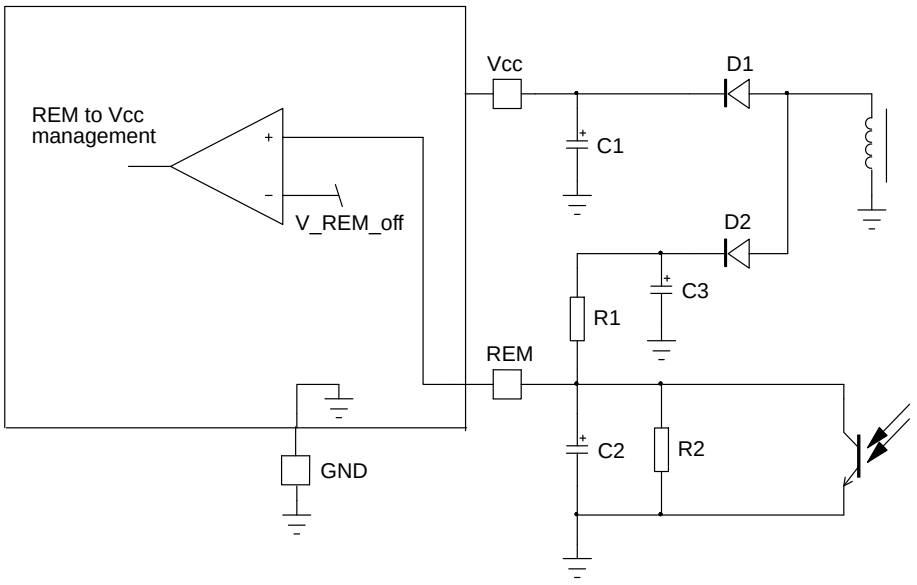


Figure 49. Simplified Block Diagram of the Remote Control Input

In summary, the REM pin works as follows:

- When pulled below a certain level (V_REM_on, 1.5 V typical), the power supply operates normally. As capacitors are connected to this pin, it is important to discharge them properly during the start−up sequence. A 100−ms timer performs this function by pulling the pin to ground. It is operating in any re−start conditions (brown−out recovery, short−circuit, latch reset and so on) except in the self−relaxing PSM mode (during which the voltage on the pin swings up and down.
- When brought above a certain level (V_REM_off, 8 V typical), the power supply stops working. In the absence of an external bias, the remote pin starts to drop at a pace imposed by the various time constants around it. During this mode, despite the absence of V_{cc}, the X2 discharge circuitry remains active and monitors the ac input line.

Fault Input

The NCP1339 includes a dedicated fault input accessible via the Fault pin. Figure 50 shows the architecture of the Fault input. The controller can be latched by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. An active clamp prevents the Fault pin voltage from reaching the $V_{Fault(OVP)}$ if the pin is open. To reach the upper threshold, the external pull−up current has to be higher than the pull−down capability of the clamp (set by $R_{Fault(clamp)}$ at $V_{Fault(clamp)}$), i.e., approximately 1 mA.

This function is typically used to detect a V_{CC} or auxiliary winding overvoltage by means of a Zener diode generally in series with a small resistor (see Figure 50).

Neglecting the resistor voltage drop, the OVP threshold is then:

$$V_{AUX(OVP)} = V_Z + V_{Fault(OVP)}, \quad \text{(eq. 4)}$$

where VZ is the Zener diode voltage.

The controller can also be latched off if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP\_in)}$, typically 0.4 V. This capability is normally used for detecting an overtemperature fault by means of an NTC thermistor. A pull up current source $I_{Fault(OTP)}$, (typically 45.5 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP\_in)}$.

The circuit detects an overtemperature situation when:

$$R_{NTC} \cdot I_{Fault(OTP)} = V_{Fault(OTP)}. \quad \text{(eq. 5)}$$

Hence, the OTP protection trips when

$$R_{NTC} = \frac{V_{Fault(OTP)}}{I_{Fault(OTP)}} \quad \text{(eq. 6)}$$

that is 8.8 kohms typically.

The controller bias current is reduced during power up by disabling most of the circuit blocks including $I_{Fault(OTP)}$. This current source is enabled once V_{CC} reaches $V_{CC(on)}$. A bypass capacitor is usually connected between the Fault and GND pins. It will take some time for V_{Fault} to reach its steady state value once $I_{Fault(OTP)}$ is enabled. Therefore, the lower fault comparator (i.e. overtemperature detection) is ignored during soft−start.

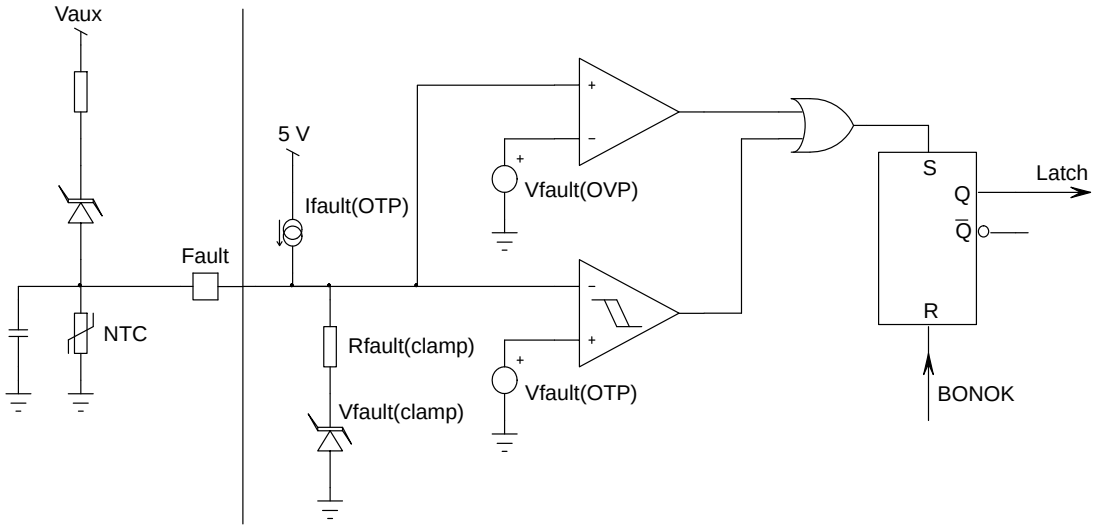


Figure 50. Fault Detection Schematic

As a matter of fact, the controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Upper and lower fault detector have blanking delays to prevent noise from triggering them. Both blanking timers ($t_{delay(Fault\_OVP)}$ and $t_{delay(Fault\_OTP)}$) are typically 27.5 μs.

When the part is latched−off, the drive is immediately turned off. Also, V_{CC} drops and stabilize to the 5.5−V $V_{CC(bias)}$ level. The power supply needs to be un−plugged to reset the part as a result of a BONOK (BO fault condition) and/or the X2 circuitry activation.

PSM mode cannot be triggered in latched−off mode.

Zero Current Detection

The NCP1339 integrates a quasi−resonant (QR) flyback controller. The power switch turn−off of a QR converter is determined by the peak current set by the feedback loop. The switch turn−on is determined by the transformer demagnetization. The demagnetization is detected by monitoring the transformer auxiliary winding voltage.

Turning on the power switch once the transformer is demagnetized or reset reduces switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lump capacitance eventually settling at the input voltage. A QR controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce switching losses and electromagnetic interference (EMI).

As sketched by Figure 51, a valley is detected once the ZCD pin voltage falls below the QR flyback demagnetization threshold, $V_{ZCD(th)}$, typically 55 mV. The controller will switch once the valley is detected or increment the valley counter depending on FB voltage.

Timeout

The ZCD block actually detects falling edges of the auxiliary winding voltage applied to the ZCD pin. At start−up or other transient phases, the ZCD comparator may be unable to detect such an event. Also, in the case of extremely damped oscillations, the system may not succeed in detecting all the valleys required by VLO operation (see next section). In this condition, the NCP1339 ensures continued operation by incorporating a maximum timeout period that resets when a demagnetization phase is detected. The timeout signal substitutes ZCD signal for the valley counter. Figure 51 shows the timeout period generator circuit schematic. The steady state timeout period, $t_{(out2)}$, is set at 6 μs.

During startup, the output voltage is still low leading to long demagnetization phases difficult to detect since the auxiliary winding voltage is small as well. In this condition, the 6−μs steady−state timeout is generally shorter than the inductor demagnetization period and if used to restart a switching cycle, it can cause continuous current mode (CCM) operation for few cycles until the voltage on the ZCD pin is high enough for proper valleys detection. A longer timeout period, $t_{(out1)}$, (typically 100 μs) is therefore set during soft−start to prevent CCM operation.

In VLO operation, the timeout periods of time are counted instead of valleys when the drain−source voltage oscillations are too damped to be detected. For instance, if the circuit must turn on at the fifth valley and if the ZCD ringing only enables to detect:

- Valleys 1 to 4: the circuit generates a DRV pulse 6 μs (steady−state timeout delay) after valley 4 detection.
- Valleys 1 to 3: the timeout delay must run twice so that the circuit generates a DRV pulse 12 μs after valley 3 detection.

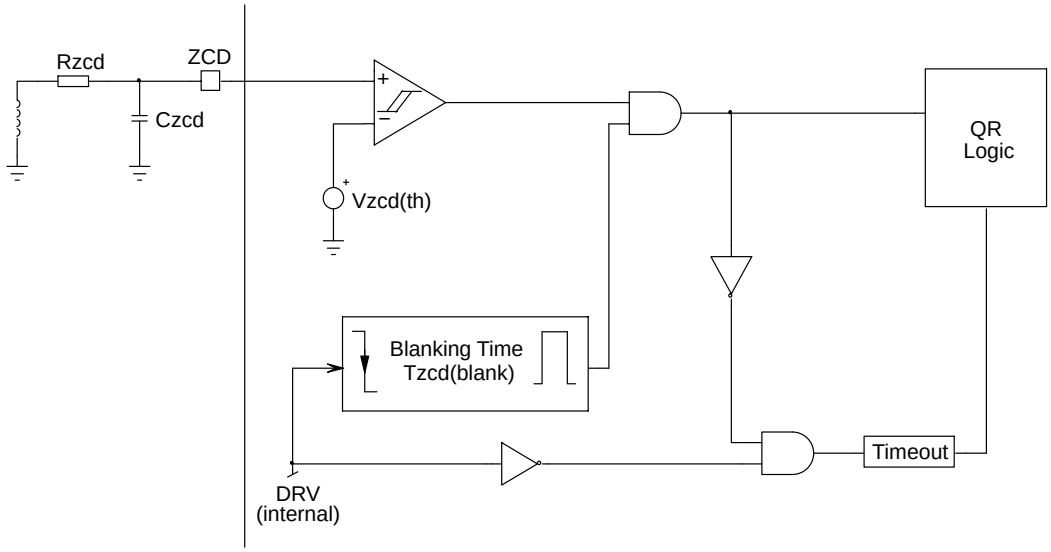


Figure 51. Valley Lockout Detection Circuitry Internal Schematic

Valley Lockout (VLO) and Frequency Foldback (FF)

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. In other words, a load reduction increases the operating frequency. A maximum frequency clamp can be useful to limit the operating frequency range. However such an approach causes instabilities since when this clamp is active, the controller tends to jump (or hesitate) between two valleys generating audible noise.

Instead, the NCP1339 incorporates a patent pending valley lockout circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly. This technique extends QR operation over a wider output power range while maintaining good efficiency and limiting the maximum operating frequency.

The operating valley (1st, 2nd, 3rd, 4th, 5th or 6th) is determined by the FB voltage. As V_{FB} decreases or increases, the valley comparators toggle one after another to select the proper valley. The decimal counter increases each time a valley is detected. The activation of an “n” valley comparator blanks the “n−1” or “n+1” valley comparator output depending if V_{FB} decreases or increases, respectively. Figure 52 shows a typical frequency characteristic obtainable at low line in a 60−W application.

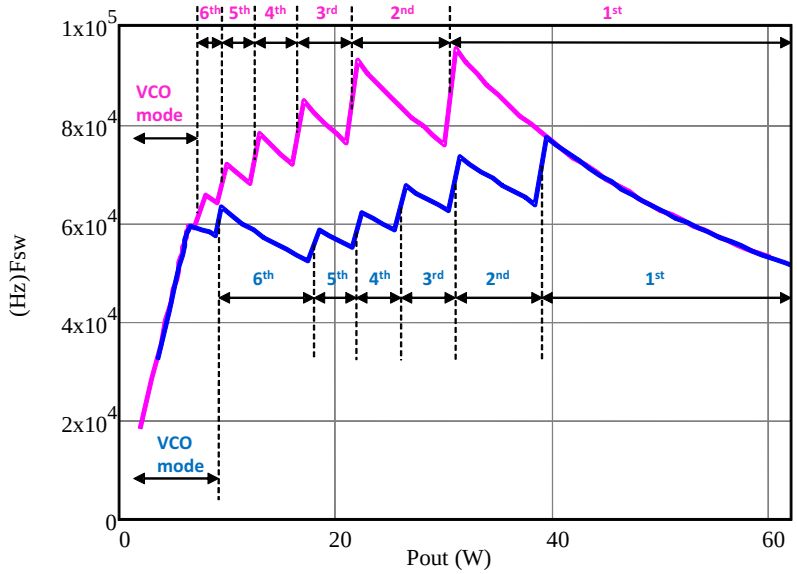


Figure 52. Valley Lockout Frequency vs Output Power Relationship

When an “n” valley is asserted by the valley selection circuitry, the controller is locked in this valley until the FB voltage decreases to the lower threshold (“n+1” valley activates) or increases to the “n valley threshold” + 600 mV (“n−1” valley activates). The regulation loop adjusts the peak current to deliver the necessary output power. Each valley selection comparator features a 600−mV hysteresis that helps stabilize operation despite the FB voltage swing produced by regulation loop.

Valley FB Thresholds (typical values):

FB Falling		FB Rising	
1st to 2nd valley	1.4 V	FF mode to 6th valley	1.0 V
2nd to 3rd valley	1.2 V	6th to 5th valley	1.5 V
3rd to 4th valley	1.1 V	5th to 4th valley	1.6 V
4th to 5th valley	1.0 V	4th to 3rd valley	1.7 V
5th to 6th valley	0.9 V	3rd to 2nd valley	1.8 V
6th valley to FF mode	0.8 V	2nd to 1st valley	2.0 V

Frequency Foldback

As the output load decreases (FB voltage decreases), the valleys are incremented from 1 to 6. For versions without IFF pin, if when the sixth valley is reached, the FB voltage further decreases below 0.8 V, the controller enters the frequency foldback mode (FF). The current setpoint being internally forced to remain above 0.2 V (setpoint corresponding to V_{FB} = 0.8 V), the controller regulates the power delivery by modulating the switching frequency. When a load increase causes FB to exceed the 1−V FF upper threshold (200−mV hysteresis), the circuit recovers VLO operation.

For versions with the IFF pin available, both frequency foldback threshold and frozen peak current are adjustable. Thanks to an external pull down resistor combined with the internal pull up current source ($I_{FF(bias)}$), the voltage develops across this resistor will determine when the controller enters in FF mode. In FF operation, the peak current is frozen to (V_{IFF}/4). When as a result of a load increase, FB exceeds back the (V_{IFF} + 200 mV) level (200 mV hysteresis), the circuit recovers VLO operation.

In frequency foldback mode, the system reduces the switching frequency by adding some dead−time after the 6th valley is detected. This dead−time increases when the FB voltage decays. There is no discontinuity when the system transitions from VLO to FF and the frequency smoothly reduces as FB goes below 0.8 V (or V_{IFF}).

The dead−time is dimensioned to generate a 2−μs dead−time when V_{FB} = 0.8 V and could linearly go to virtually infinity as V_{FB} falls down to 0.4 V if the switching was not forced to keep above 25−kHz to eliminate risk of audible noise.

Figure 53 summarizes the operation mode with respect to the FB voltage for versions without IFF pin (fixed internally to 0.8 V).

25−kHz Frequency Clamp and Skip Mode

As aforementioned, the circuit prevents the switching frequency from dropping below 25 kHz. When the switching cycle is longer than 40 μs, the circuit forces a new switching cycle. However, the 25−kHz frequency clamp cannot generate a DRV pulse until the demagnetization is completed. In other words, it cannot cause operation in continuous conduction mode.

Since the NCP1339 forces a minimum peak current (as aforementioned, the circuit prevents the peak current from dropping below (0.2 V / R_{SENSE} or (V_{IFF}/4) / R_{SENSE}) where R_{SENSE} is the current sense resistor) and a minimum frequency (25 kHz typically), the power delivery cannot be continuously controlled down to zero. Instead, the circuit stops pulsing when the FB voltage drops below 400 mV and recovers operation when V_{FB} exceeds 450 mV (50−mV hysteresis). This skip−mode method provides an efficient power control in light load.

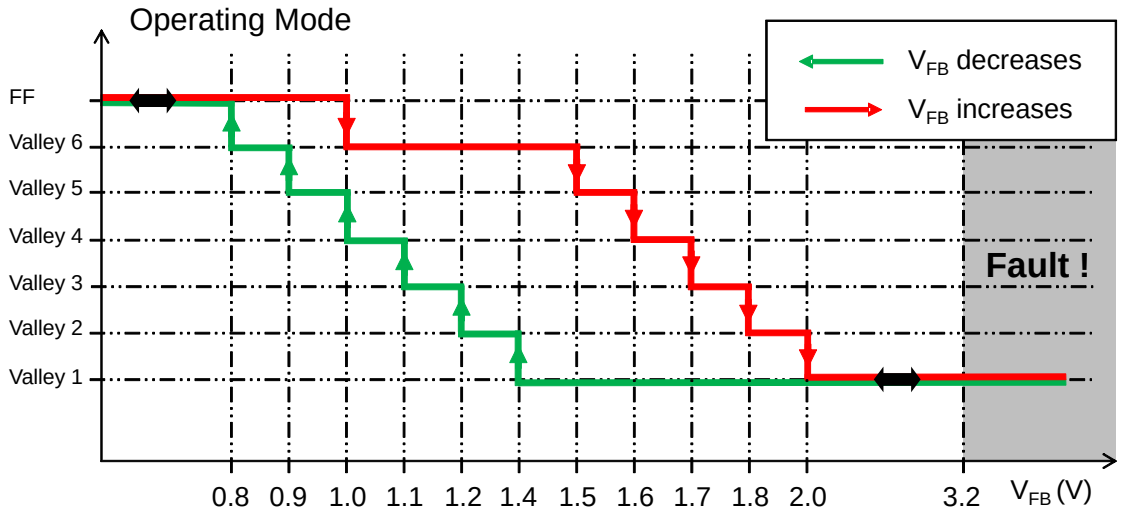


Figure 53. Valley Lockout Thresholds Without IFF Pin

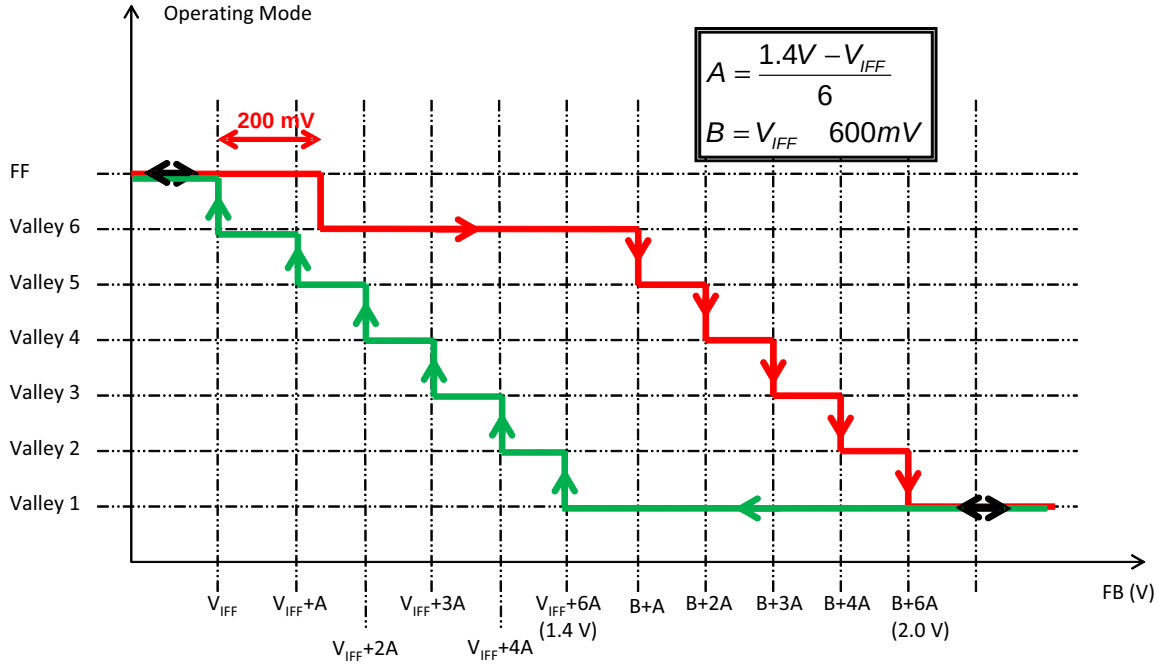


Figure 54. Valley Lockout Thresholds With IFF Pin

Over Power Compensation (OPP)

The power delivered by a QR flyback stage is an increasing function of the bulk voltage, V_{bulk}. It is however desirable to clamp the power delivery to limit the stress on the power components that can otherwise be excessive during transient or fault conditions.

An integrated overpower circuit provides a relatively constant output power across bulk voltage, V_{bulk}. Practically, the maximum peak current is made a decreasing function of the bulk voltage. The direct measure of the V_{bulk} high−voltage rail would cause losses in the sensing network and hence alter the standby efficiency.

Instead, the auxiliary winding voltage (V_{AUX}) is used. During power−switch on−time, V_{AUX} provides a negative voltage that is a V_{bulk} portion (input voltage scaled down by the primary to auxiliary winding turns ratio) as shown in Figure 55. The negative voltage applied to the pin is referred as V_{OPP}. The maximum internal current setpoint ($V_{CS(OPP)}$) is the sum of V_{OPP} and peak current sense threshold, V_{ILIM1}. The current setpoint is calculated using Equation 7.

$$V_{CS(OPP)} = V_{ILIM1} + V_{OPP} \qquad \text{(eq. 7)}$$

That is that:

$$V_{CS(OPP)} = V_{ILIM1} - \left(\frac{N_{AUX}}{N_P} \cdot V_{BULK}\right) \qquad \text{(eq. 8)}$$

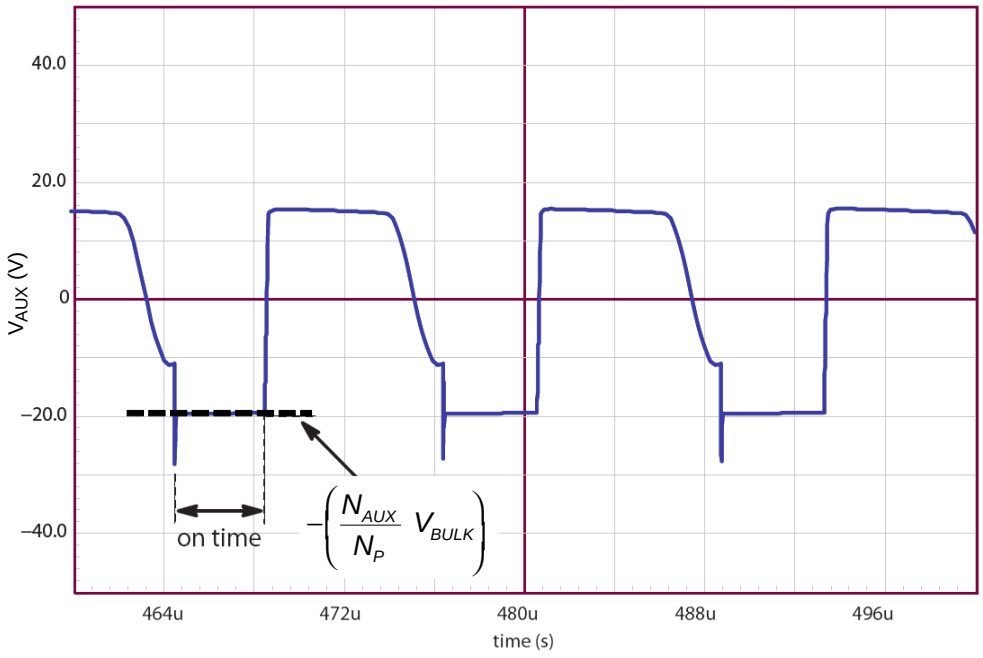


Figure 55. Auxiliary Winding Voltage Waveform

For example, (V_{OPP} = −0.25 V) results in a current setpoint of 0.55 V. In general, V_{OPP} is selected in the range of −200 mV at the highest line level. Refer to application notes for more details.

$$\left(V_{CS(OPP)} = 0.8-0.25 = 0.55 = 68.75\% \cdot 0.8 = 68.75\% \cdot V_{ILIM1}\right)$$

The OPP pin is not designed to operate below –250 mV which corresponds to a 31.25% decrease of the maximum current limit. If a lower voltage happens to be applied, the internal ESD diode that clamps OPP pin negative voltages may turn on and lead to carriers injection within the die. To avoid possible resulting disturbance, care must be taken to limit the current sourced by the diode below 2 mA. If the circuitry of Figure 56 is used, a conservative condition is:

$$\frac{V_{AUX,max}}{R_{OPP1}} \geq -2\ mA \Rightarrow R_{OPP1} \geq -\frac{V_{AUX,max}}{2\ m} \qquad \text{(eq. 9)}$$

Finally, please note that another comparator internally fixes the maximum peak current set point to V_{ILIM1}. Hence, even if the OPP pin is adversely biased above 0 V, the current setpoint remains clamped to 0.8 V typically.

For optimum performance over temperature, we recommend keeping the low−side OPP resistor below 3 kΩ.

Current Setpoint

As explained in this operating description, the current setpoint is affected by several functions. Figure 56 summarizes these interactions. As shown by this figure, the current setpoint is FB/4. However, this value is limited by the following functions:

- This level is clamped during the soft−start phase. The setpoint is actually limited by a clamp level ramping from 0 to 0.8 V within 4 ms.
- It is also limited by the OPP function: during the on−time, a negative voltage is applied to the OPP pin. This voltage is summed with a 0.8−V voltage reference to form the actual maximum setpoint (see OPP section).

It must be noted that the OPP pin voltage is high during the off−time. The summer is designed to face this situation without degradation of the circuitry.

- A minimum setpoint is forced that equals to V_{freeze} (0.2 V, typically).
- In addition, a second OCP comparator ensures that in any case the current setpoint is limited to 0.8 V. This prevents the over−current limit from being increased due to the OPP function if a positive voltage is accidentally applied during the on−time. Hence, even in this faulty condition, the MOSFET current setpoint remains limited to V_{ILIM1} (0.8 V typically).

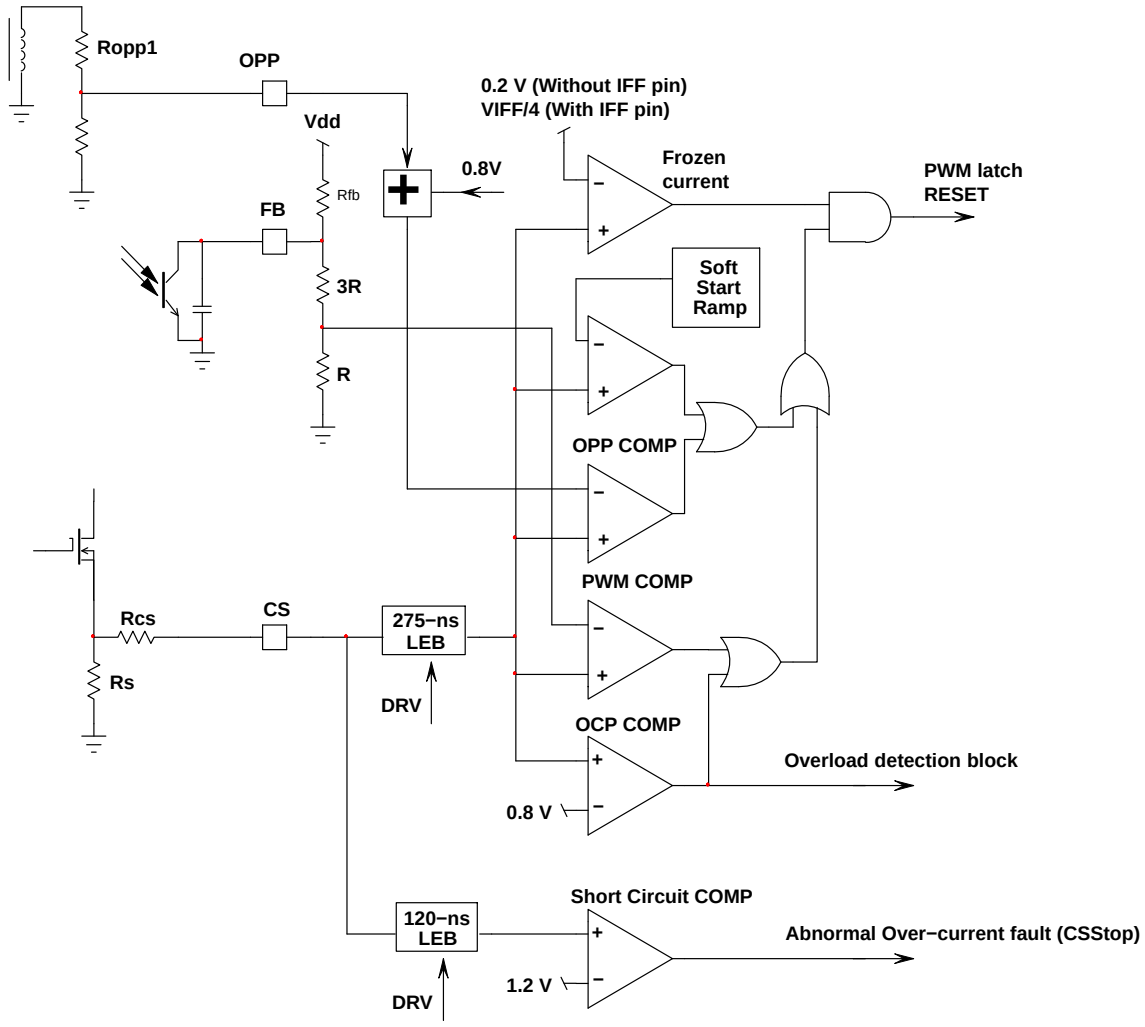


Figure 56. Current Setpoint

Current Sense and Associated Protections

The feedback voltage (V_{FB}) is internally divided by K_{FB} (K_{FB}=4, typically) to form the current setpoint. The power switch on time is modulated by comparing a ramp proportional to the switch current to V_{FB}/K_{FB} using the PWM Comparator. The switch current is sensed across a current sense resistor, R_{SENSE} and the resulting voltage is applied to the CS pin. The current sense signal is blanked by a leading edge blanking (LEB) circuit. The blanking period eliminates the leading edge spike and high frequency noise during the switch turn−on event. The LEB period, $t_{CS(LEB1)}$, is typically 275 ns. The drive pulse terminates once the current sense signal exceeds V_{FB}/K_{FB}.

The Maximum Peak Current Comparator compares the current sense signal to a reference voltage to limit the maximum peak current of the system. The maximum peak current reference voltage, V_{ILIM1}, is typically 0.8 V. The maximum peak current setpoint is reduced by the overpower compensation (OPP) circuitry. In case, a wrong OPP signal is applied to the circuit, a second comparator to V_{ILIM1} is placed to get sure that the current setpoint is at least limited to V_{ILIM1}. An overload condition causes the output of one of the Maximum Peak Current Comparators to transition high and enable the overload timer. Figure 57 shows the implementation of the current sensing circuitry.

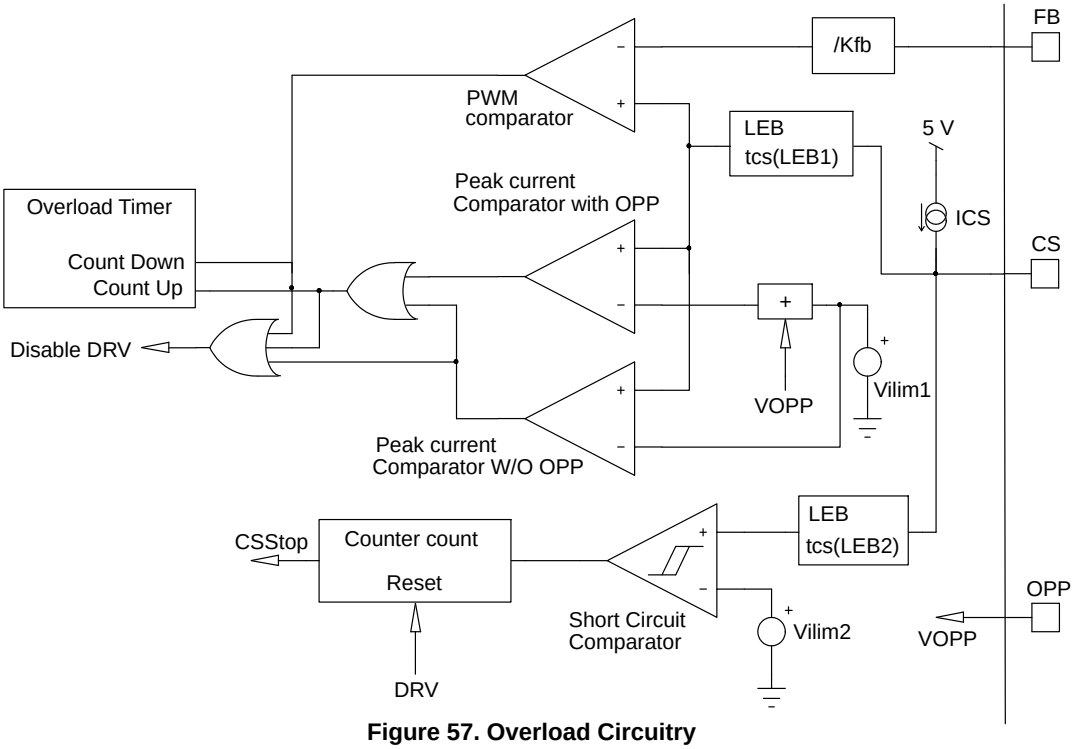


Figure 57. Overload Circuitry

Overload Protection

The overload timer integrates the duration of the overload fault. That is, the timer count increases while the fault is present and reduces its count once it is removed. The timer counts up or down in 10 ms increments. The overload timer duration, t_{OVLD}, is typically 160 ms. If both the PWM and Maximum Peak Current Comparators toggle at the same time, the PWM Comparator takes precedence and the overload timer counts down. When the overloard timer elapses, the circuit detects an overload condition and

- The controller latches off (versions D, E, F and I) or
- Enters a safe low duty−ratio operation named auto−recovery mode (versions C, G, H and J).

Latching or Auto−Recovery Mode

The NCP1339D, E, F and I latch off when it detects an overload situation. In this condition, the circuit stops generating drive pulses and let V_{CC} drop down. When V_{CC} has reached its 5.5 V $V_{CC(bias)}$ level, the circuit maintains V_{CC} to this level. It cannot recover operation until V_{CC} drops below its reset level. Practically, the power supply must be unplugged to be reset.

The NCP1339C, G, H and J versions are autorecovery. When an overload fault is detected, like latched versions, it stops generating drive pulses and let V_{CC} drop down to its 5.5 V $V_{CC(bias)}$ level. However, the V_{CC} is maintained to its 5.5 V $V_{CC(bias)}$ level for 2 s only (typically). After this 2 s delay time, the circuit attempts to restart. More practically, after an overload condition is detected, operation is interrupted and hence, the V_{CC} that is provided by an auxiliary winding, decays. When it reaches $V_{CC(off)}$, the circuit waits for 2 s before allowing the circuit operation recovery. During this delay, V_{CC} is forced to the 5.5 V $V_{CC(bias)}$ level so that the blocks monitoring the line remain active. When this phase is complete, a V_{CC} charge sequence starts.

Figures 58 and 59 show operating waveforms for auto−recovery and latched overload conditions.

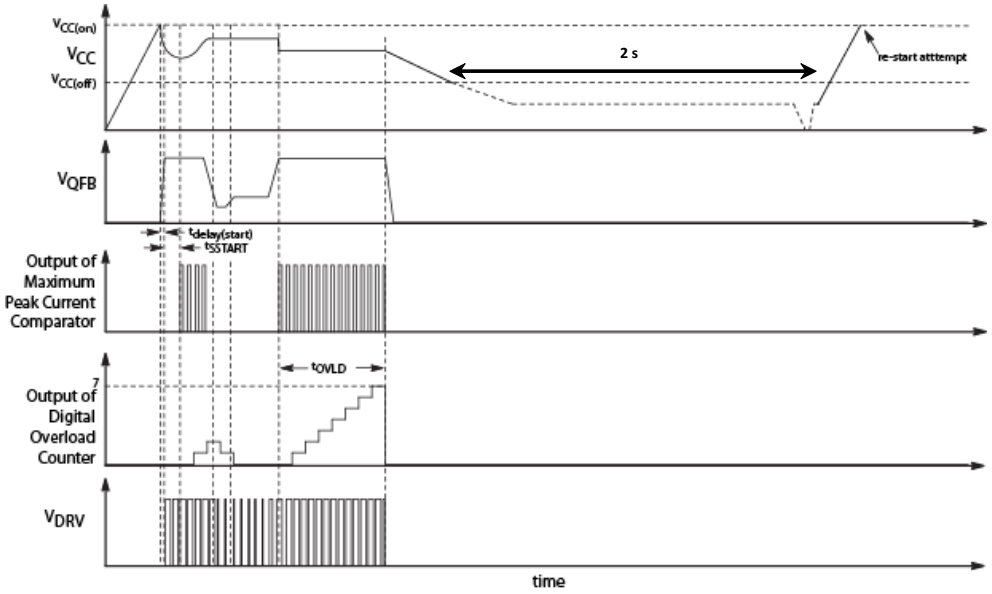


Figure 58. Auto−recovery Overload Operation

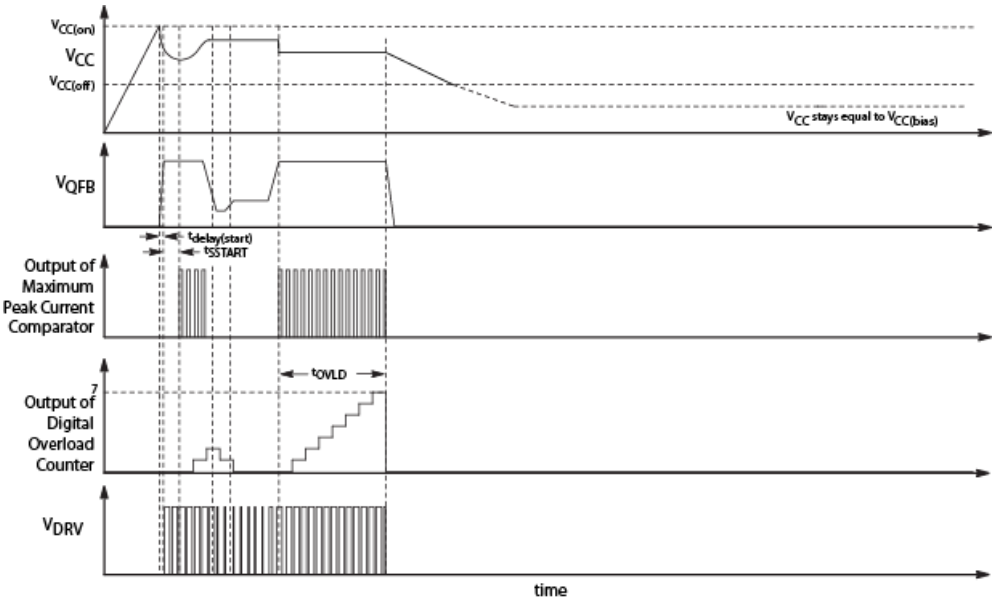


Figure 59. Latched Overload Operation

A 2nd Over−Current Comparator for Abnormal Overcurrent Fault Detection

A severe fault like a winding short−circuit can cause the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{ILIM1}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the power switch current can become huge causing system damage.

The NCP1339 protects against this fault by adding an additional comparator for Abnormal Overcurrent Fault detection. The current sense signal is blanked with a shorter LEB duration, $t_{CS(LEB2)}$, typically 125 ns, before applying it to the Abnormal Overcurrent Fault Comparator. The voltage threshold of the comparator, V_{ILIM2}, typically 1.2 V, is set 50% higher than V_{ILIM1}, to avoid interference with normal operation. Four consecutive Abnormal Overcurrent faults cause the controller to enter latch mode (NCP1339D, E, F and I versions) or auto−recovery (NCP1339C, G, H and J). The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the Fault Overcurrent Comparator.

Protecting from a Failure of the Current Sensing

A 1−μA (typically) pull−up current source, I_{CS}, pulls up the CS pin to disable the controller if the pin is left open.

In addition the maximum on−time (32 μs typically) avoids that the MOSFET stays permanently on if the switch current cannot reach the current setpoint when for instance, the input voltage is low.

Soft−Start

Soft−start is achieved by ramping up an internal reference, V_{SSTART}, and comparing it to current sense signal. V_{SSTART} ramps up from 0 V once the controller powers up. The setpoint rise is then limited by the V_{SSTART} ramp so that a gradual increase of the power switch current during start−up. The soft−start duration (that is, the time necessary for the ramp to reach the V_{ILIM1} steady state current limit), t_{SSTART}, is typically 4 ms.

During soft−start the ZCD timeout duration is extended. This is because, during startup, demagnetization phases are long and difficult to detect since the auxiliary winding voltage is small. In this condition, the 6−μs steady−state timeout is generally shorter than the inductor demagnetization period and if used to restart a switching cycle, it can cause continuous current mode (CCM) operation for few cycles until the voltage on the ZCD pin is high enough for proper valleys detection. A longer timeout period, $t_{(out1)}$, (typically 100 μs) is therefore set during soft−start to prevent CCM operation.

Also, the Fault comparator to 0.4 V (or OTP comparator since typically used for overtemperature) is blanked for the soft−start duration. The pin can then be filtered by an external capacitor.

Jittering Capability

In order to help meet the EMI requirements, the NCP1339 (E, F, G, I and J versions) features the jittering capability to average the spectrum rays over the frequency range. The function consists of sourcing a 0 to 100 μA, 1.3 kHz triangular current out of the CS pin (I_{JIT}). This current together with the external resistor placed on the CS pin generates an offset that will change the actual power switch peak current and hence the operation frequency.

The jittering current source and hence the jittering function is enabled only in high line condition since at low line, the input voltage ripple is generally sufficient to help meet EMI specs. This function is also disabled in Frequency Foldback operation mode.

The jittering function modulates the peak current level. As a result, the FB signal that struggles for compensating this effect and limiting the output voltage ripple, exhibits a swing. The resistor placed between the CS pin and the current sense resistor must not be too high. Otherwise, the jittering offset on the CS pin can lead to a FB swing exceeding the VLO mode 600 mV hysteresis inbuilt to avoid unwanted transitions between valleys. In practice, this resistor is generally below 1 kohm.

Driver

The NCP1339 maximum supply voltage, $V_{CC(max)}$, is 28 V. Typical high−voltage MOSFETs have a maximum gate voltage rating of 20 V. The DRV pin incorporates an active voltage clamp to limit the gate voltage on the external MOSFETs. The DRV voltage clamp, $V_{DRV(high)}$ is typically 12 V with a maximum limit of 14 V.

Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 150°C. A continuous V_{CC} hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next $V_{CC(on)}$ once the IC temperature drops below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 40°C.

The thermal shutdown is also cleared if V_{CC} drops below $V_{CC(reset)}$, a brown−out fault is detected or if the controller enters power savings mode. A new power up sequences commences at the next $V_{CC(on)}$ once all the faults are removed.

ORDERING INFORMATION

Part Number	Overload Protection	Abnormal Overcurrent Fault	ZCD Blanking Time	Jittering Function	Shipping†
NCP1339CDR2G	Auto-Recovery	Auto−recovery	3 μs	Disabled	2500 / Tape & Reel
NCP1339DDR2G	Latching−off	Latching−off	3 μs	Disabled	
NCP1339EDR2G	Latching−off	Latching−off	3 μs	Enabled	
NCP1339FDR2G	Latching−off	Latching−off	0.7 μs	Enabled	
NCP1339GDR2G	Auto-Recovery	Auto−recovery	0.7 μs	Enabled	
NCP1339HDR2G	Auto-Recovery	Auto−recovery	0.7 μs	Disabled	
NCP1339IDR2G	Latching−off	Latching−off	0.7 μs	Enabled	
NCP1339JDR2G	Auto-Recovery	Auto−recovery	0.7 μs	Enabled	

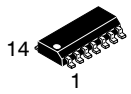
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

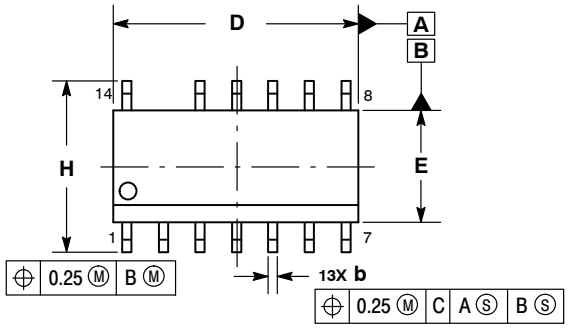
ON Semiconductor®

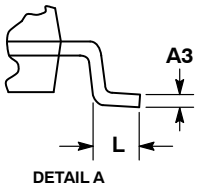
SOIC−14 NB, LESS PIN 13
CASE 751AN−01
ISSUE A

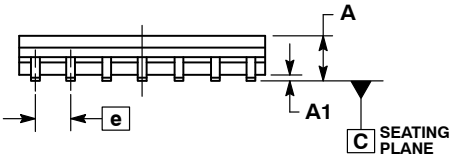
DATE 28 JAN 2008

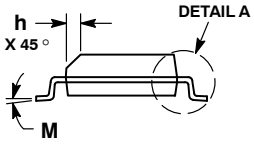


SCALE 1:1





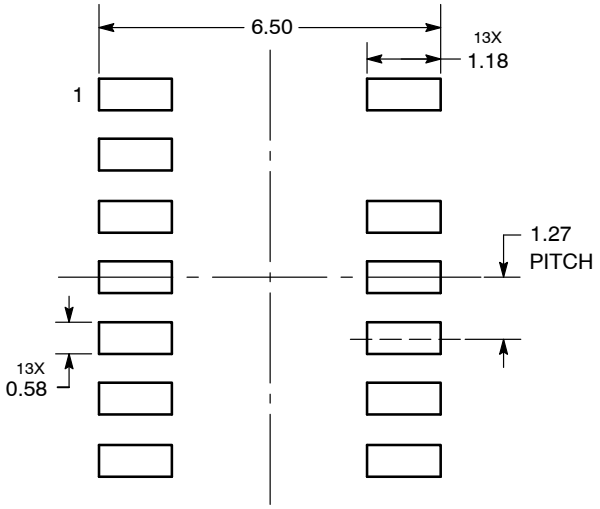




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
A3	0.19	0.25
b	0.35	0.49
D	8.55	8.75
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

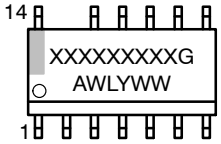
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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