LM48556 Boomer™ Fully Differential, Mono, Ceramic Speaker Driver

Check for Samples: LM48556

FEATURES

- **Fully Differential Amplifier**
- **Externally Configurable Gain**
- **Integrated Charge Pump**
- **Low Power Shutdown Mode**
- **Soft Start Function**

APPLICATIONS

- **Mobile Phones**
- **PDA's**
- **Digital Cameras**

KEY SPECIFICATIONS

- **Output Voltage Swing**
  - **V_{DD} = 3.6V, 1kHz 14.2V_{PP} (typ)**
  - **V_{DD} = 4.5V, 1kHz 17.5V_{PP} (typ)**
- **Power Supply Rejection Ratio**
  - **f = 217Hz, V_{DD} = 3.6V 80dB (typ)**
- **I_{DD} at V_{DD} = 3.6V 4.8mA (typ)**
- **Wake-Up Time 0.5ms (typ)**

DESCRIPTION

The LM48556 is a single supply, mono, ceramic speaker driver with an integrated charge-pump, designed for portable devices, such as cell phones, where board space is at a premium. The LM48556 charge pump allows the device to deliver 17.5V_{PP} (typ) from a single 4.5V supply. Additionally, the charge pump features a soft start function that minimizes transient current during power-up.

The LM48556 features high power supply rejection ratio (PSRR) of 80dB at 217Hz, allowing the device to operate in noisy environments without additional power supply conditioning. Flexible power supply requirements allow operation from 2.7V to 5.0V. Additionally, the LM48556 features a differential input function and an externally configurable gain. A low power shutdown mode reduces supply current consumption to 0.1μA.

Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48556 is available in an ultra-small 12-bump DSBGA package (2mm x 1.5mm).

TYPICAL APPLICATION

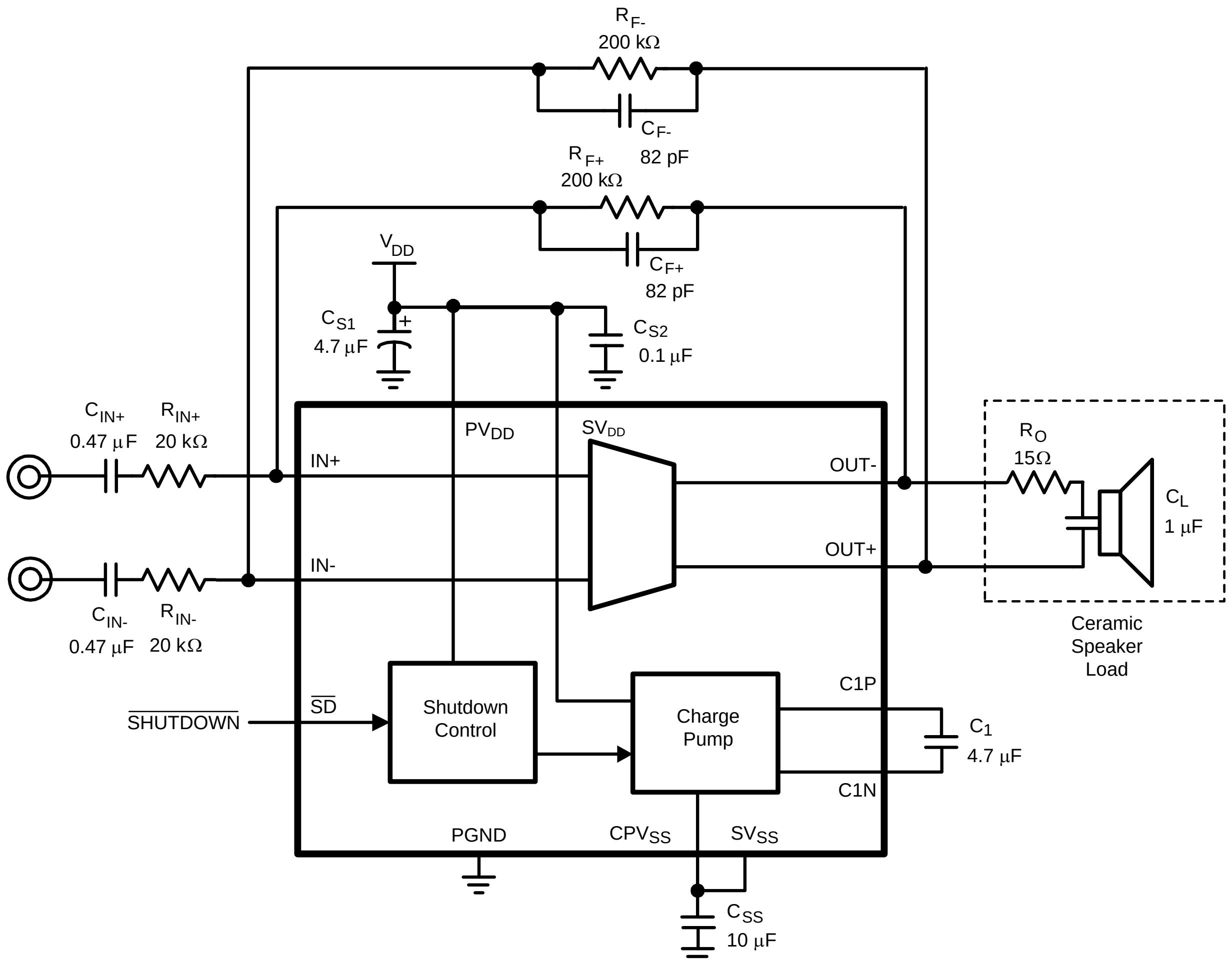


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

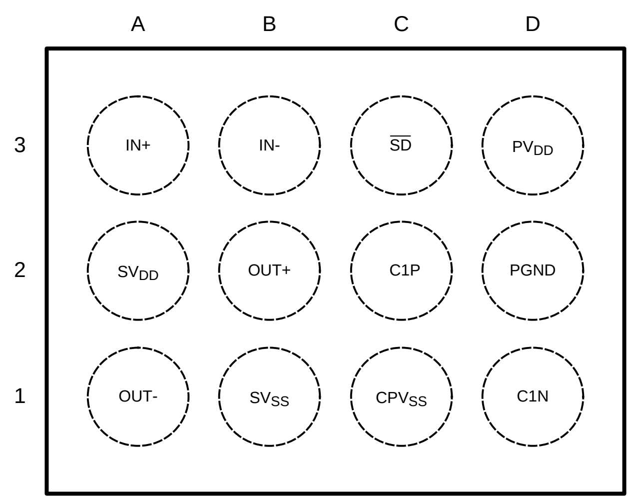


Figure 2. 12 Bump DSBGA - Top View
See Package Number YZR00121AA

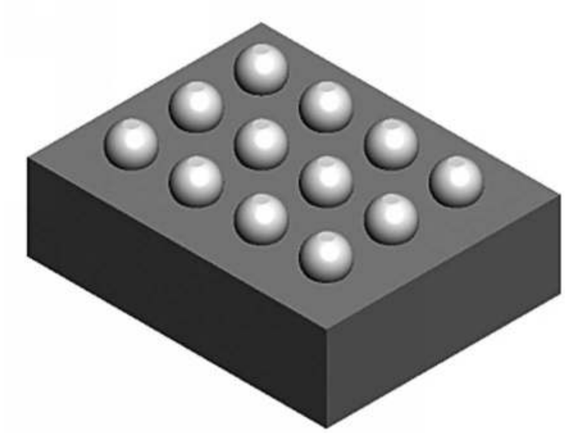


Figure 3. 12 Bump DSBGA - Package View

BUMP DESCRIPTIONS

Bump	Name	Description
A1	OUT-	Amplifier Inverting Output
A2	SV_{DD}	Signal Power Supply - Positive
A3	IN+	Amplifier Non-inverting Input
B1	SV_{SS}	Signal Power Supply - Negative
B2	OUT+	Amplifier Non-inverting Output
B3	IN-	Amplifier Inverting Input
C1	CPV_{SS}	Charge Pump Output Voltage
C2	C1P	Charge Pump Flying Capacitor Positive Terminal
C3	$\overline{SD}$	Active Low Reset Input. Connect to V_{DD} for normal operation. Drive $\overline{SD}$ low to disable.
D1	C1N	Charge Pump Flying Capacitor Negative Terminal
D2	PGND	Power Ground
D3	PV_{DD}	Power Supply

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage (SV_{DD}, PV_{DD})[1]		5.25V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} + 0.3V
Power Dissipation[4]		Internally limited
ESD Rating[5]		2000V
ESD Rating[6]		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (YZR)	114°C/W
Soldering Information		See AN-1112 (SNVA009) Micro SMD Wafer Level Chip Scale

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
(5) Human body model, applicable std. JESD22-A114C.
(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage (SV_{DD}, PV_{DD})	2.7V ≤ _V_{DD} ≤ 5.0V

Electrical Characteristics V_{DD} = 3.6V[1]

The following specifications apply for V_{DD} = 3.6V, $A_{V\text{-}BTL}$ = 20dB (R_F = 200kΩ, R_{IN} = 20kΩ), Z_L = 15Ω+1µF, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48556		Units (Limits)
			Typical[2]	Limit[3]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V	4.8	7	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{SD}}$ = GND (Note 8)	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	C_{IN} = 0.47µF, A_V = 1V/V (0dB)	0.6	4	mV (max)
T_{WU}	Wake-up Time		0.5		ms
V_{OUT}	Output Voltage Swing	THD+N = 1% (max); f = 1kHz	14.2		V_{PP}
		THD+N = 1% (max); f = 10kHz	11.5	11	V_{PP} (min)
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 11V_{PP}, f = 1kHz			
		A_V = 0dB	0.005		%
		A_V = 20dB	0.03		%
ε_{OS}	Output Noise	A-weighted filter, V_{IN} = 0V Input referred	8		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}, f = 217Hz	80	60	dB (min)

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(3) Datasheet min/max specification limits are specified by test or statistical analysis.

Electrical Characteristics V_{DD} = 3.6V(1) (continued)

The following specifications apply for V_{DD} = 3.6V, $A_{V\text{-}BTL}$ = 20dB (R_F = 200kΩ, R_{IN} = 20kΩ), Z_L = 15Ω+1µF, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48556		Units (Limits)
			Typical(2)	Limit(3)	
CMRR	Common Mode Rejection Ratio	Input Referred	70	60	dB (min)
V_{LH}	Logic High Threshold Voltage			1.2	V (min)
V_{LL}	Logic Low Threshold Voltage			0.45	V (max)

Electrical Characteristics V_{DD} = 4.5V(1)

The following specifications apply for V_{DD} = 4.5V, $A_{V\text{-}BTL}$ = 20dB (R_F = 200kΩ, R_{IN} = 20kΩ), Z_L = 15Ω+1µF, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48556		Units (Limits)
			Typical(2)	Limit(3)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V	6.5	10	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{SD}}$ = GND (Note 8)	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	C_{IN} = 0.47µF, A_V = 1V/V (0dB)	0.6	4	mV (max)
T_{WU}	Wake-up Time		0.5		ms (max)
V_{OUT}	Output Voltage Swing	THD+N = 1% (max); f = 1kHz	17.5		V_{PP}
		THD+N = 1% (max); f = 10kHz	14.6	14	V_{PP} (min)
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 14V_{PP}, f = 1kHz			
		A_V = 0dB	0.005		%
		A_V = 20dB	0.03		%
ε_{OS}	Output Noise	A-weighted filter, V_{IN} = 0V Input referred	8		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}, f = 217Hz,	80	60	dB (min)
CMRR	Common Mode Rejection Ratio	Input Referred	70	60	dB (min)
V_{LH}	Logic High Threshold Voltage			1.2	V (min)
V_{LL}	Logic Low Threshold Voltage			0.45	V (max)

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(3) Datasheet min/max specification limits are specified by test or statistical analysis.

Typical Performance Characteristics

(Z_L = 15Ω+1µF, A_V = 20dB, BW = 22kHz)

THD+N vs Frequency
V_{DD} = 2.7V, V_O = 8V_{PP}

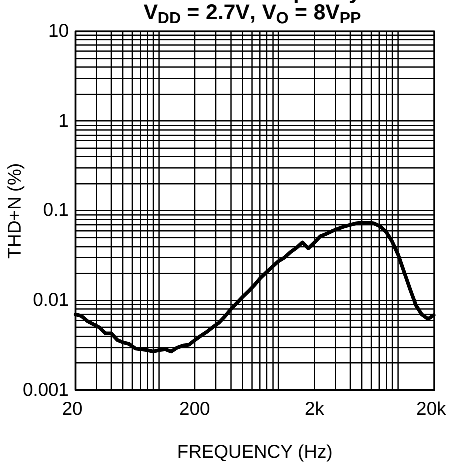


Figure 4.

THD+N vs Frequency
V_{DD} = 3.6V, V_O = 14.2V_{PP}

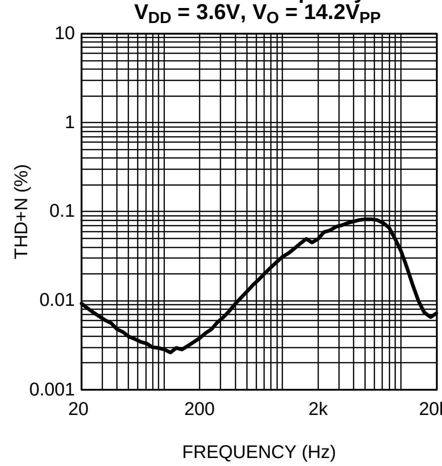


Figure 5.

THD+N vs Frequency
V_{DD} = 4.5V, V_O = 17.5V_{PP}

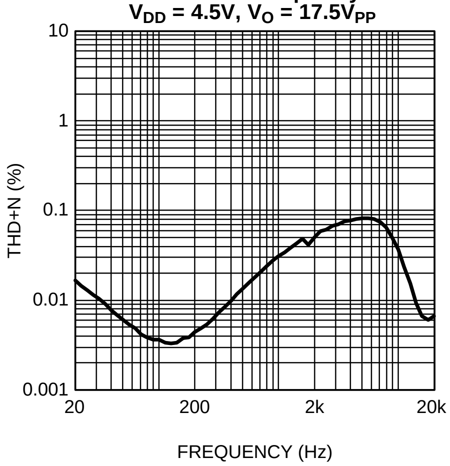


Figure 6.

THD+N vs Output Voltage Swing
V_{DD} = 2.7V, f = 1kHz

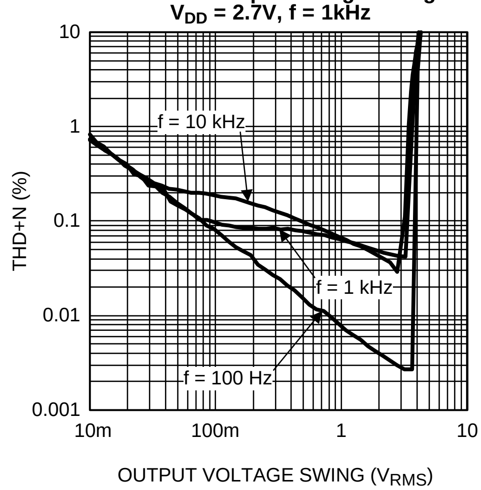


Figure 7.

THD+N vs Output Voltage Swing
V_{DD} = 3.6V, f = 1kHz

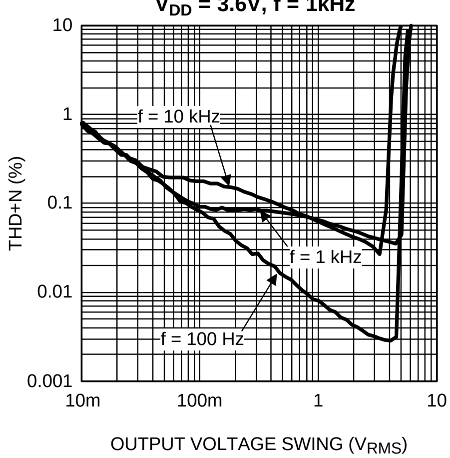


Figure 8.

THD+N vs Output Voltage Swing
V_{DD} = 4.5V, f = 1kHz

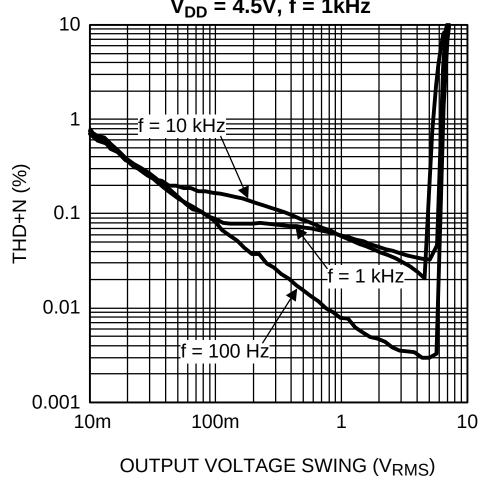


Figure 9.

Typical Performance Characteristics (continued)

(Z_L = 15Ω+1μF, A_V = 20dB, BW = 22kHz)

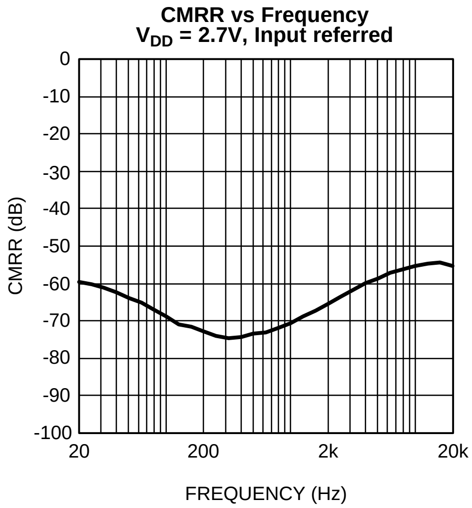


Figure 10.

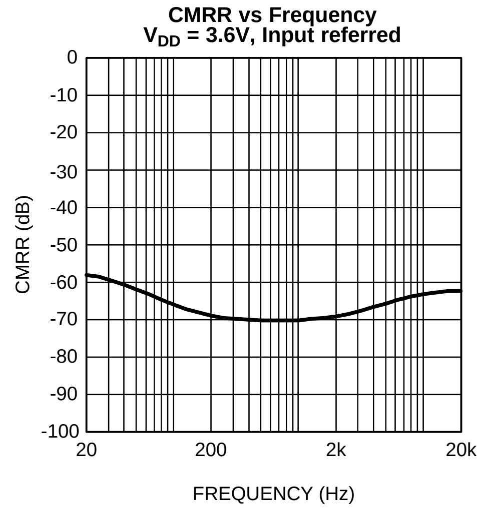


Figure 11.

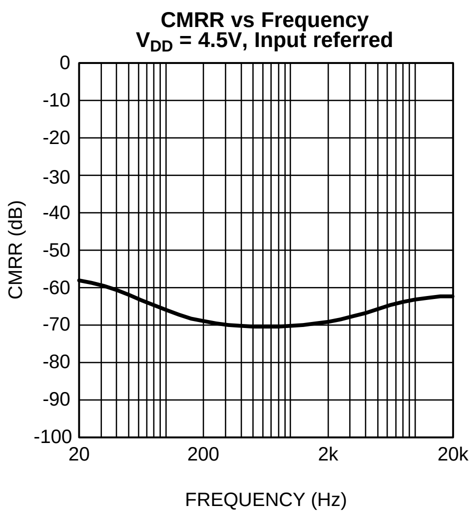


Figure 12.

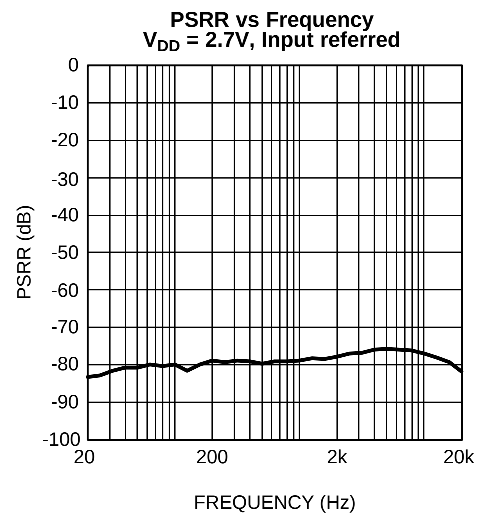


Figure 13.

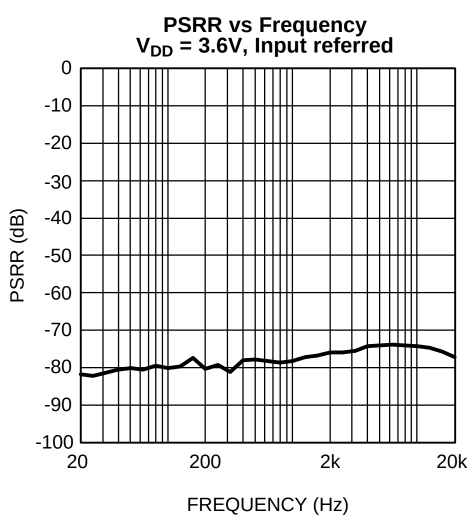


Figure 14.

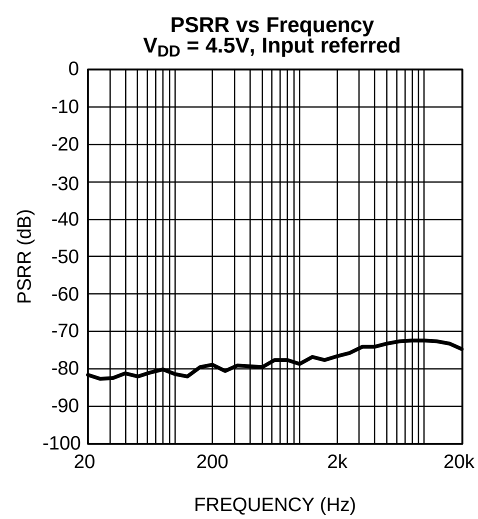


Figure 15.

Typical Performance Characteristics (continued)

(Z_L = 15Ω+1μF, A_V = 20dB, BW = 22kHz)

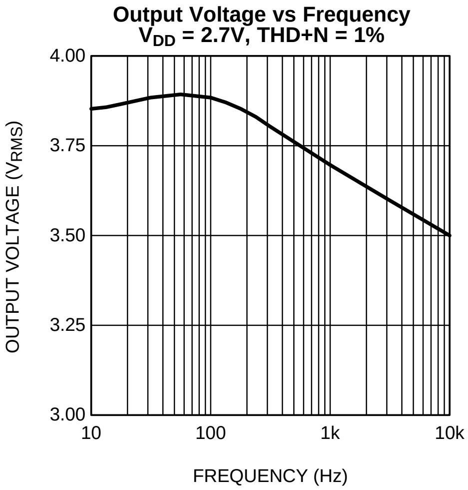


Figure 16.

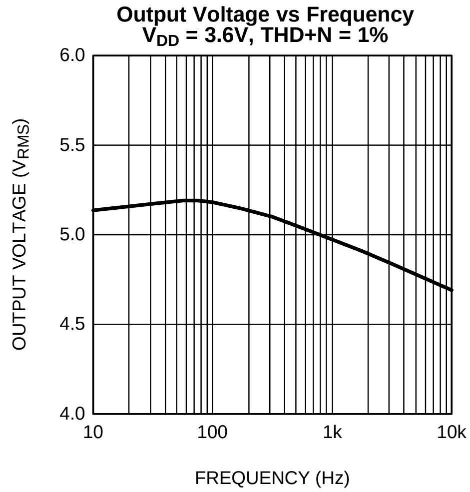


Figure 17.

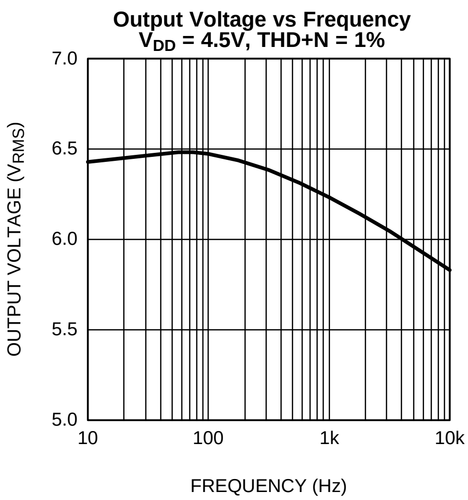


Figure 18.

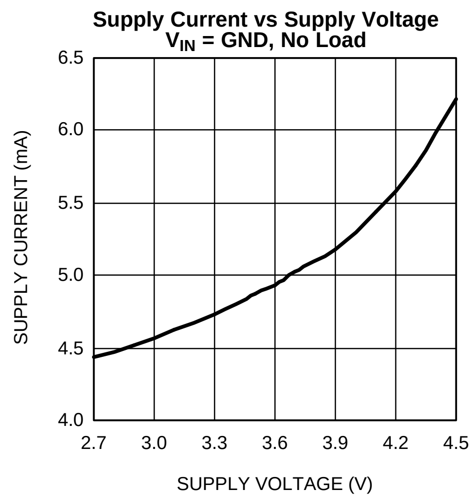


Figure 19.

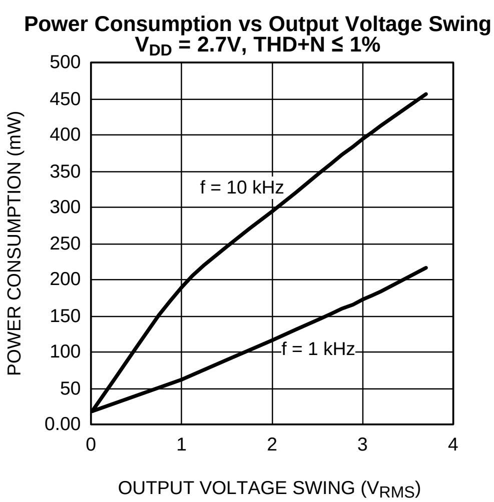


Figure 20.

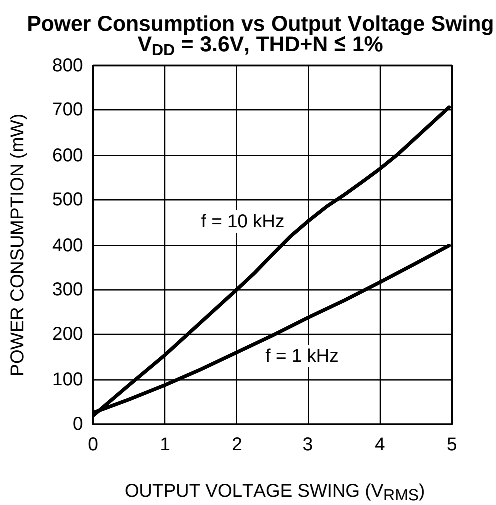


Figure 21.

Typical Performance Characteristics (continued)

(Z_L = 15Ω+1μF, A_V = 20dB, BW = 22kHz)

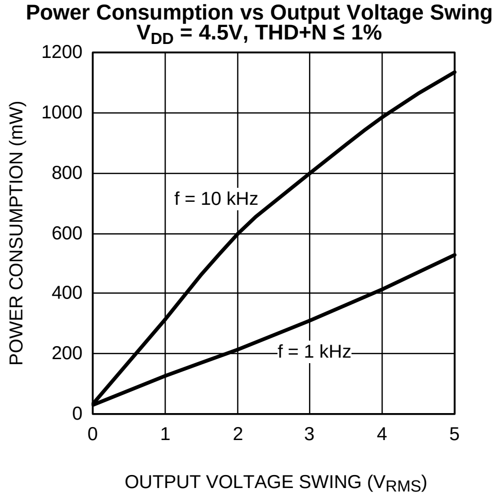


Figure 22.

APPLICATION INFORMATION

GENERAL AMPLIFIER FUNCTION

The LM48556 is a fully differential ceramic speaker driver that utilizes TI's inverting charge pump technology to deliver the high drive voltages required by ceramic speakers, without the need for noisy, board-space consuming inductive based regulators. The low-noise, inverting charge pump creates a negative supply (CPV_{SS}) from the positive supply (PV_{DD}). Because the amplifiers operate from these bipolar supplies, the maximum output voltage swing for each amplifier is doubled compared to a traditional single supply device. Additionally, the LM48556 is configured as a bridge-tied load (BTL) device, quadrupling the maximum theoretical output voltage range when compared to a single supply, single-ended output amplifier, see Bridge Configuration Explained section. The charge pump and BTL configuration allow the LM48556 to deliver over $17V_{P-P}$ at 1kHz to a 1µF ceramic speaker while operating from a single 4.5V supply .

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM48556 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM48556 can be used without input coupling capacitors when configured with a differential input signal.

BRIDGE CONFIGURATION EXPLAINED

The LM48556 is designed to drive a load differentially, a configuration commonly referred to as a bridge-tied load (BTL). The BTL configuration differs from the single-ended configuration, where one side of the load is connected to ground. A BTL amplifier offers advantages over a single-ended device. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Any component common to both outputs is cancelled, thus there is no net DC voltage across the load, eliminating the DC blocking capacitors required by single-ended, single-supply amplifiers.

SHUTDOWN FUNCTION

The LM48556 features a low current shutdown mode. Set $\overline{SD}$ = GND to disable the amplifier and reduce supply current to 0.1µA. Switch $\overline{SD}$ between V_{DD} and GND for minimum current consumption in shutdown. The LM48556 may be disabled with shutdown voltages less than 0.45V, however, the idle current will be greater than the typical 0.1µA value.

PROPER SELECTION OF EXTERNAL COMPONENTS

Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 4.7µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and C_{SS} dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Hold Capacitor (C_{SS})

The value and ESR of the hold capacitor (C_{SS}) directly affects the ripple on CPV_{SS}. Increasing the value of C_{SS} reduces output ripple. Decreasing the ESR of C_{SS} reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Gain Setting Resistor Selection

The amplifier gain of the LM48556 is set by four external resistors, two per each input, $R_{IN\_}$ and $R_{F\_}$ Figure 1. The amplifier gain is given by Equation 1:

$$A_V = R_F / R_{IN} \quad (V/V) \tag{1}$$

Careful matching of the resistor pairs, R_{F+} and R_{F-}, and R_{IN+} and R_{IN-}, is required for optimum performance. Any mismatch between the resistors results in a differential gain error that leads to an increase in THD+N, decrease in PSRR and CMRR, as well as an increase in output offset voltage. Resistors with a tolerance of 1% or better are recommended.

The gain setting resistors should be placed as close to the device as possible. Keeping the input traces close together and of the same length increases noise rejection in noisy environments. Noise coupled onto the input traces which are physically close to each other will be common mode and easily rejected.

Feedback Capacitor Selection

Due to their capacitive nature, ceramic speakers poorly reproduce high frequency audio content. At high frequencies, a ceramic speaker presents a low impedance load to the amplifier, increasing the required drive current. The higher output current can drive the device into clipping, increasing THD+N. Low-pass filtering the audio signal improves audio quality by decreasing the signal amplitude at high frequencies, reducing the speaker drive current. Adding a capacitor in parallel with each feedback resistor creates a simple low-pass filter with the -3dB point determined by Equation 2:

$$f_{-3dB} = 1 / 2\pi R_F C_F \quad (Hz)$$

Where

- R_F is the value of the feedback resistor determined by Equation 1 in the Gain Setting Resistor Selection section
- C_F is the value of the feedback capacitor (2)

The feedback capacitor is optional and not required for normal operation.

Input Capacitor Selection

Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48556. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation 3 below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (Hz)$$

Where

- the value of R_{IN} is determined by Equation 1 in the Gain Setting Resistor Selection section (3)

When the LM48556 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 1% or better are recommended for impedance matching and improved CMRR and PSRR.

SINGLE-ENDED AUDIO AMPLIFIER CONFIGURATION

The LM48556 is compatible with single-ended sources. Figure 4 shows the typical single-ended applications circuit.

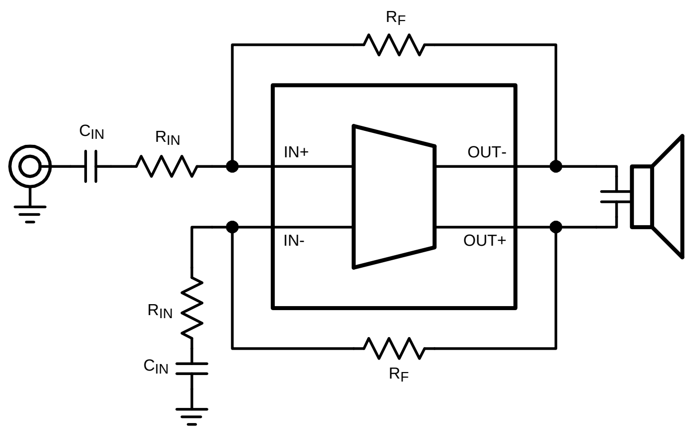
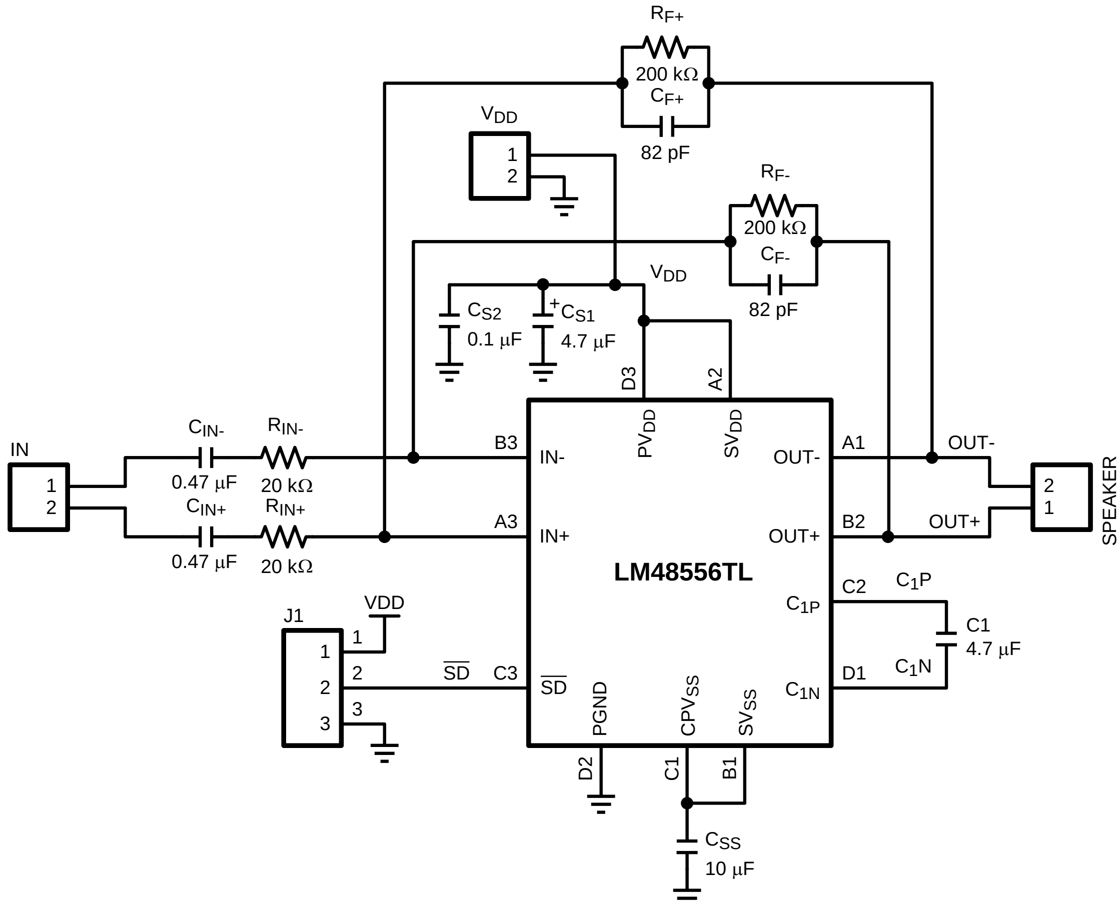


Figure 23. Single-Ended Input Configuration

Bill Of Materials

Component	Description	Designator	Footprint	Quantity
LM48556TL	LM48556TL	LM48556TL	LM48556TL	1
Capacitor	4.7µF, ceramic, low ESR (<0.1Ω) 16V, -40°C to +85°C	C1	CR3216-1206	1
Capacitor	82µF, 16V, -40°C to +85°C	C_{F+}	CR2012-0805	1
Capacitor	82µF, 16V, -40°C to +85°C	C_{F-}	CR2012-0805	1
Capacitor	0.47µF, 16V, -40°C to +85°	C_{IN+}	CR2012-0805	1
Capacitor	0.47µF, 16V, -40°C to +85°C	C_{IN-}	CR2012-0805	1
Capacitor	4.7µF, 16V, -40°C to +85°C	C_{S1}	CR3216-1206	1
Capacitor	0.1µF ceramic, 16V, -40°C to +85°C	C_{S2}	CR2012-0805	1
Capacitor	10µF ceramic, low ESR (<0.1Ω) 16V, -40°C to +85°C	C_{SS}	CR3216-1206	1
Header, 2–Pin	Header 2	IN	HDR1X2	1
Resistor	200kΩ	R_{F+}	CR2012-0805	1
Resistor	200kΩ	R_{F+}	CR2012-0805	1
Resistor	200kΩ	R_{IN+}	CR2012-0805	1
Resistor	200kΩ	R_{IN-}	CR2012-0805	1
Header, 2–Pin	Header 2	SPEAKER	HDR1X2	1
Header, 2–Pin	Header 2	V_{DD}	HDR1X2	1
Header, 3–Pin	3–pole jumper	J1	3–pole jumper	1

Demonstration Board Schematic



Demonstration Board PCB Views

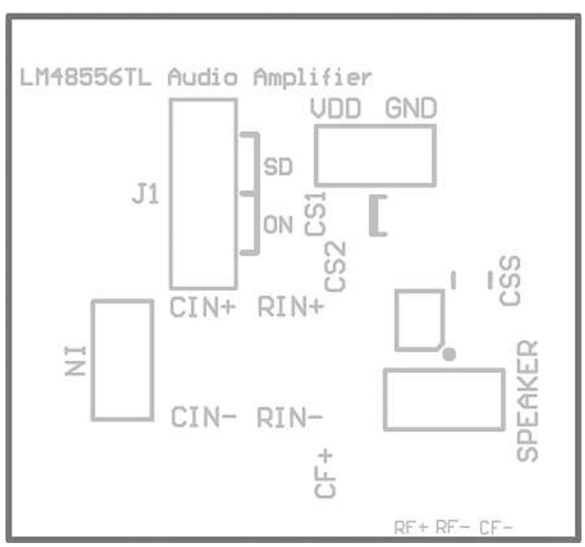


Figure 24. Top Overlay

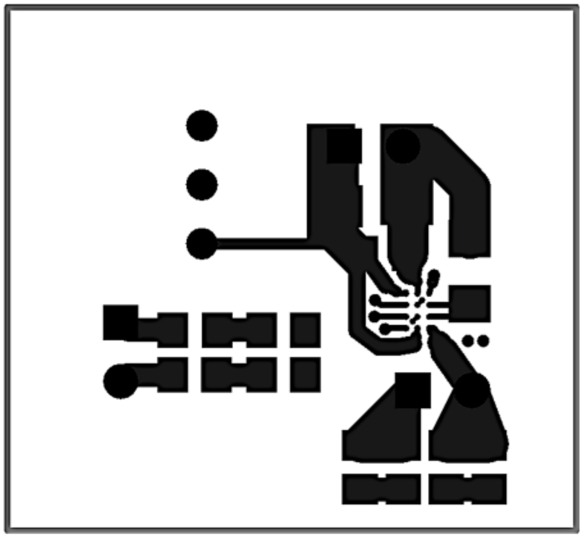


Figure 25. Top Layer

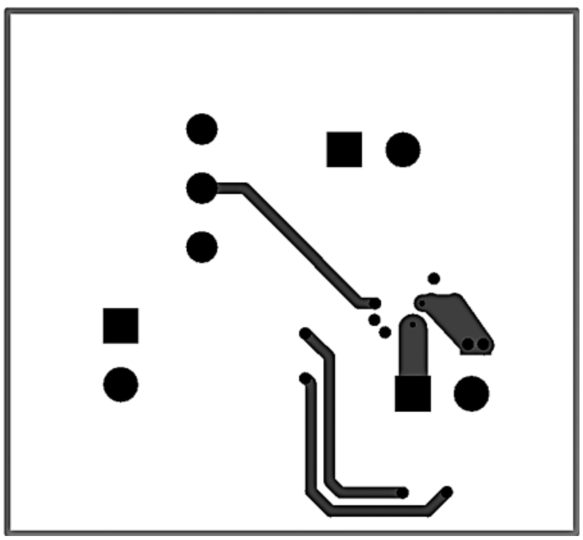


Figure 26. Mid Layer 1

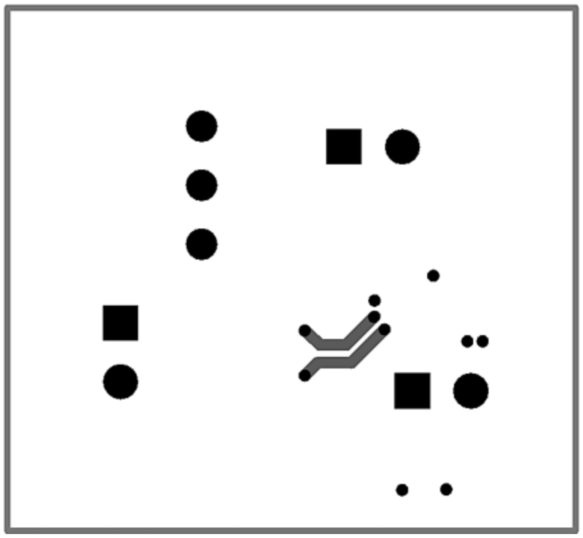


Figure 27. Mid Layer 2

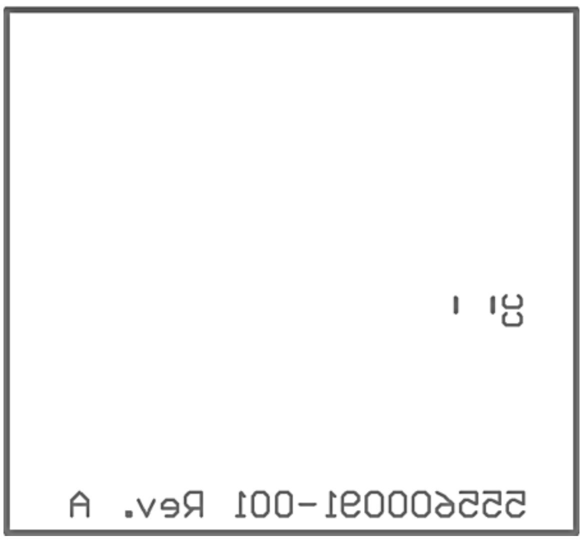


Figure 28. Bottom Overlay

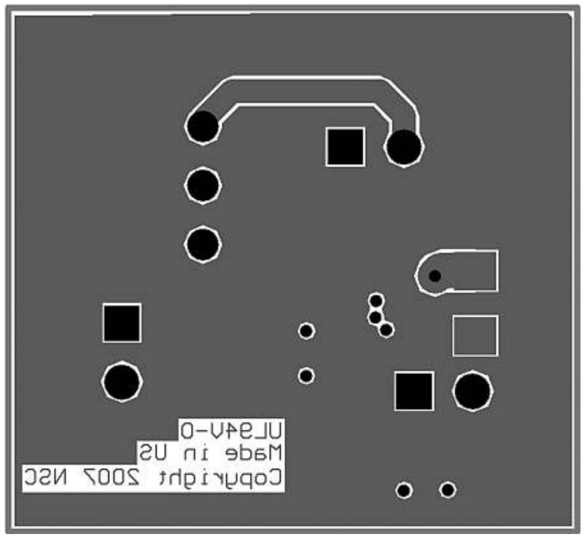


Figure 29. Bottom Layer

REVISION HISTORY

Rev	Date	Description
1.0	06/03/08	Initial release.
1.01	12/09/08	Changed Power Supply Voltage Limits from 4.5V to 5.0V.
B	05/02/2013	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM48556TL/NOPB	ACTIVE	DSBGA	YZR	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		GK4	Samples
LM48556TLX/NOPB	ACTIVE	DSBGA	YZR	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		GK4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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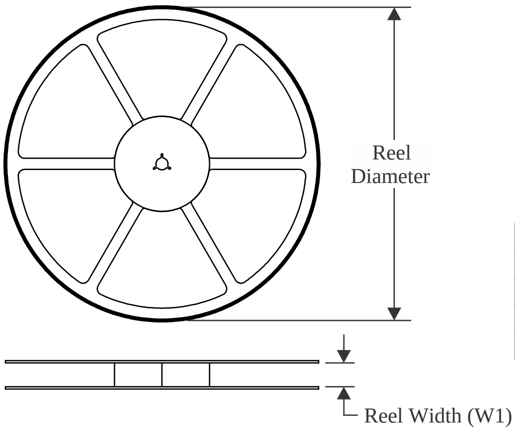
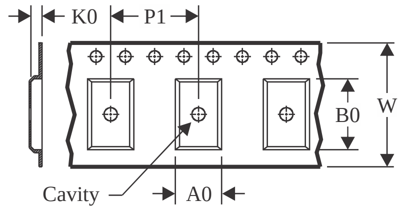
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

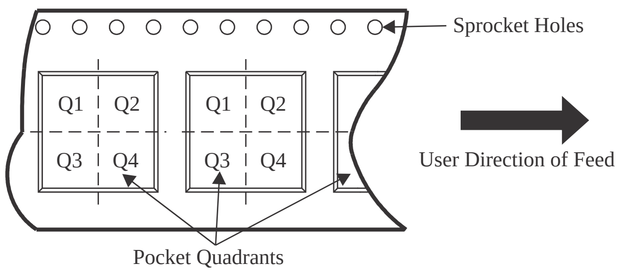


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

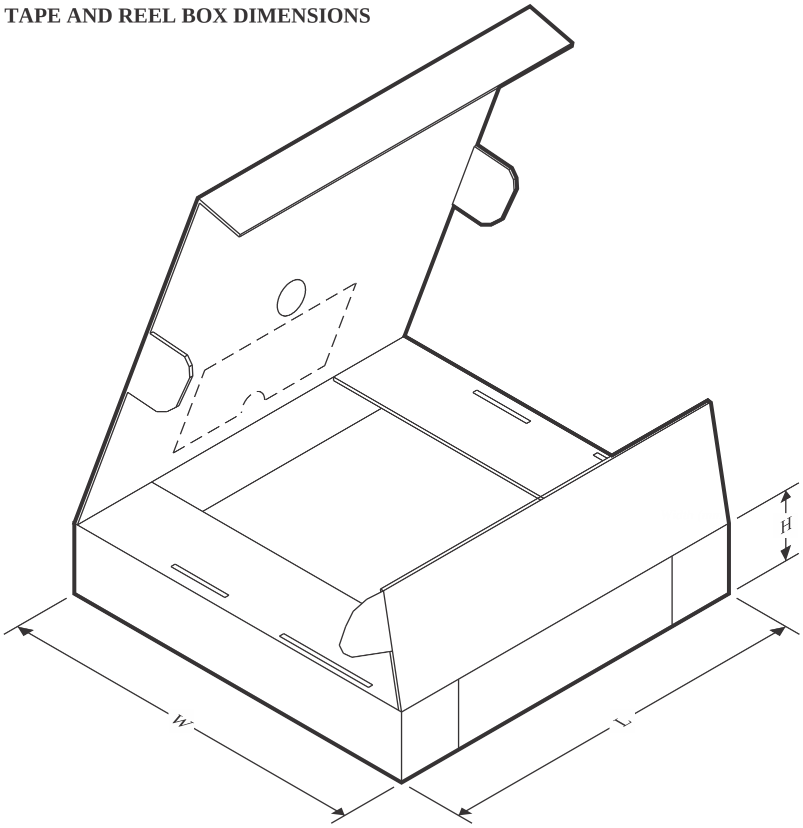
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

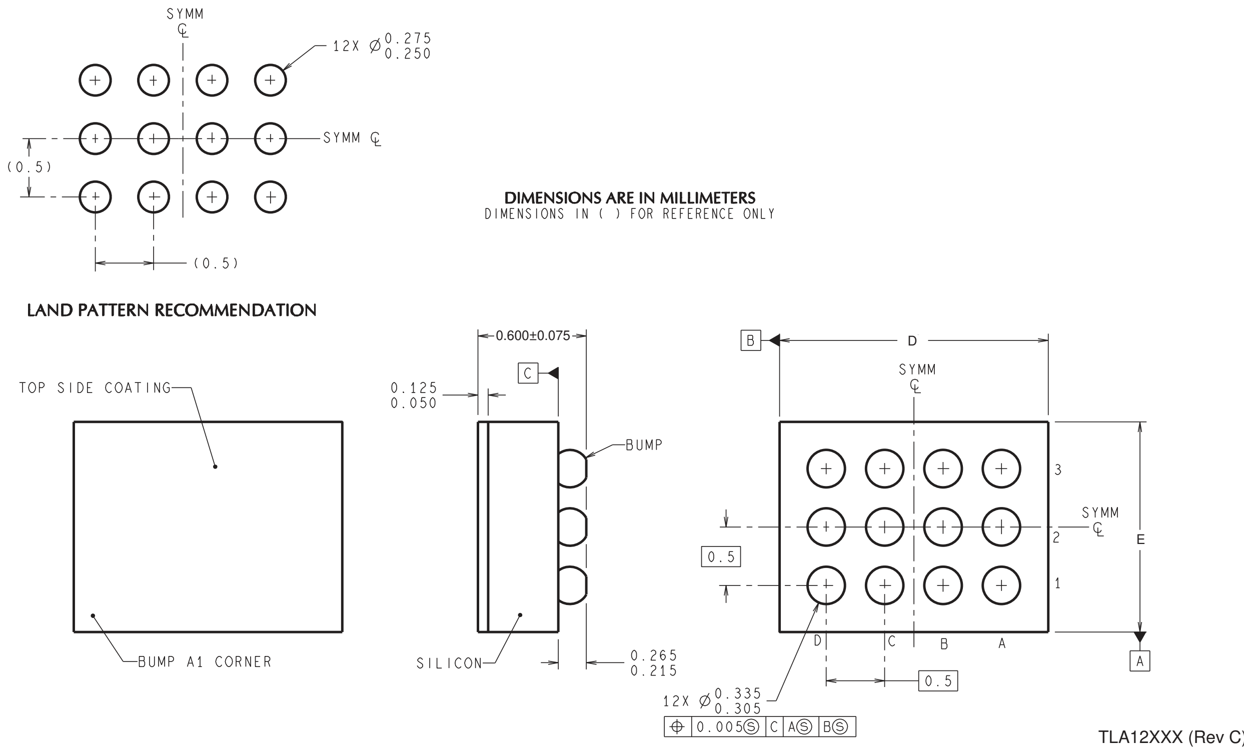
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48556TL/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
LM48556TLX/NOPB	DSBGA	YZR	12	3000	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48556TL/NOPB	DSBGA	YZR	12	250	208.0	191.0	35.0
LM48556TLX/NOPB	DSBGA	YZR	12	3000	208.0	191.0	35.0



D: Max = 2.012 mm, Min =1.951 mm

E: Max = 1.512 mm, Min =1.452 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.