



# PSMN1R0-30YLD

N-channel 30 V, 1.0 m $\Omega$ , 300 A logic level MOSFET in LFAK56 using NextPowerS3 Technology

21 April 2023

Product data sheet

## 1. General description

300 Amp Logic level gate drive N-channel enhancement mode MOSFET in LFAK56 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

## 2. Features and benefits

- 300 Amp capability
- Avalanche rated, 100 % tested at  $I_{(as)} = 190$  Amps
- Ultra low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor  $> 1$
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with  $< 1 \mu A$  leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

## 3. About product line

## 4. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control
- Power OR-ing

## 5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$		-	-	30	V
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	[1]	-	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>		-	-	238	W
$T_j$	junction temperature			-55	-	175	°C

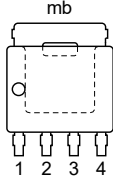
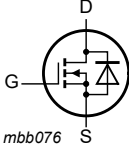
N-channel 30 V, 1.0 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	1	1.3	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 150 °C; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	2.15	mΩ
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	10.9	16.35	nC
Q <sub>G(tot)</sub>	total gate charge		-	38.2	57.3	nC
<b>Source-drain diode</b>						
S	softness factor	I <sub>S</sub> = 25 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 15 V; <a href="#">Fig. 16</a>	-	0.95	-	

[1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, Thermal design and operating temperature.

## 6. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076 S</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 7. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-30YLD	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 8. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-30YLD	1D030L

## 9. Limiting values

Table 5. Limiting values

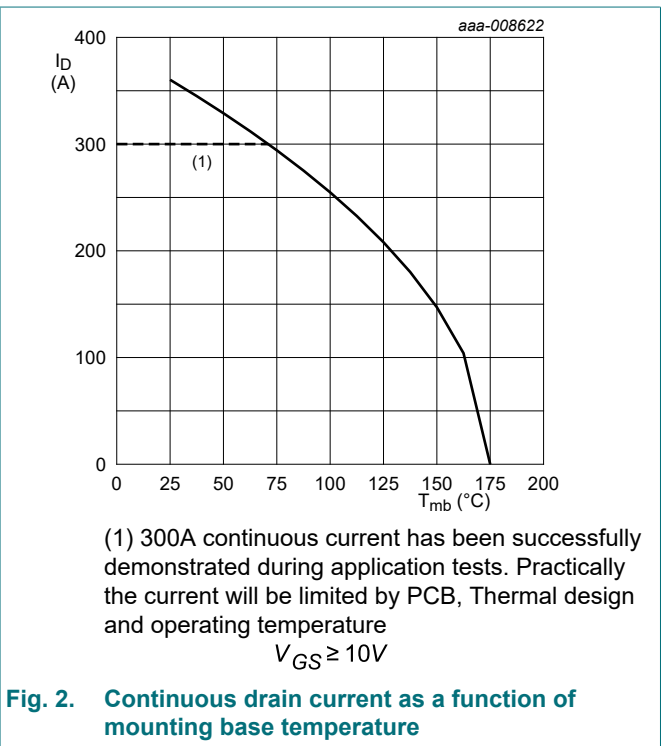
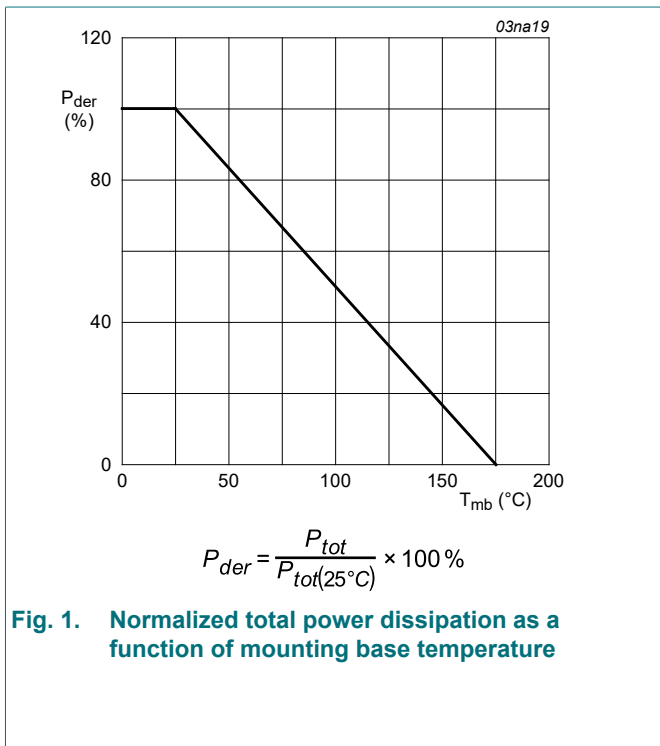
In accordance with the Absolute Maximum Rating System (IEC 60134).

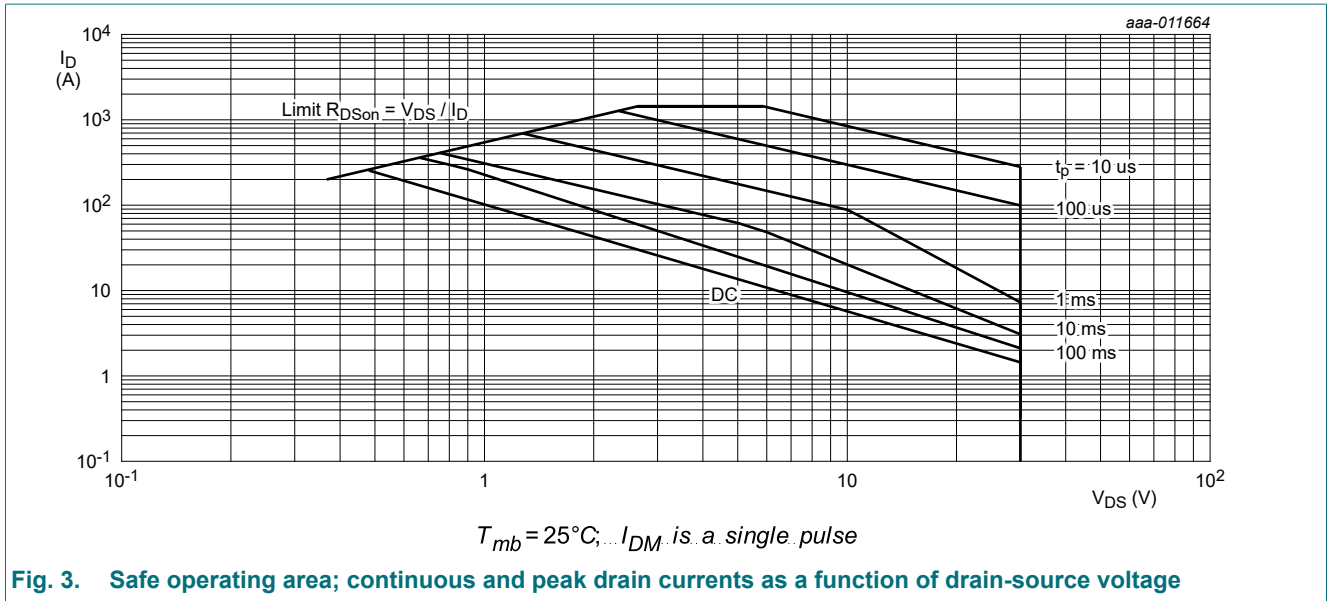
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	30	V

N-channel 30 V, 1.0 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ		-	30	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1		-	238	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2	[1]	-	300	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2		-	255	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3		-	1441	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature			-	260	°C
V <sub>ESD</sub>	electrostatic discharge voltage	human body model		1500	-	V
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	198	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1441	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 25 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 5.1 ms	[2]	-	2491	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 30 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω	[2]	-	190	A

- [1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, Thermal design and operating temperature.
- [2] Protected by 100% test

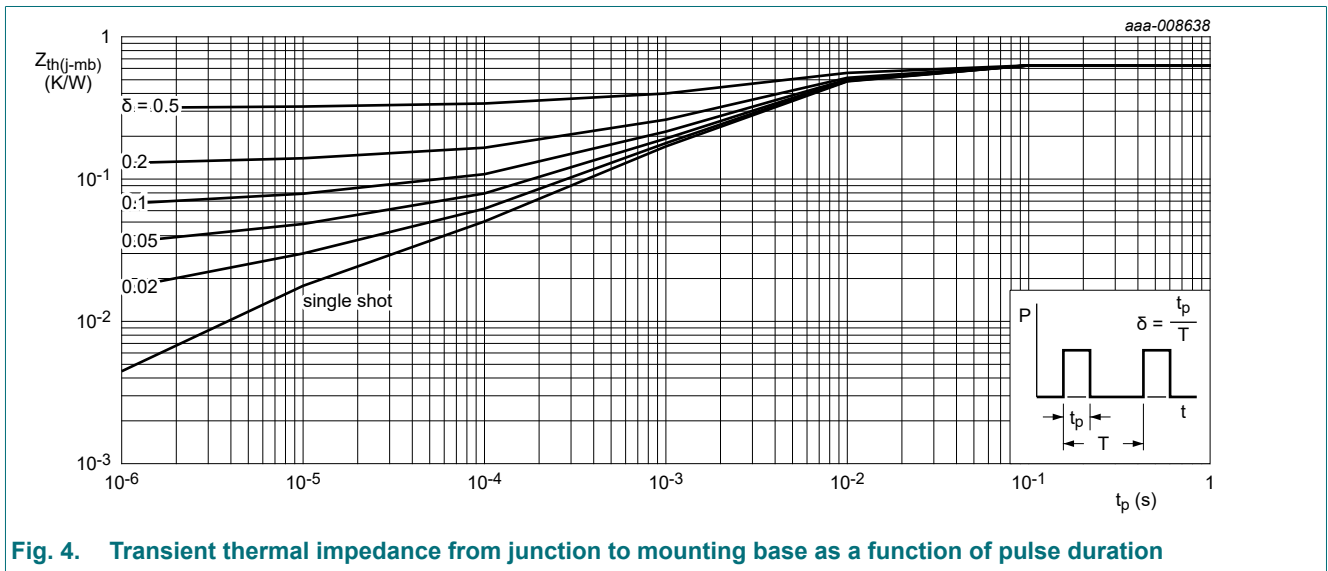


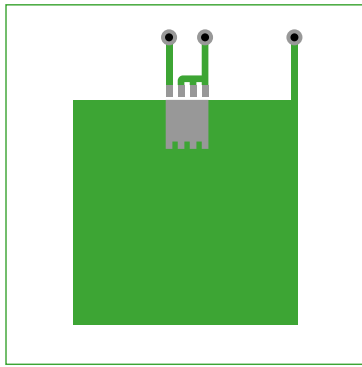


### 10. Thermal characteristics

Table 6. Thermal characteristics

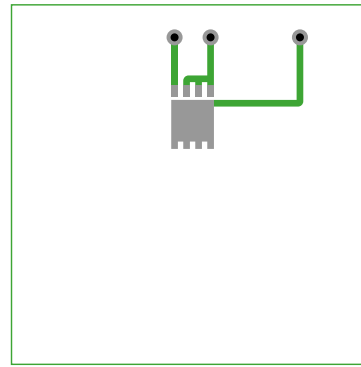
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	125	-	K/W





aaa-005750

Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper



aaa-005751

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint;FR4 board; 2oz copper

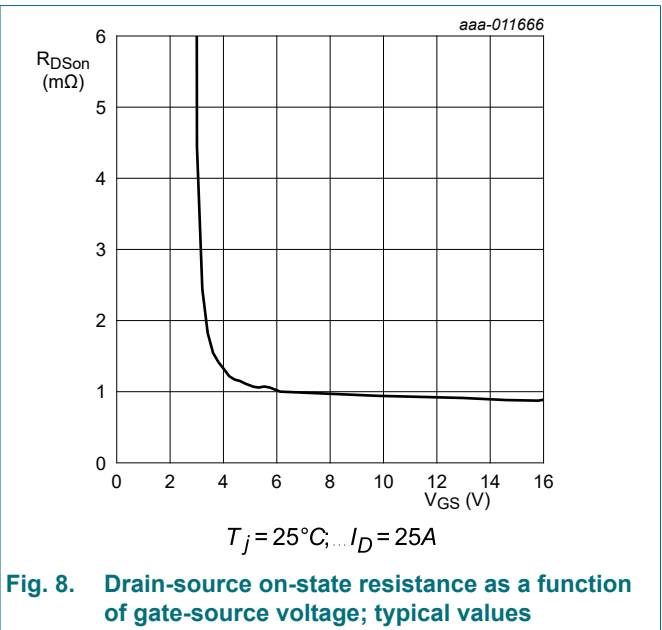
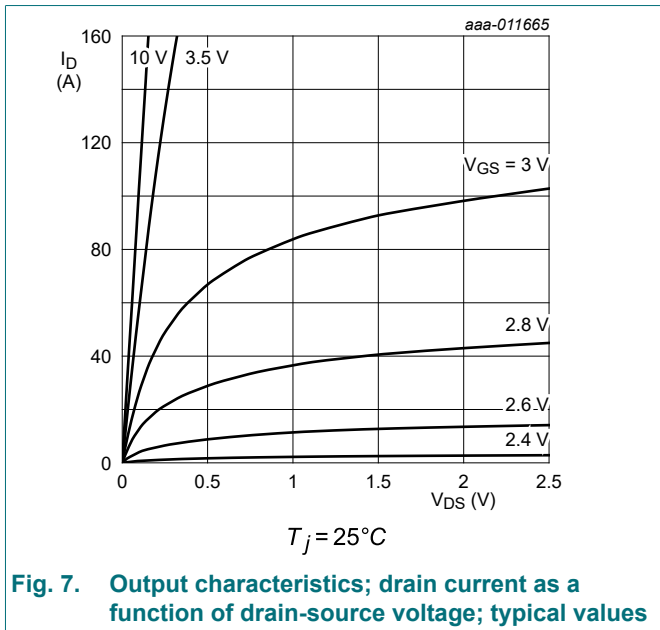
## 11. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.75	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.9	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	2.8	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	1	1.3	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	2.15	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	0.79	1.02	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	1.7	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.22	2.44	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	80.9	121.35	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	38.2	57.3	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	72	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	12.5	-	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		-	7.8	-	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.7	-	nC	
$Q_{GD}$	gate-drain charge		-	10.9	16.35	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 15\text{ V};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.6	-	V	
$C_{iss}$	input capacitance	$V_{DS} = 15\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	-	5732	8598	pF	
$C_{oss}$	output capacitance		-	2424	3636	pF	
$C_{rss}$	reverse transfer capacitance		-	340	510	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 1\text{ }^\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }^\Omega$	-	32.4	-	ns	
$t_r$	rise time		-	44.4	-	ns	
$t_{d(off)}$	turn-off delay time		-	43	-	ns	
$t_f$	fall time		-	31.7	-	ns	
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	55.9	-	nC	
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	0.77	1.2	V	
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 15\text{ V};$ <a href="#">Fig. 16</a>	-	51.8	103.6	ns	
$Q_r$	recovered charge		[1]	-	67.1	134.2	nC
$t_a$	reverse recovery rise time		-	-	26.5	-	ns
$t_b$	reverse recovery fall time		-	-	25.3	-	ns
S	softness factor		-	-	0.95	-	

[1] includes capacitive recovery



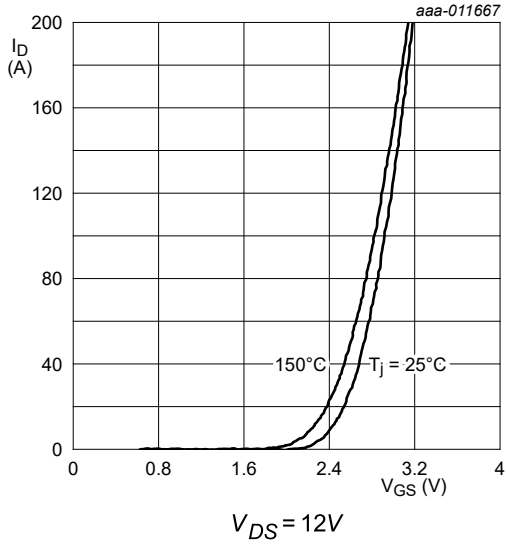


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

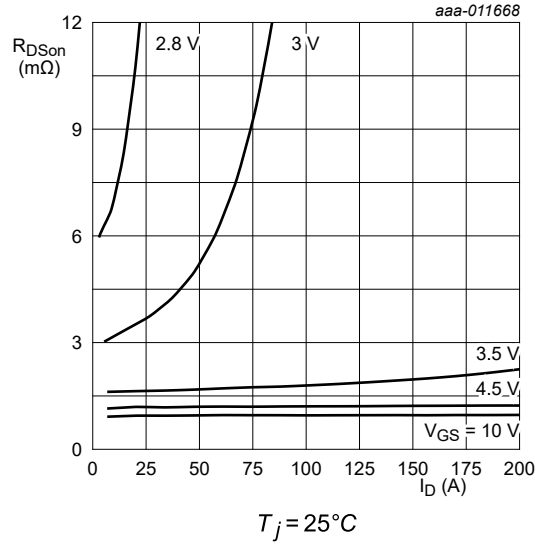


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

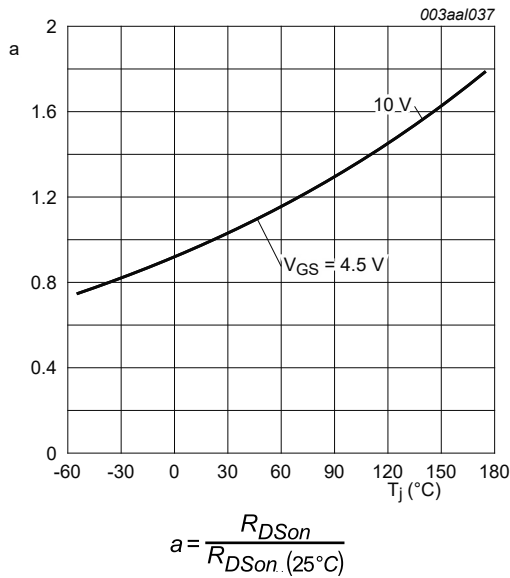


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

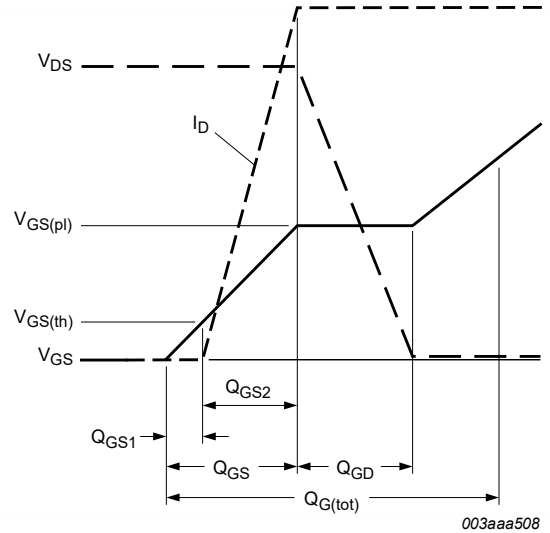


Fig. 12. Gate charge waveform definitions

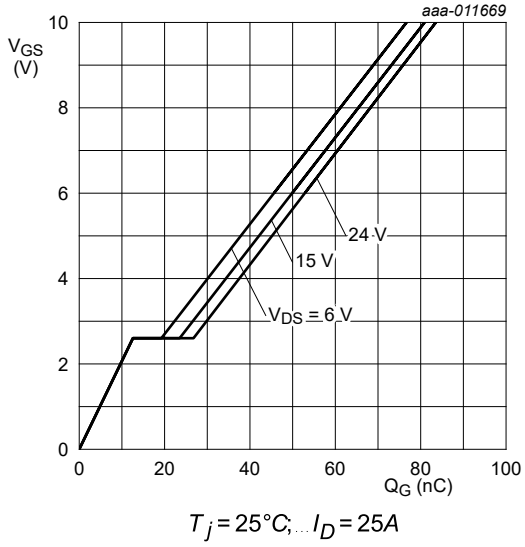


Fig. 13. Gate-source voltage as a function of gate charge; typical values

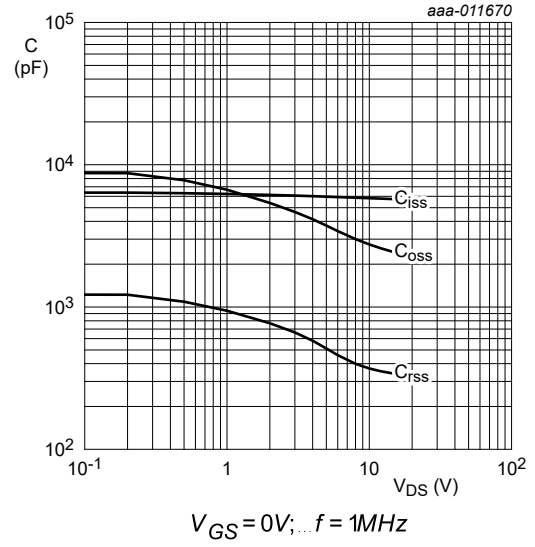


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

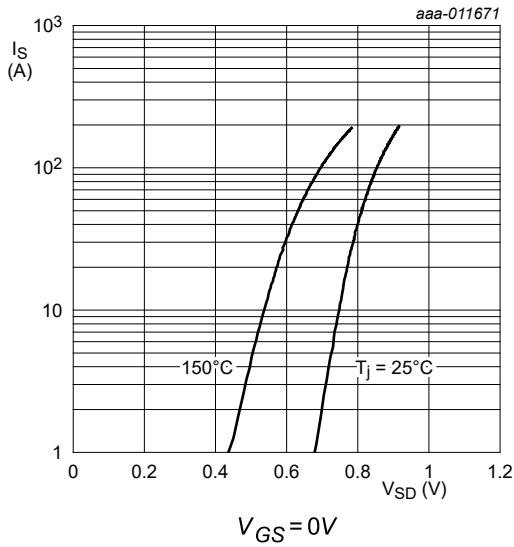


Fig. 15. Source current as a function of source-drain voltage; typical values

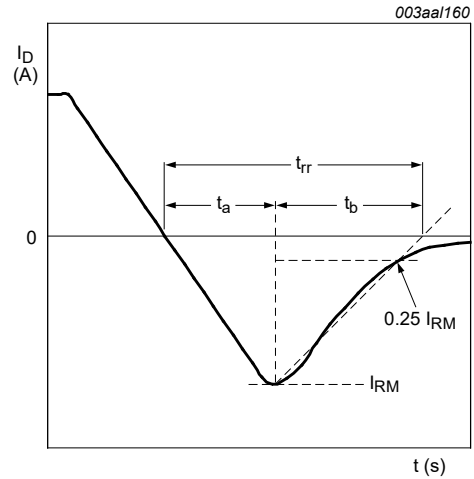


Fig. 16. Reverse recovery timing definition



## 12. Package outline

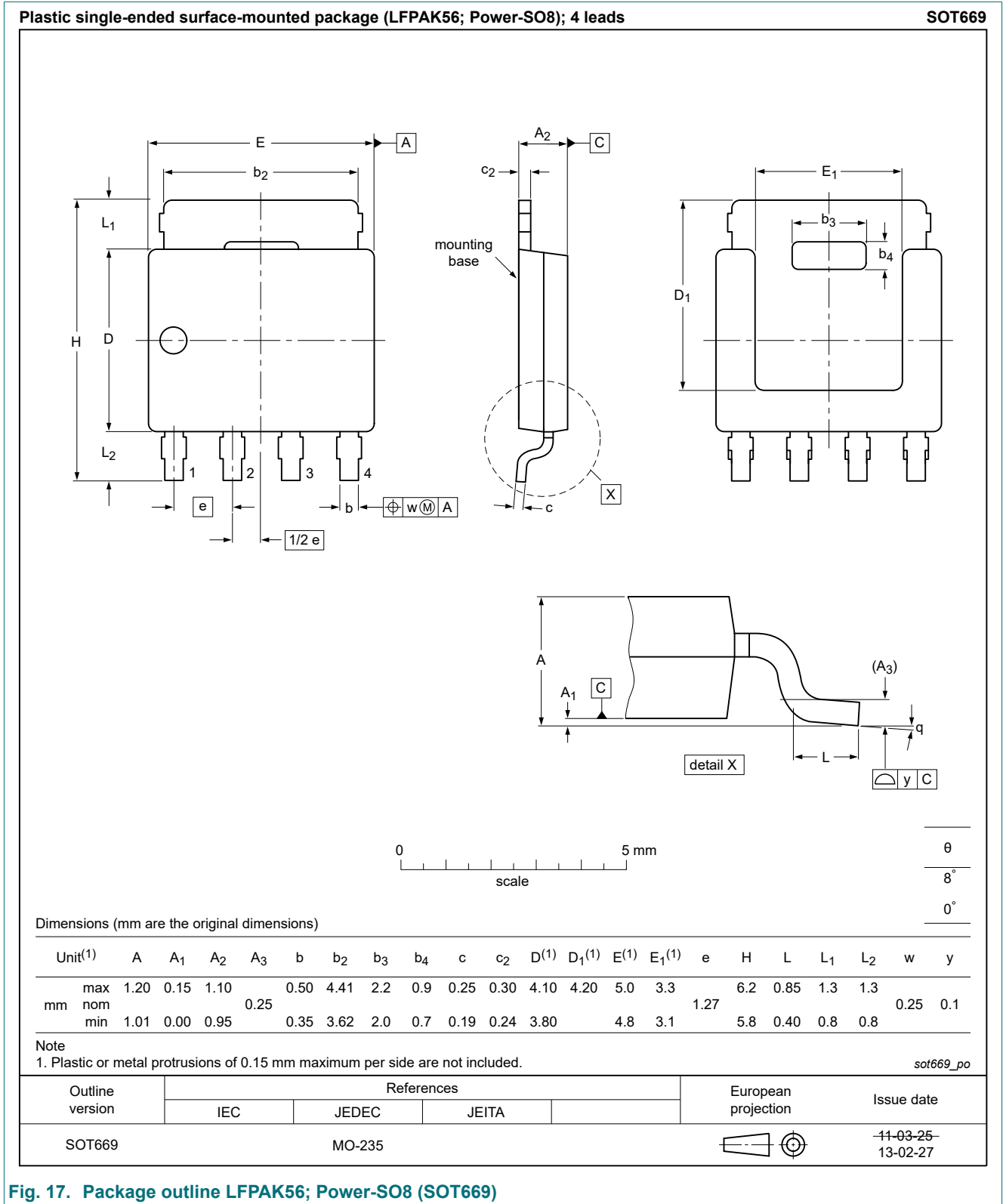


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

### 13. Soldering

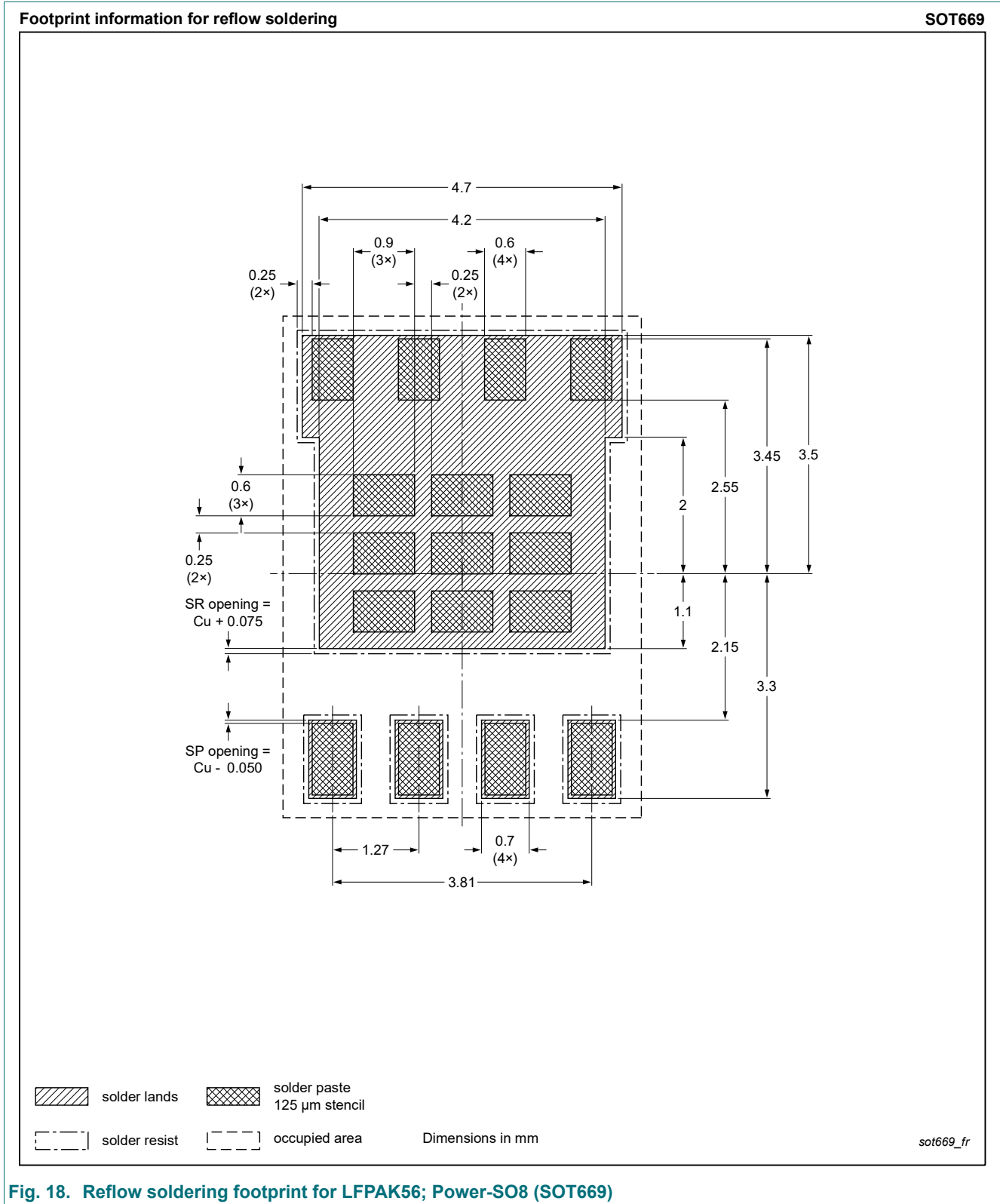
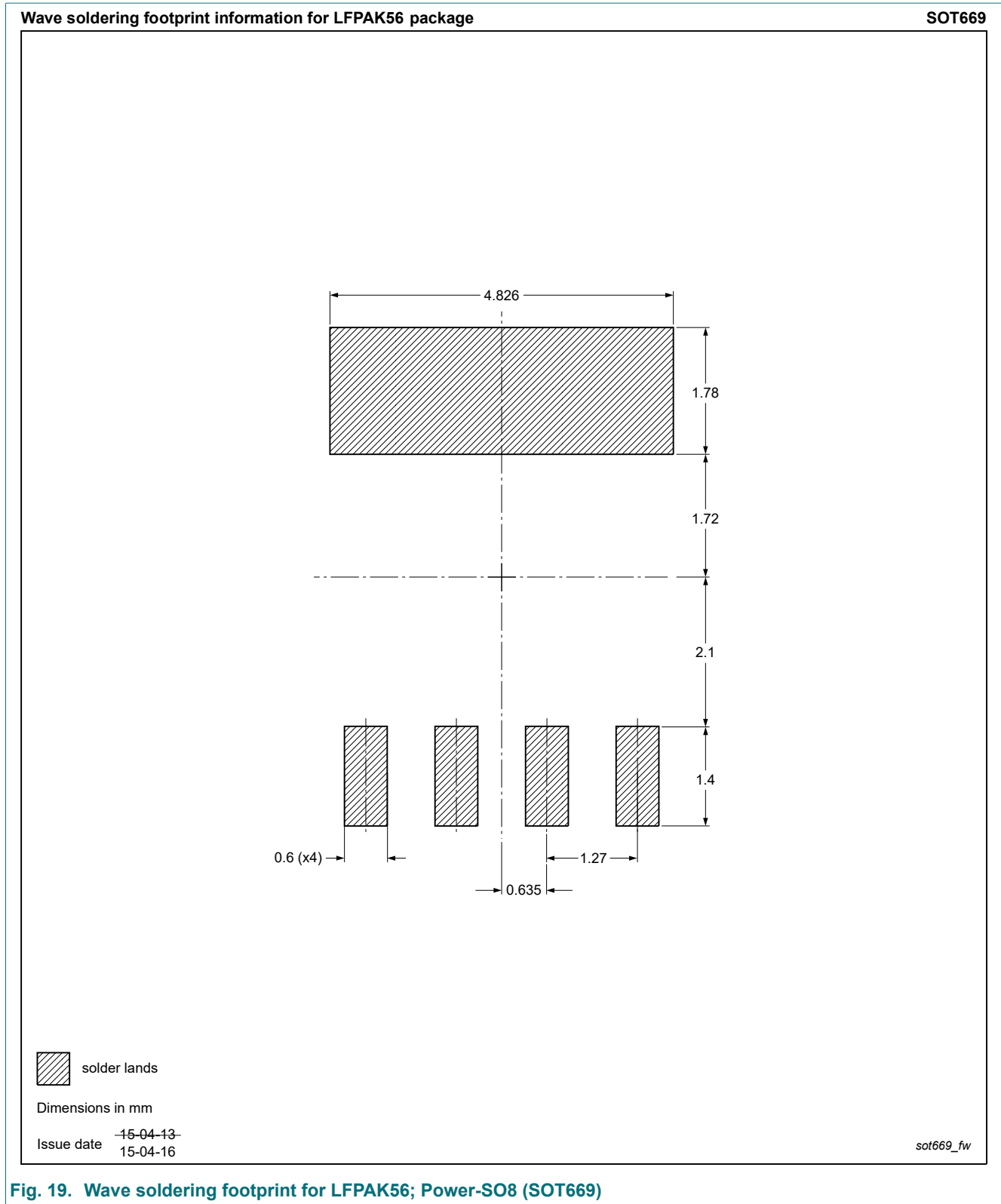


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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