

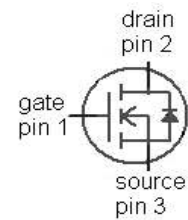
OptiMOS[®] -T Power-Transistor

Product Summary

V_{DS}	55	V
$R_{DS(on),max}$	7.8	m Ω
I_D	50	A

Features

- N-channel - Logic Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

PG-TO252-3-11


Type	Package	Marking
IPD50N06S3L-08	PG-TO252-3-11	3N06L08

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	50	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	50	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=25\text{ A}$	370	mJ
Avalanche current, single pulse	I_{AS}		50	A
Gate source voltage ³⁾	V_{GS}		± 16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	107	W
Operating and storage temperature	T_j, T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}		-	-	1.4	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁴⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=55\text{ }\mu\text{A}$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=16\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=5\text{ V}, I_D=29\text{ A}$	-	11.2	14	m Ω
		$V_{GS}=10\text{ V}, I_D=43\text{ A}$	-	6.4	7.8	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	6475	7450	pF
Output capacitance	C_{oss}		-	812	1220	
Reverse transfer capacitance	C_{rss}		-	775	1160	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=27.5\text{ V},$ $V_{GS}=10\text{ V}, I_D=50\text{ A},$ $R_G=5.1\ \Omega$	-	17	-	ns
Rise time	t_r		-	43	-	
Turn-off delay time	$t_{d(off)}$		-	47	-	
Fall time	t_f		-	50	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=11\text{ V}, I_D=50\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	30	40	nC
Gate to drain charge	Q_{gd}		-	17	26	
Gate charge total	Q_g		-	90	110	
Gate plateau voltage	$V_{plateau}$		-	4.3	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	50	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	0.6	0.9	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	40	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	50	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 1.4\text{ K/W}$ the chip is able to carry 87 A at 25°C. For detailed information see Application Note ANPS071E.

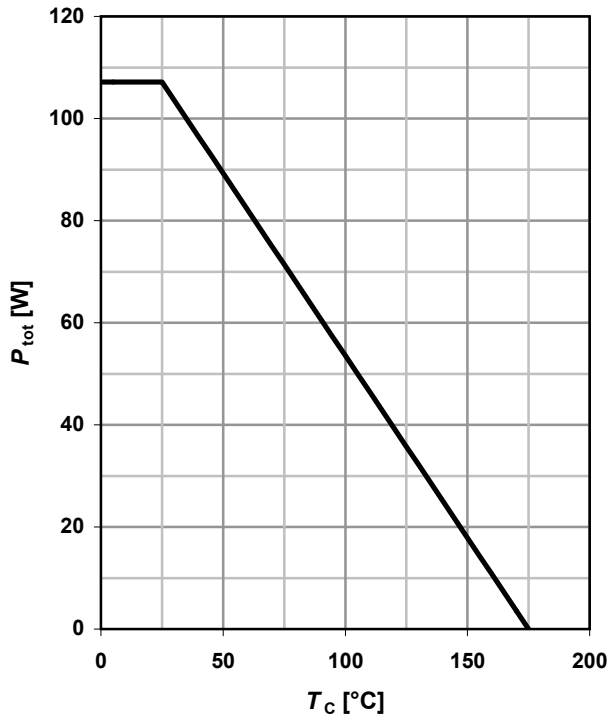
²⁾ Defined by design. Not subject to production test.

³⁾ Qualified at -5V and +20V.

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

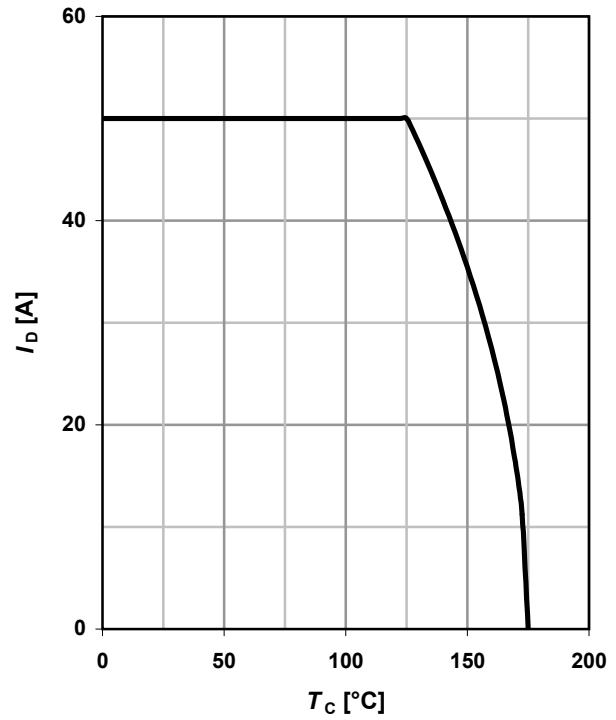
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6 V$



2 Drain current

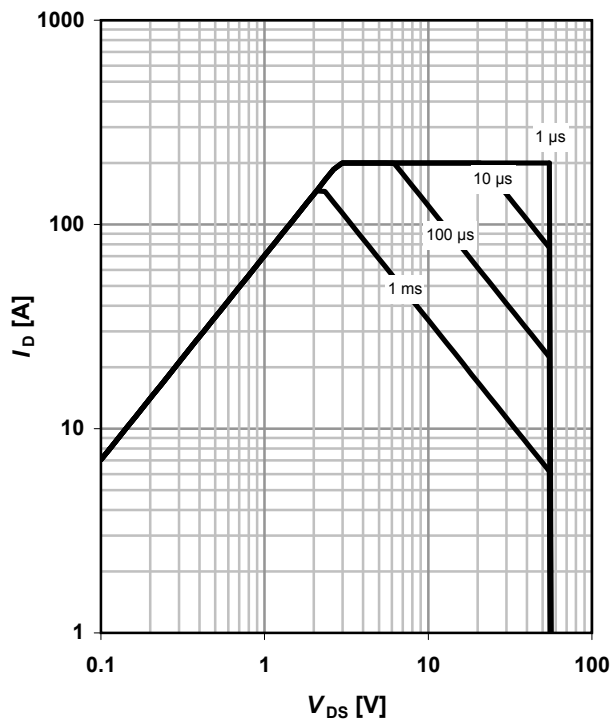
$I_D = f(T_C); V_{GS} \geq 6 V$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

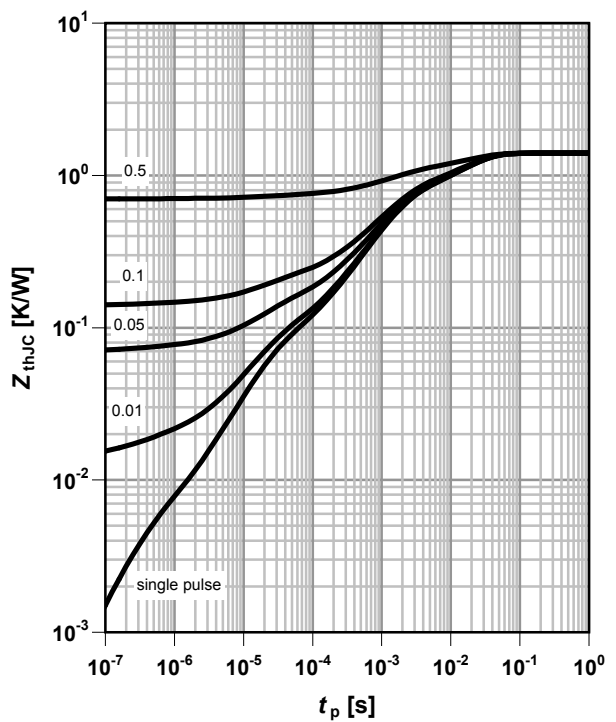
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

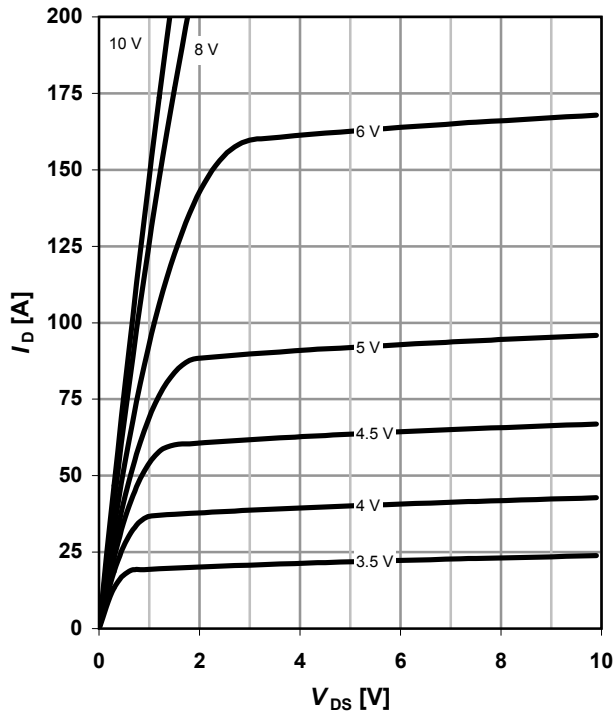
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

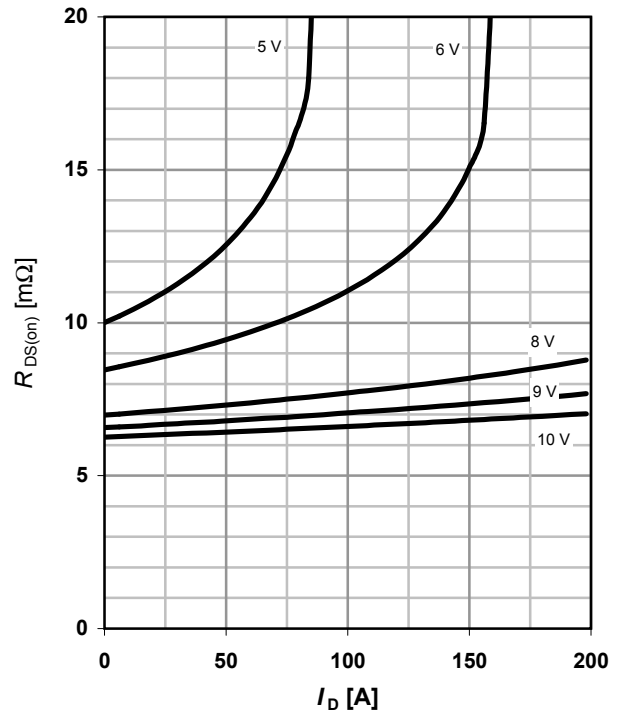
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

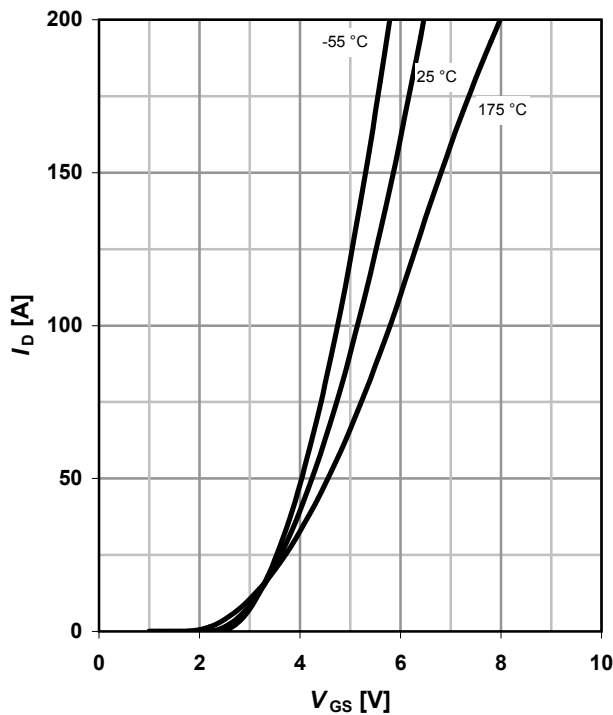
parameter: V_{GS}



7 Typ. transfer characteristics

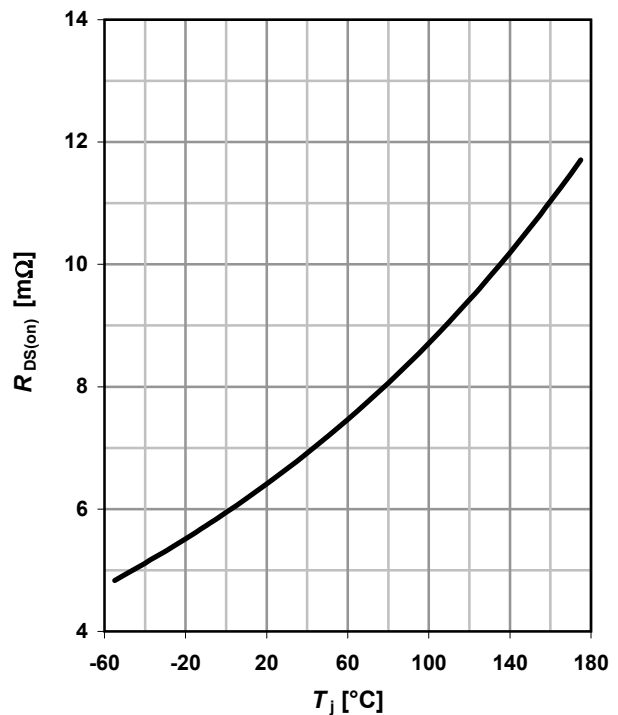
$I_D = f(V_{GS}); V_{DS} = 4\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance

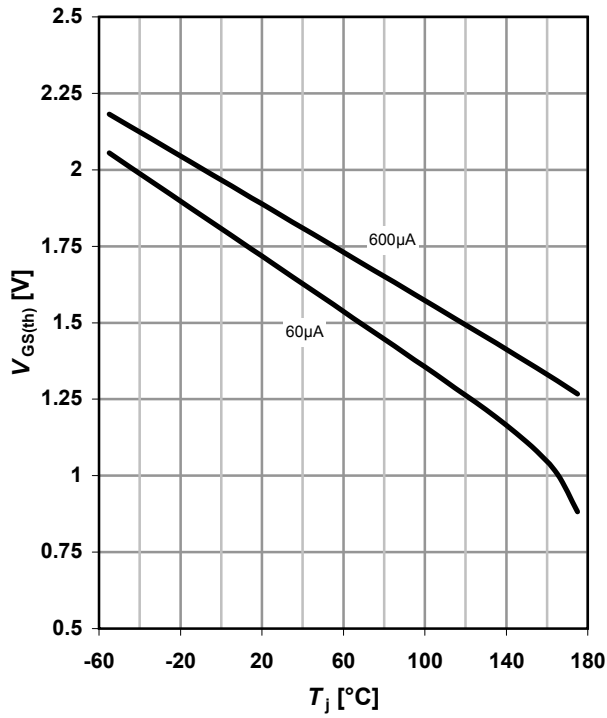
$R_{DS(on)} = f(T_j); I_D = 43\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

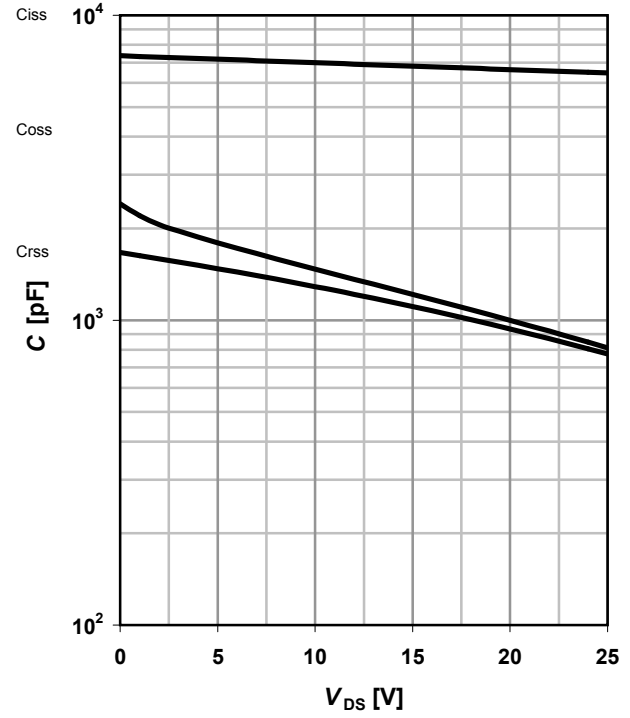
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

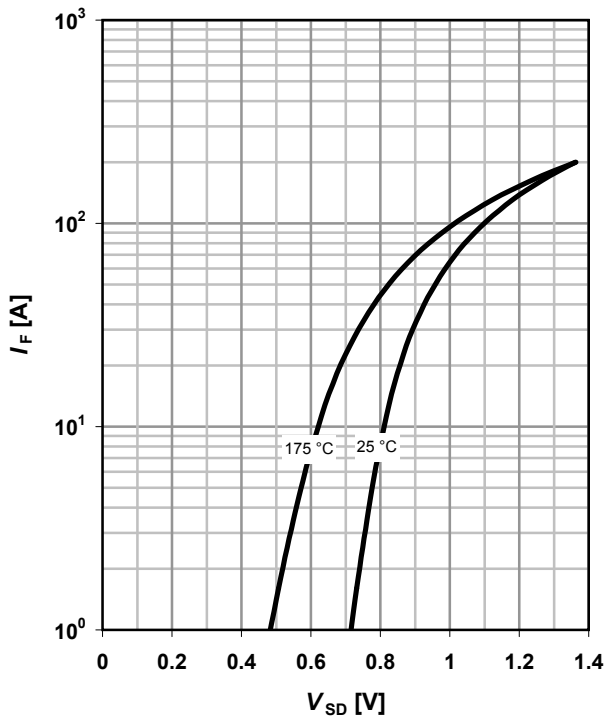
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

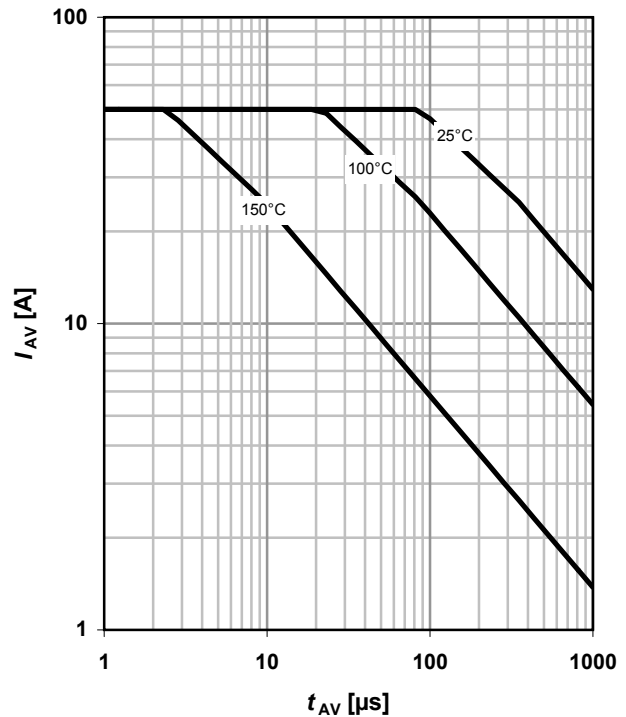
parameter: T_j



12 Typ. avalanche characteristics

$I_{AV} = f(t_{AV})$

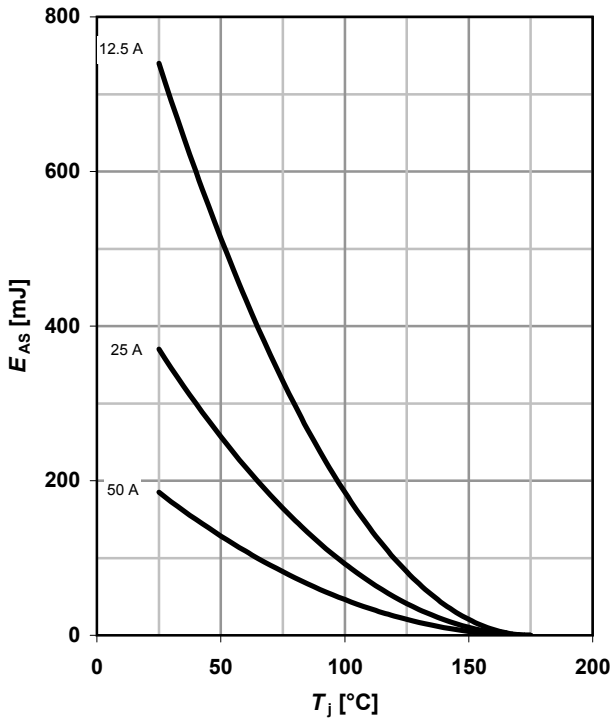
parameter: $T_{j(start)}$



13 Typical avalanche Energy

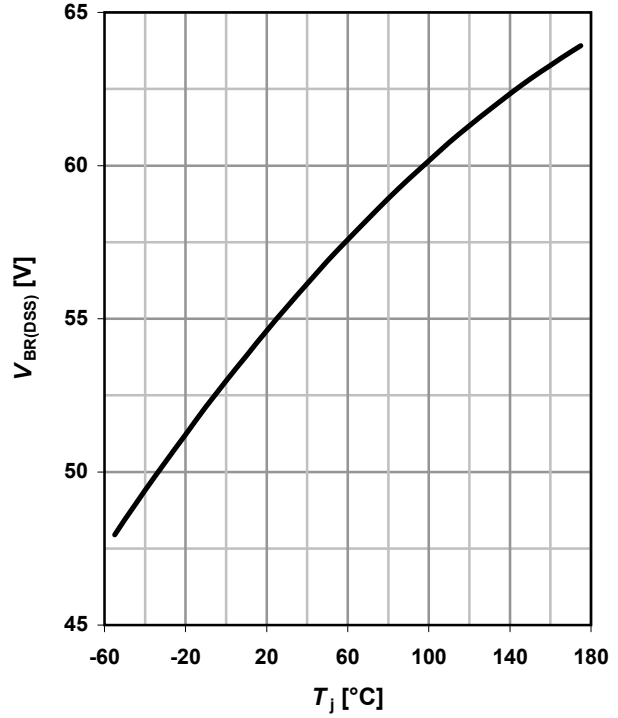
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

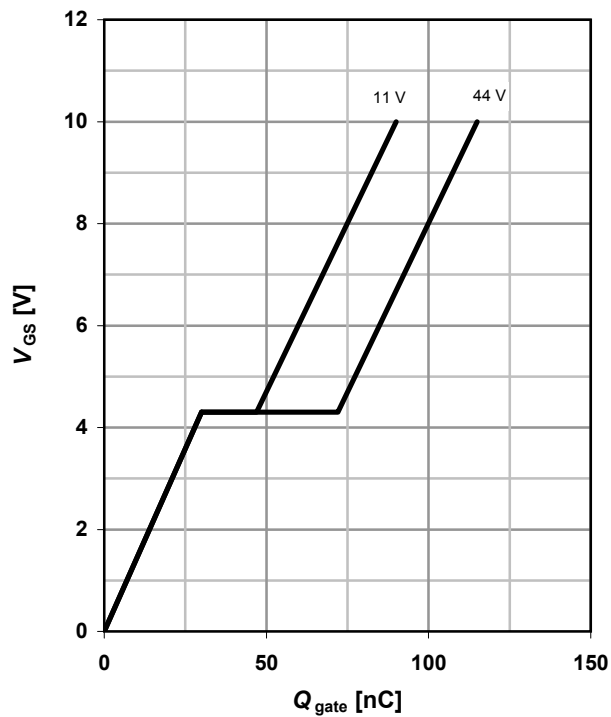
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



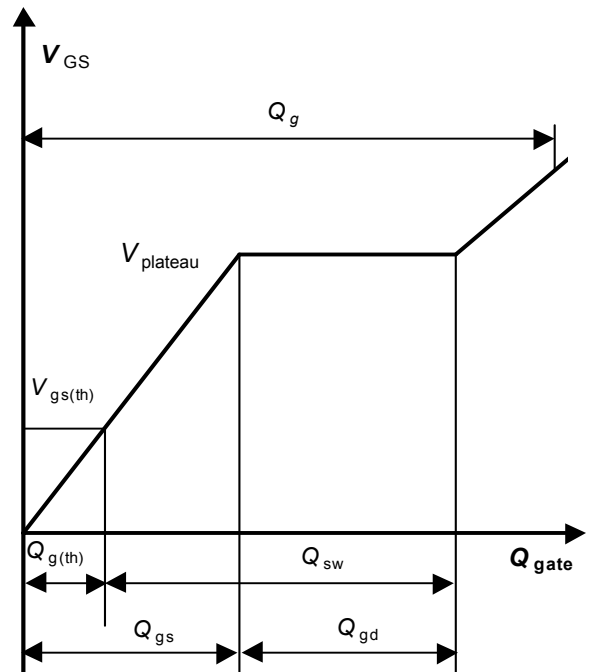
15 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Data Sheet version 1.1	15.06.2009	Correction of marking and update of disclaimer
Data Sheet version 1.1	15.06.2009	Correction of package name