Evaluating the ADPA1106 46 dBm (40 W), 2.7 GHz to 3.5 GHz, GaN Power Amplifier

FEATURES

- 2-layer Rogers 4350B evaluation board with heat spreader
- End launch SMA jack RF connectors
- Through calibration path
- Drain or gate pulsing capability

EVALUATION KIT CONTENTS

- ADPA1106-EVALZ evaluation board
- 50 V drain pulser board

EQUIPMENT NEEDED

- Pulse generator
- Oscilloscope
- 50 V, 2 A power supply
- −4 V power supply
- Tektronix TCPA312A current probe
- Tektronix TCPA300 current probe amplifier
- RF signal generator
- Directional coupler
- RF power sensor
- RF power meter
- RF attenuator

DOCUMENTS NEEDED

- ADPA1106 data sheet

GENERAL DESCRIPTION

The ADPA1106-EVALZ consists of a 2-layer printed circuit board (PCB) fabricated from a 10 mil thick, Rogers 4350B copper clad mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow the spreader to be attached to a heat sink. Alternatively, the spreader can be clamped to a hot and cold plate. The RFIN and RFOUT ports on the ADPA1106-EVALZ are populated by Subminiature Version A (SMA) female coaxial connectors, and the respective RF traces have a 50 Ω characteristic impedance. The ADPA1106-EVALZ is populated with components suitable for use over the entire operating temperature range of the device. To calibrate board trace losses, a through calibration path is provided between the J6 and J5 connectors. J6 and J5 must be populated with SMA RF connectors to use the through calibration path.

Ground, power, gate control, and the detector output voltage are provided through the two 24-pin headers (P4 and P5) on the ADPA1106-EVALZ. The pinouts for these two headers are shown in Table 1.

RF traces on the ADPA1106-EVALZ are 50 Ω, grounded, coplanar waveguide. The package ground leads and the exposed paddle connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground pad to provide adequate electrical conduction and thermal conduction to the heat spreader.

The ADPA1106-EVALZ ships with a drain pulser board that can be plugged into the ADPA1106-EVALZ headers and configured to control the biasing of the ADPA1106 by providing a negative gate voltage and a control signal that connects and disconnects the drain voltage to the ADPA1106-EVALZ. The ADPA1106-EVALZ can also operate alone in gate pulsed mode where a negative pulse is applied to the VGG1 and VGG2 pins of the ADPA1106.

For full details on the ADPA1106, see the ADPA1106 data sheet, which must be consulted in conjunction with this user guide when using the ADPA1106-EVALZ.

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REVISION HISTORY

4/2022—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

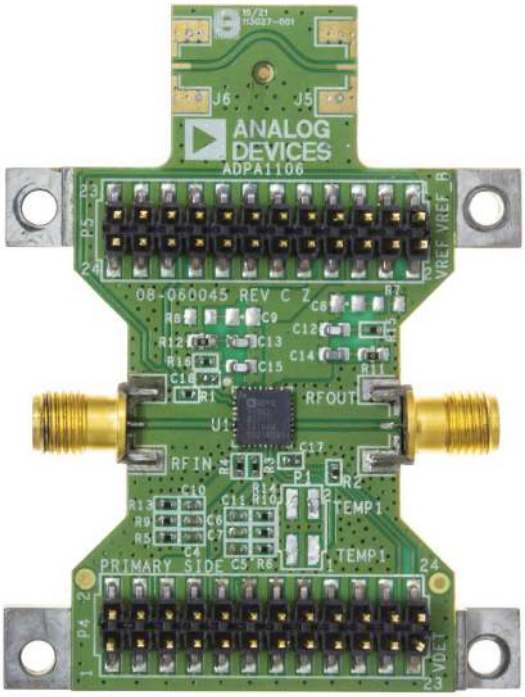

Figure 1. ADPA1106-EVALZ Evaluation Board, Primary Side

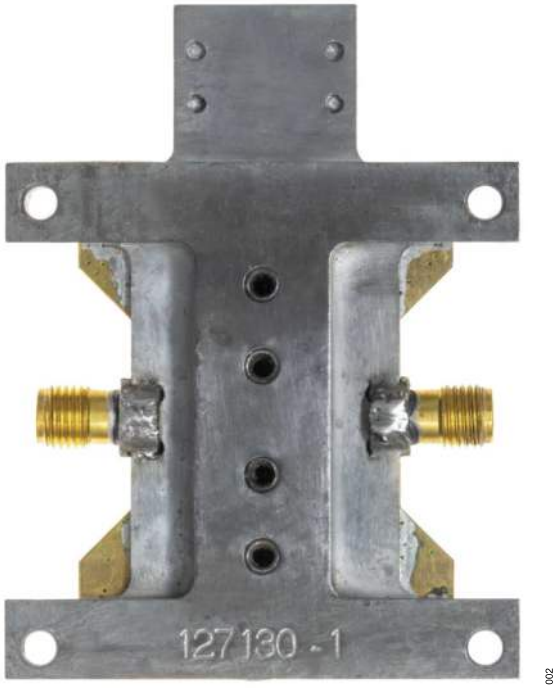

Figure 2. ADPA1106-EVALZ Evaluation Board, Secondary Side

HEADER PINOUT

The schematic for the ADPA1106-EVALZ is shown in Figure 6. The ADPA1106-EVALZ contains two headers, P4 and P5. Table 1 describes the pinout of these headers.

Table 1. P4 and P5 Header Connections on the ADPA1106-EVALZ

Header	Header Pin Number	Header Pin Name
P4	1 to 5, 7, 9, 11 to 17, 19, 21	GND
	6, 8	VGG1
	10	VGG2
	18, 20, 22	Not connected
	23	VDET
	24	VDET_BIAS
P5	1	VREF
	2	VREF_BIAS
	3, 5, 7, 9 to 15, 17, 19, 21 to 24	GND
	4, 6	VDD2
	8	VDD1
	16, 18, 20	Not connected

INSERTION LOSS OF THE THROUGH CALIBRATION PATH

To calibrate board trace losses, a through calibration path is provided between the J6 and J5 connectors. J6 and J5 must be populated with SMA RF connectors to use the through calibration path. Figure 3 shows the insertion loss, input return loss, and output return loss of the through calibration path. Table 2 lists the insertion loss of the through path vs. frequency.

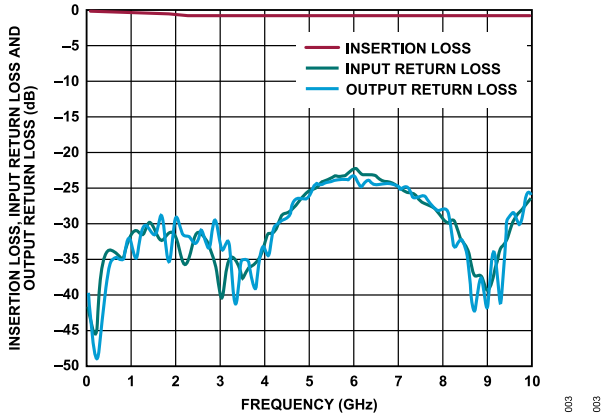

Figure 3. Insertion Loss, Input Return Loss, and Output Return Loss of Through Calibration Path

Table 2. Insertion Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
1	−0.24
2	−0.36
3	−0.48
4	−0.45
5	−0.5
6	−0.55
7	−0.61
8	−0.64
9	−0.65
10	−0.65

OPERATING THE ADPA1106-EVALZ WITH A PULSED GATE VOLTAGE

To implement gate pulsed operation, apply a negative voltage pulse to the VGG1 and VGG2 inputs of the ADPA1106 while the voltage on the VDD1 and VDD2 pins of the ADPA1106 is held constant.

SETUP

All power supply, ground, and control signals are applied to the P4 and P5 headers of the ADPA1106-EVALZ. For this mode of operation, pulse the gate voltage between −4 V (off) and approximately −2.3 V (on) to set the quiescent current (I_{DQ}) to approximately 300 mA. The pulse width and duty cycle must be approximately 100 µs and 10%, respectively.

OPERATION

Take the following steps to power up the ADPA1106-EVALZ:

1. Set VDDx (Pin 4, Pin 6, and Pin 8 of P5) to 0 V.
2. Set VGGx (Pin 6, Pin 8, and Pin 10 of P4) to off (VGG1 = VGG2 = −4 V).
3. Set the supply voltage (V_{DD}) to 50 V.
4. Turn on the gate voltage pulse (VGG1 and VGG2 pulsing between −4 V and approximately −2.3 V).
5. Fine tune the pulse high voltage to achieve the desired I_{DQ} (nominally 300 mA) while maintaining the pulse off voltage level at −4 V.
6. Apply the RF input signal.

Take the following steps to power down the ADPA1106-EVALZ:

1. Turn off the RF signal.
2. Turn off the pulse to VGG1 and VGG2 (VGG1 = VGG2 = −4 V).
3. Set V_{DD} to 0 V.
4. Increase the pulse to VGG1 and VGG2 to 0 V.

OPERATING THE ADPA1106-EVALZ WITH THE DRAIN BIAS PULSER BOARD

The ADPA1106-EVALZ ships with a drain bias pulser board. A block diagram of the pulser board is shown in Figure 4. The pulser board has two primary components. The BSC340N08NS3 is an 80 V/ 23 A, metal-oxide semiconductor field effect transistor (MOSFET) that switches the drain voltage to the ADPA1106 on and off, and the LTC7000 is a high-side, negative channel metal-oxide semiconductor (NMOS), static switch driver that controls the MOSFET.

The pulser board plugs into the P4 and P5 headers of ADPA1106-EVALZ and can be configured to provide a pulsed drain voltage and a negative gate control voltage to control the biasing of the ADPA1106.

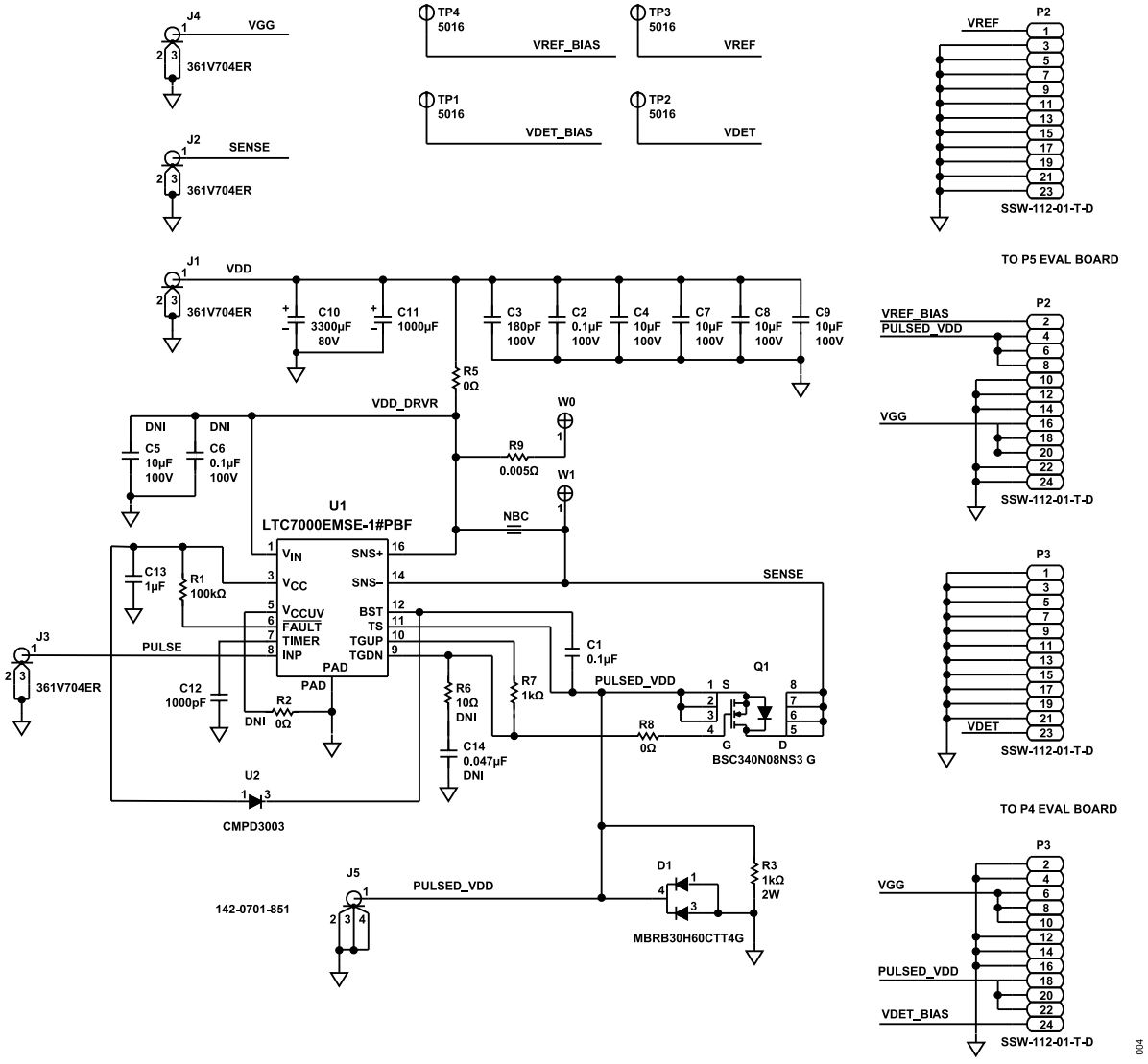

Figure 4. Analog Devices, Inc., Pulser Board Schematic

OPERATING THE ADPA1106-EVALZ WITH THE DRAIN BIAS PULSER BOARD

SETUP

The connections required to use the ADPA1106-EVALZ with the drain bias pulser board are shown in Figure 5. Before applying any bias or signals, plug the pulser board into the ADPA1106-EVALZ so that the P2 header connector of the pulser board connects to the P5 header of the ADPA1106-EVALZ, and the P3 header of the pulser board connects to the P4 header of the ADPA1106-EVALZ. All external supply voltages and control signals are applied to the J1 thru J4 BNC connectors of the pulser board, which are listed in Table 3.

Table 3. Pulser Board J1 to J4, TP1 to TP4, and P2 and P3 Header Connections to the ADPA1106

Header	Header Pin Number	Header Pin Name
J1	Not applicable	VDD
J2	Not applicable	SENSE
J3	Not applicable	PULSE
J4	Not applicable	VGG
J5	Not applicable	PULSED VDD
TP1	Not applicable	VDET_BIAS
TP2	Not applicable	VDET
TP3	Not applicable	VREF
TP4	Not applicable	VREF_BIAS
P2	1	VREF
	2	VREF_BIAS
	3, 5, 7, 9 to 15, 17, 19, 21 to 24	GND

Table 3. Pulser Board J1 to J4, TP1 to TP4, and P2 and P3 Header Connections to the ADPA1106

Header	Header Pin Number	Header Pin Name
	4, 6, 8	PULSED_VDD
	16, 18, 20	VGG
P3	1 to 5, 7, 9, 11 to 17, 19, 21	GND
	6, 8, 10	VGG
	18, 20, 22	PULSED_VDD
	23	VDET
	24	VDET_BIAS

The gate control voltage applied to the J4 connector passes directly through the pulser board and drives the VGG1 and VGG2 pins of the ADPA1106. Because the VDD and GND lines carry currents up to 2 A, the use of heavy gauge twister pair wires is recommended to minimize voltage drops. To observe the pulsed drain voltage (PULSED_VDD) that drives the VDD1 and VDD2 pins of the ADPA1106, connect an oscilloscope to the J5 coaxial connector on the pulser board.

Connect a digital pulse generator that can generate 0 V to 5 V pulses with a pulse width of 100 µs and a duty cycle of 10% to the pulse input, J3.

To observe and measure the drain current and the ADPA1106 RF output power, use a current probe and a pulsed RF power meter. If these methods are not available, make approximations as described in the Making Average to Pulsed Approximations section.

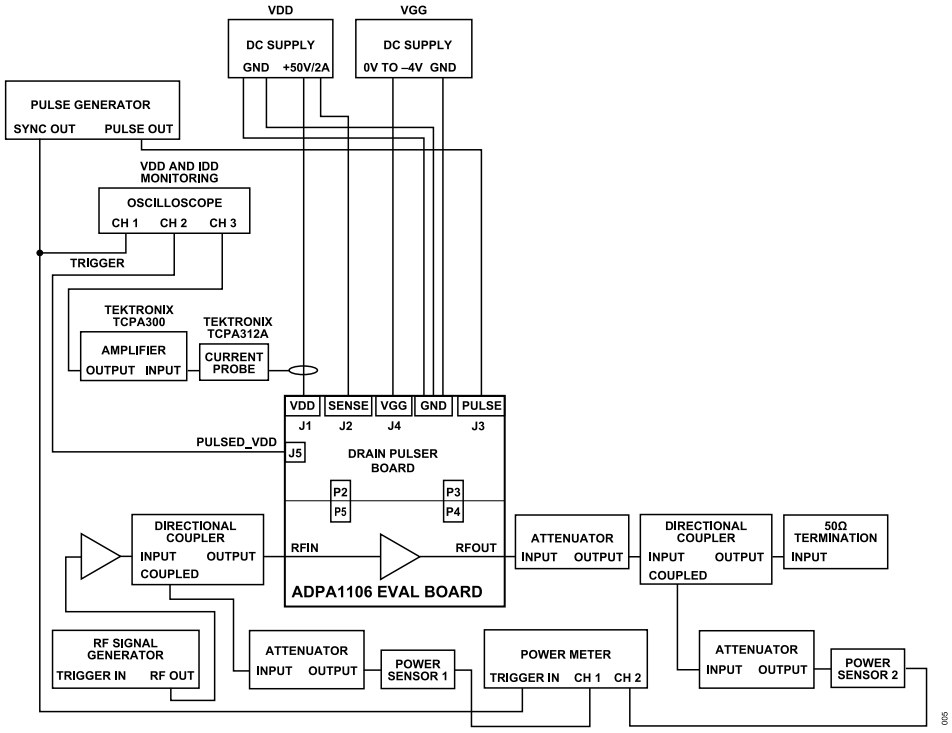

Figure 5. Setup Block Diagram

OPERATING THE ADPA1106-EVALZ WITH THE DRAIN BIAS PULSER BOARD

OPERATION

Take the following steps to power up (unless otherwise stated, all signals are applied to the pulser board) the ADPA1106-EVALZ:

1. Set the voltage on J3 (PULSE) to 0 V.
2. Set the voltage on J4 (VGG) to −4 V.
3. Set the voltage on J1 (VDD) to 50 V.
4. Turn on PULSE (0 V/5 V, 100 µs, 10% duty cycle).
5. Increase the voltage on J4 (VGG) until the target I_{DQ} is reached (nominally 300 mA).
6. Apply the RF input signal to the RFIN connector of the ADPA1106-EVALZ.

Take the following steps to power down the ADPA1106-EVALZ:

1. Turn off the RF input signal.
2. Set the voltage on J4 (VGG) to −4 V.
3. Turn off PULSE (set to 0 V).
4. Set the voltage on J1 (VDD) to 0 V.
5. Set the voltage on J4 (VGG) to 0 V.

MAKING AVERAGE TO PULSED APPROXIMATIONS

Instruments that can be triggered are required to measure the RF power, drain current, and power added efficiency (PAE) accurately under pulsed operation. When such instrumentation is not available, use averaging and approximations. The most common approximations involve measuring the average values and then adjusting those values to account for the duty cycle. These approximations can result in errors because of limited measurement bandwidths of instruments and/or the inclusion of on and off transients and/or partial periods in the measurement.

To ensure that partial periods do not contribute significant errors to the measurements, perform averaging over a large number of pulse periods. The results of such approximations can vary with the instruments and settings used. Therefore, experimentation can be necessary to achieve credible and repeatable results. When it is not possible to make pulse triggered measurements, the only pulse connection required is the connection from the pulse generator to the J3 connector of the pulser (see Figure 5).

EVALUATION BOARD SCHEMATIC AND ARTWORK

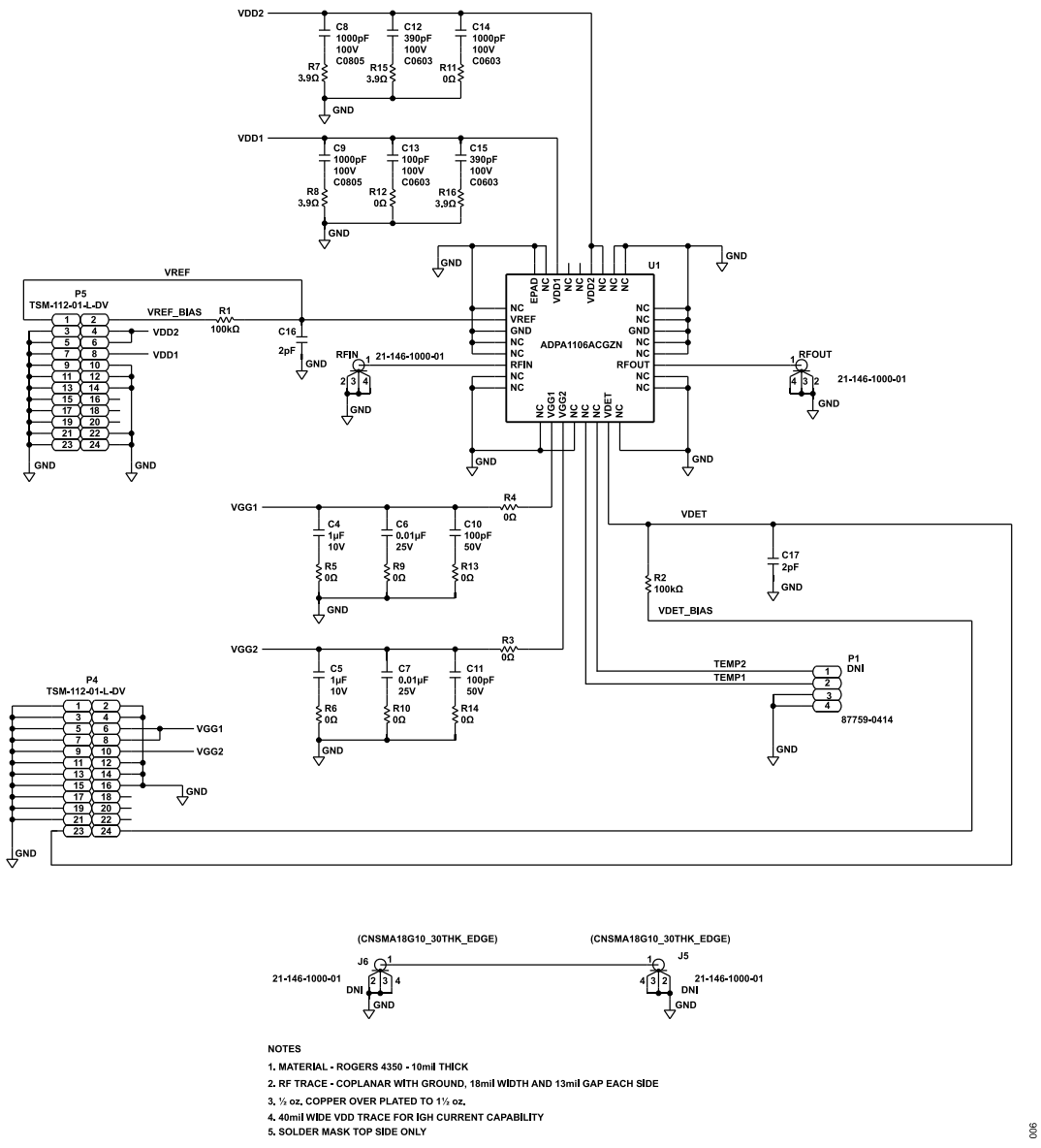

Figure 6. ADPA1106-EVALZ Evaluation Board Schematic

EVALUATION BOARD SCHEMATIC AND ARTWORK

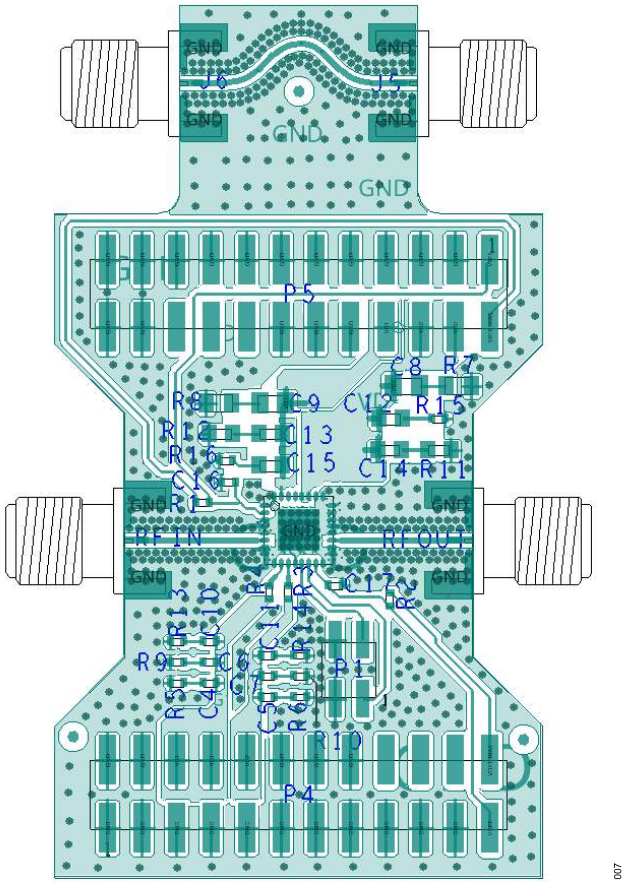

Figure 7. ADPA1106-EVALZ Assembly Drawing (J6 and J5 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description	Manufacturer	Part Number
C4, C5	Capacitors, ceramic, 1 µF	TDK	C1005X7S1A105K
C6, C7	Capacitors, ceramic, 0.01 µF	TDK	C1005X8R1E103K
C8, C9	Capacitors, ceramic, ceramic 1000pF 100V	AVX Corporation	08051C102KAT2A
C10, C11	Multilayer capacitors, ceramic, 100 pF	TDK	C1005NP01H101J050BA
C12, C15	Capacitors, ceramic, 390 pF	KEMET	C0603C391J1GAC7867
C14	Capacitor, ceramic, 1000 pF	TDK	C1608C0G2A102J
C13	Capacitor, ceramic,100 pF, 100 V	MURATA	GCM1885G2A101FA16
C16, C17	Capacitors, ceramic, 2 pF	AVX	04023U2R0BAT2A
P1	Connector, PCB header, vertical, dual-row, 4-pin, 2 mm pitch, do not install (DNI)	Molex	87759-0414
P4, P5	Connectors, PCB header, vertical, dual-row, 24-pin, 2.54 mm pitch	SAMTEC INC.	TSM-112-01-L-DV
R1, R2	Resistors, thick film chip,100 kΩ, 1%	Panasonic	ERJ-2RKF1003X
R3, R4, R5, R6, R9, R10, R13, R14	Resistors, surface-mount device (SMD) chip jumper, 0 Ω	Panasonic	ERJ-2GE0R00X
R7, R8	Resistors, thick film chip	Stackpole Electronics, Inc.	RMCF0805FT3R90
R11, R12	Resistors, film SMD, 0 Ω	Panasonic	ERJ-3GEY0R00V
R15, R16	Resistors, thick film chip, 3.9 Ω	Panasonic	ERJ-2GEJ3R9X
J5, J6	Connectors, SMA jack edge, DNI	SRI Connector Gage Co.	21-146-1000-01
J1 RFIN, J2 RFOUT	Connectors, SMA jack edge	SRI Connector Gage Co.	21-146-1000-01
U1	40 dBm (40 W), 2.7 GHz to 3.5 GHz, GaN power amplifier	Analog Devices	ADPA1106ACGZN
Not Applicable	Aluminum heat sink, 2.51 in × 1.91 in	Not applicable	Not applicable

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.