



# **LIF-MD6000 Raspberry Pi AP Link Board**

## **Evaluation Board User Guide**

FPGA-EB-02006 Version 1.1

January 2018

## Contents

1. Introduction .....	3
2. Headers and Test Connections .....	5
3. Power Supply .....	6
4. Ordering Information .....	7
References .....	8
Technical Support Assistance .....	8
Appendix A. Raspberry Pi AP Link Board Schematics .....	9
Appendix B. Raspberry Pi AP Link Board Bill of Materials .....	10
Revision History .....	11

## Figures

Figure 1.1. Top View of Raspberry Pi AP Link Board .....	3
Figure 1.2. Bottom View of Raspberry Pi AP Link Board .....	4
Figure A.1. Raspberry Pi AP Link Board .....	9

## Tables

Table 2.1. Headers and Test Connectors .....	5
Table 2.2. J1 and J2 Connector Description .....	5
Table 2.3. U1 Connector Description .....	5
Table 3.1. Power LED .....	6
Table 4.1. Ordering Information .....	7

## 1. Introduction

This document describes the Lattice Semiconductor LIF-MD6000 Raspberry Pi AP Link board (RPI-APL-EVN) that is part of the two inputs to one output MIPI® Camera Serial Interface (CSI-2) camera aggregator bridge solution. This solution aggregates the data from two image sensors and outputs it to a single MIPI® CSI-2 output. The Raspberry Pi AP Link board allows the Raspberry Pi processor board to interface to the CrossLink™ LIF-MD6000 Master Link board. The Raspberry Pi processor board is attached to this board via a ribbon cable to the 15-pin connector.

The CrossLink: LIF-MD6000 Raspberry Pi Boards kit (LIFMD-RPI-EVN) consists of two LIF-MD6000 Raspberry Pi Camera Link Boards (RPI-CL-EVN) and one LIF-MD6000 Raspberry Pi AP Link Board (RPI-APL-EVN).

For the latest information about this board, visit

[www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/CrossLinkLIFMD6000RaspberryPiBoards](http://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/CrossLinkLIFMD6000RaspberryPiBoards)

For details about the CrossLink FPGA, refer to FPGA-DS-02007, [CrossLink Family Data Sheet](#).

The content of this user guide includes descriptions of connectors, schematics, and bill of materials of the LIF-MD6000 Raspberry Pi AP Link board. Refer to [Appendix A](#) and [Appendix B](#) for the schematics and BOM.

[Figure 1.1](#) shows the top view of the Raspberry Pi AP Link board, and [Figure 1.2](#) shows the bottom view of the board.

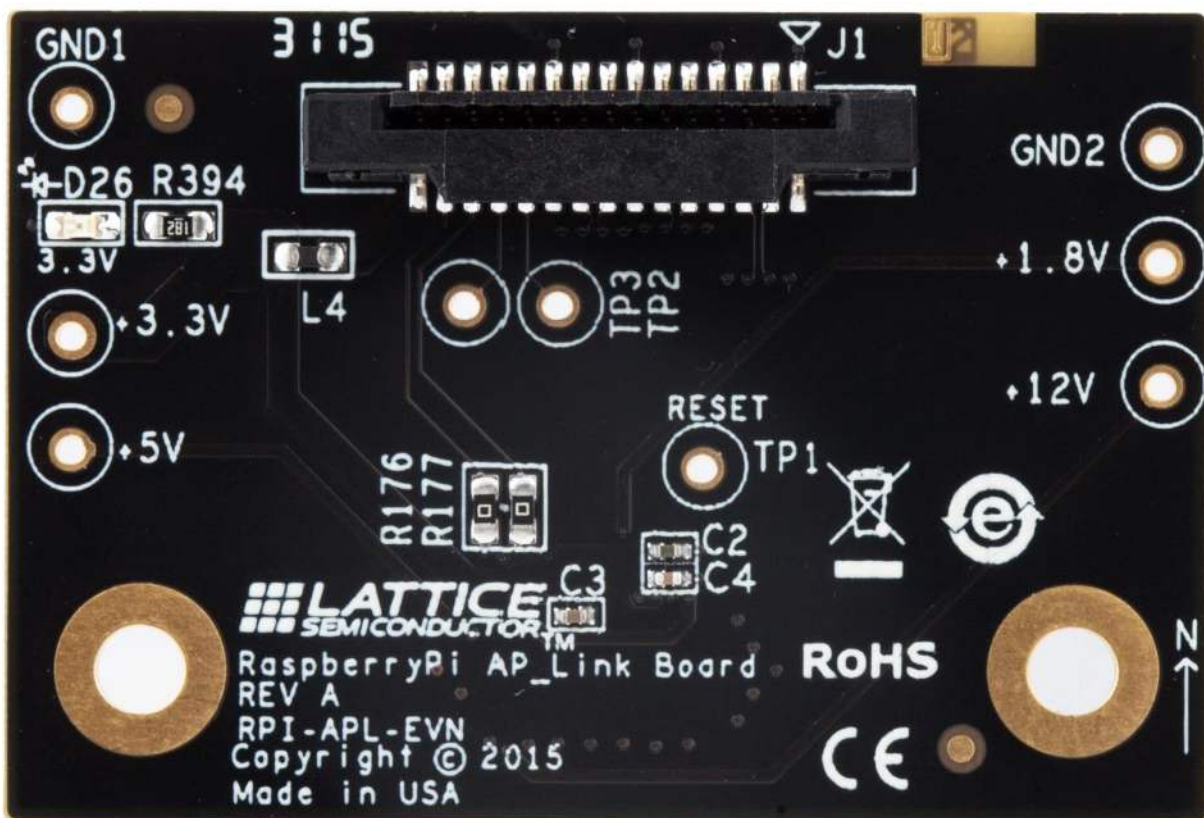


Figure 1.1. Top View of Raspberry Pi AP Link Board

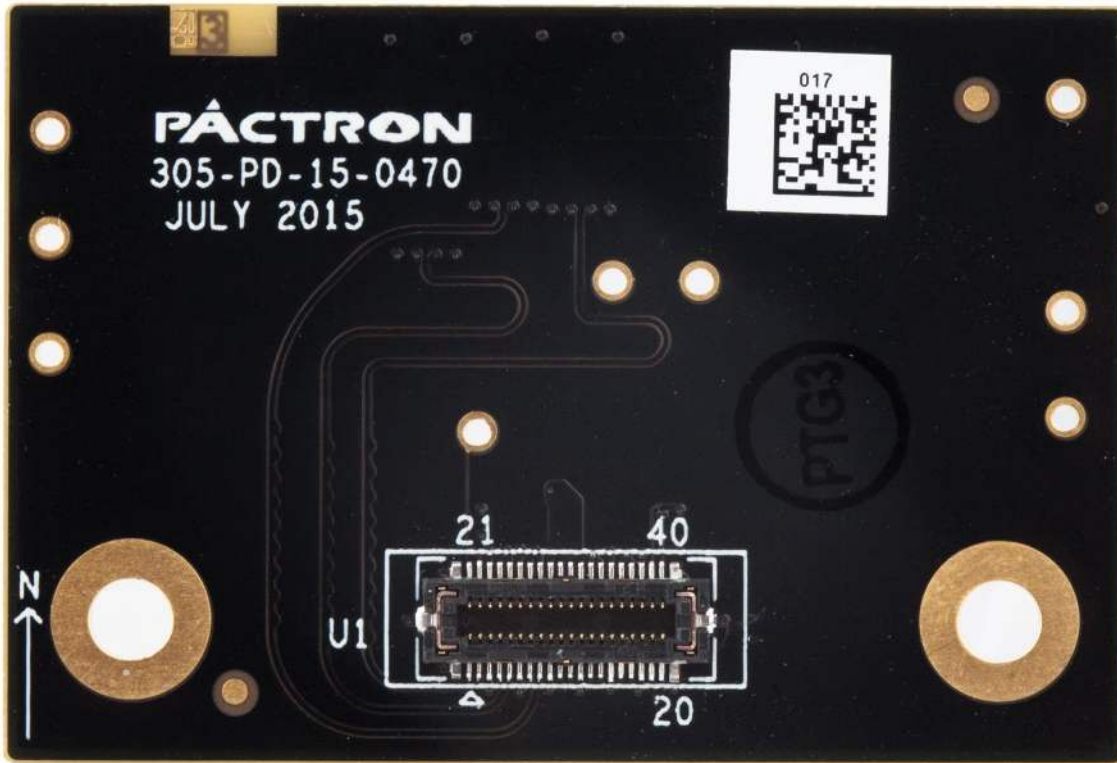


Figure 1.2. Bottom View of Raspberry Pi AP Link Board

## 2. Headers and Test Connections

Figure 1.1 and Figure 1.2 show the top and bottom views of the Raspberry Pi AP Link board. The connectors on the board provide an interface between LIF-MD6000 Master Link board and Raspberry Pi processor board. Table 2.1 lists the headers and test connectors.

**Table 2.1. Headers and Test Connectors**

Part	Description	Setting
J1	15-pin connector to interface to Raspberry Pi processor board	—
U1	40-pin connector to interface to CrossLink Master Link board	—

**Table 2.2. J1 and J2 Connector Description**

Pin	J1
1	GND
2	DATA0_N
3	DATA0_P
4	GND
5	DATA1_N
6	DATA1_P
7	GND
8	DCK_N
9	DCK_P
10	GND
11	GPIO1
12	GPIO2
13	SCL
14	SDA
15	AP_3V3

**Table 2.3. U1 Connector Description**

Pin	Name
1	CH4_DCK_P
2	CH4_DCK_N
3	GND
4	CH4_DATA0_P
5	CH4_DATA0_N
6	GND
7	CH4_DATA1_P
8	CH4_DATA1_N
9	GND
10	SN
11	SCLK

**Table 2.3. U1 Connector Description (Continued)**

Pin	Name
12	GND
13	CH4_DATA2_P
14	CH4_DATA2_N
15	GND
16	CH4_DATA3_P
17	CH4_DATA3_N
18	GND
19	12V
20	12V
21	TBD
22	RESETN
23	PWR_5-0V
24	GND
25	GND
26	PWR_3-3V
27	GND
28	GND
29	PWR_1-8V
30	MOSI
31	MISO
32	PWR_1-8V
33	GND
34	GND
35	PWR_3-3V
36	GND
37	GND
38	PWR_5-0V
39	SDA
40	SCL

### 3. Power Supply

Power is provided to the Raspberry Pi AP Link board from the CrossLink Master Link board through U7 connector.


Table 3.1 lists the power status LED.

**Table 3.1. Power LED**

Voltage Rail	LEDs	Colour
3.3	D26	Green

## 4. Ordering Information

Table 4.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
CrossLink: LIF-MD6000 Raspberry Pi Boards Kit includes one Raspberry Pi AP Link Board and two Raspberry Pi Camera Link Boards	LIFMD-RPI-EVN	

## References

For more information, refer to:

- FPGA-DS-02007, [CrossLink Family Data Sheet](#)
- UG117, [2:1 MIPI CSI-2 Image Sensor Aggregator Bridge Demo User Guide](#)

## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).



## Appendix A. Raspberry Pi AP Link Board Schematics

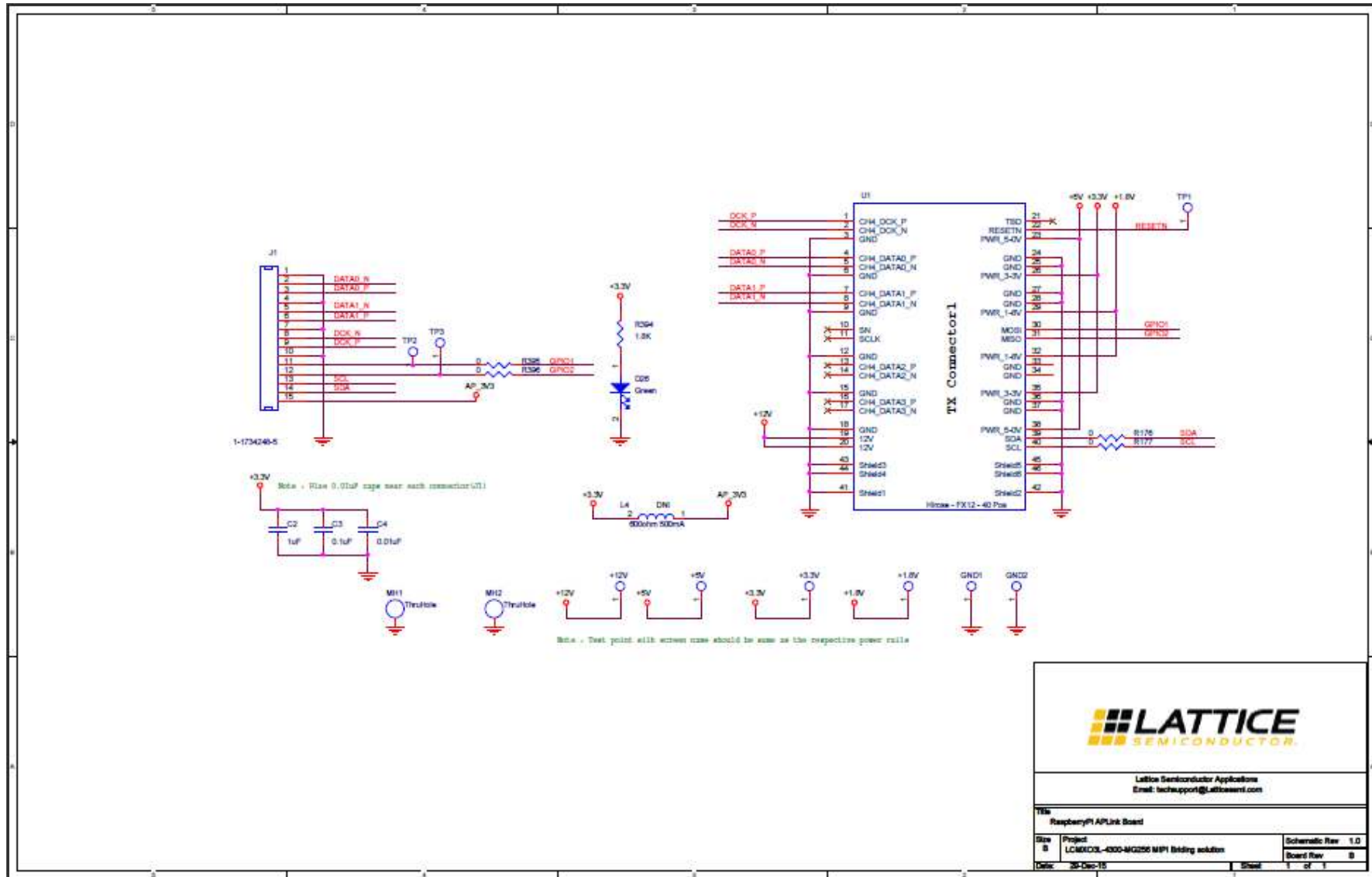


Figure A.1. Raspberry Pi AP Link Board

## Appendix B. Raspberry Pi AP Link Board Bill of Materials

### Raspberry Pi AP Link Board Bill of Materials

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	Description
1	TP1, GND1, TP2, GND2, TP3, +5V, +12V, +1.8V, +3.3V	9	TP_S_40_63	tp_s_40_63	DNL	—	—	Square test point, 40 mil inner diameter, 63 mil outer diameter
2	C2	1	1 $\mu$ F	C0402	—	C0402C105K9 PACTU	Kemet	CAP CERAMIC 1 $\mu$ F 6.3 V X5R 0402
3	C3	1	0.1 $\mu$ F	C0402	—	C0402C104K4 RACTU	Kemet	CAP CERAMIC 0.1 $\mu$ F 16 V X7R 0402
4	C4	1	0.01 $\mu$ F	C0402	—	C0402C103J4 RACTU	Kemet	CAP CERAMIC 10 nF 16 V 5% X7R 0402
5	D26	1	Green	led_0603	—	LTST-C190KGKT	LITE-On INC	LED SUPER GREEN CLEAR 0603 SMD
6	J1	1	1-1734248-5	1-1734248-5	—	1-1734248-5	TE CONNECTIVITY	CONN FPC VERT 15 POS 1.00 mm SMD
7	L4	1	600 $\Omega$ 500 mA	FB0603	—	BLM18AG601 SN1D	Murata	Ferrite Bead 600 $\Omega$ @100 MHz 500 mA 0603
8	MH1, MH2	2	ThruHole	MTG125	DNL	—	—	—
9	R176, R177	2	0	R0603	—	RC0603JR-070RL	Yageo	Res 1/10 W 0.0 $\Omega$ 5% 0603
10	R394	1	1.8K	R0603	—	RC0603FR-071K8L	Yageo	Thick Film Resistors - SMD 1.8K $\Omega$ 1%
11	U1	1	Hirose - FX12 - 40 Pos	Hirose-FX12S	—	FX12B-40S-0.45V	Hirose Electric Co Ltd	Conn Board to Board PL 40 POS 0.4 mm Solder ST SMD T/R
12	RASPBERRYPI_A PLINK_BOARD PCB	1	—	—	—	305-PD-15-0470	PACTRON	—

## Revision History

Date	Version	Change Summary
January 2018	1.1	<ul style="list-style-type: none"><li>• Changed pASSP to FPGA in the <a href="#">Introduction</a> section.</li><li>• Updated Lattice Semiconductor Logo on the cover pages, the headers, and the footers of the document.</li></ul>
May 2017	1.0	Initial release.



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