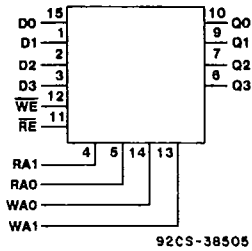


High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4 x 4 Register File

Type Features:

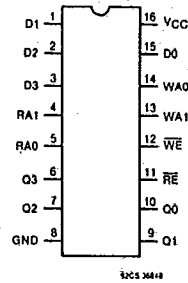
- Simultaneous and Independent Read and Write Operations
- Expandable to 512 Words of n-Bits
- 3-State Outputs
- Organized as 4 Words x 4 Bits Wide
- Typical read time: 16 ns for HC670 at $V_{CC} = 5 V$, $C_L = 15 pF$, $T_A = 25^\circ C$
- Buffered inputs

The RCA-CD54/74HC670 and CD54/74HCT670 are 16-bit register files organized as 4 words x 4 bits each. Read and write address and enable inputs allow simultaneous writing into one location while reading another. Four data inputs are provided to store the 4-bit word. The write address inputs (WA0 and WA1) determine the location of the stored word in the register. When write enable (\overline{WE}) is low the word is entered into the address location and it remains transparent to the data. The outputs will reflect the true form of the input data. When (\overline{WE}) is high data and address inputs are inhibited. Data acquisition from the four registers is made possible by the read address inputs (RA1 and RA0). The addressed word appears at the output when the read enable (\overline{RE}) is low. The output is in the high impedance state when the (\overline{RE}) is high. Outputs can be tied together to increase the word capacity to 512 x 4 bits.

The RCA CD54HC/HCT670 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT670 are supplied in a 16-lead dual-in-line plastic package (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 V$ Max., $V_{IH} = 2 V$ Min.
CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC670 CD54/74HCT670

HARRIS SEMICONDUCTOR 27E D 4302271 0017859 J HAS

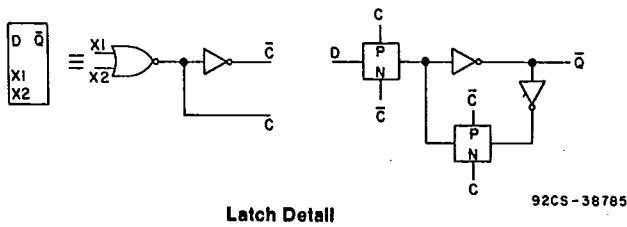
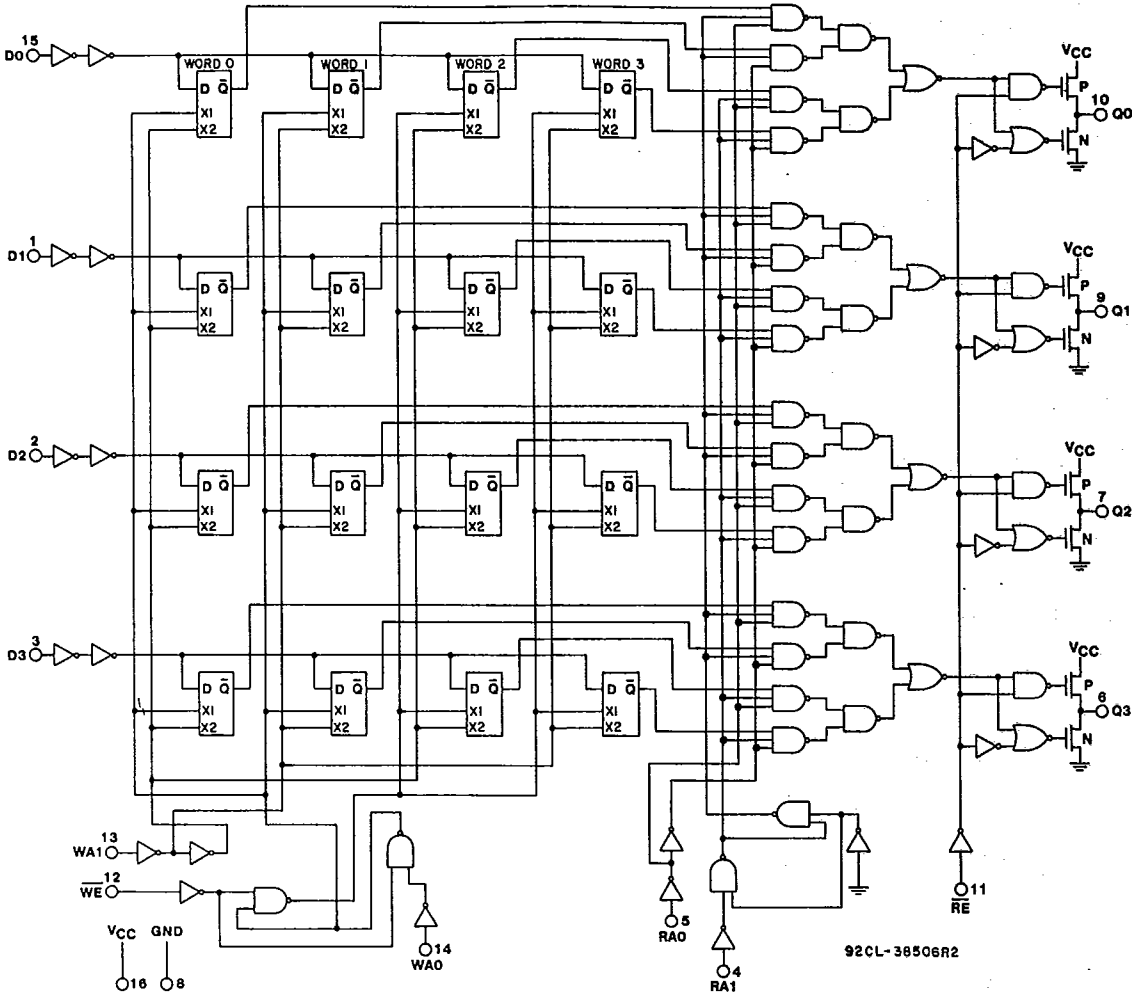


Fig. 1 — Logic Diagram.

CD54/74HC670
CD54/74HCT670

HARRIS SEMICOND SECTOR 27E D ■ 430227J 0017860 8 ■ HAS

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES ^(a)
	\overline{WE}	D_N	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE:

a. The Write Address (WA0 and WA1) to the "internal latches" must be stable while \overline{WE} is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT Q_N
	\overline{RE}	INTERNAL LATCHES ^(b)	
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

NOTE:

b. The selection of the "internal latches" by Read Address (RA0 and RA1) are not constrained by \overline{WE} or \overline{RE} operation

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = HIGH impedance "off" state.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ$ C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ$ C
PACKAGE TYPE E, M	-40 to $+85^\circ$ C
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ$ C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 in. (1.59 \pm 0.79 mm) from case for 10 s max.	$+265^\circ$ C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	$+300^\circ$ C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A :			
CD74 Types	-40	+85	$^\circ$ C
CD54 Types	-55	+125	$^\circ$ C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC670
CD54/74HCT670

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC670/CD54HC670										CD74HCT670/CD54HCT670										UNITS			
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES			54HC SERIES			TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES				54HCT SERIES		
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C			-55/ +125°C			V _I V	V _{CC} V	+25°C			-40/ +85°C				-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max		
High-Level Input Voltage V _{OH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	—	V		
			4.5	3.15	—	—	3.15	—	3.15	—	—	5.5		—	—	—	—	—	—	—	—	—	—	
			6	4.2	—	—	4.2	—	4.2	—	—	—		—	—	—	—	—	—	—	—	—	—	
Low-Level Input Voltage V _{OL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5		—	—	—	—	—	—	—	—	—	—	
			6	—	—	1.8	—	1.8	—	1.8	—	—		—	—	—	—	—	—	—	—	—	—	
High-Level Output Voltage V _{OH} CMOS Loads	V _{IL} or V _{OH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{OH}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V		
			4.5	4.4	—	—	4.4	—	4.4	—	—			—	—	—	—	—	—	—	—	—	—	
			6	5.9	—	—	5.9	—	5.9	—	V _{IL} or V _{OH}			4.5	3.98	—	—	3.84	—	3.7	—	—	—	V
TTL Loads Bus Driver	V _{IL} or V _{OH}	-6 or -7.8	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL} or V _{OH}	4.5	3.98	—	—	3.84	—	3.7	—	—	—	V		
			6	5.48	—	—	5.34	—	5.2	—	—			—	—	—	—	—	—	—	—	—		
			—	—	—	—	—	—	—	—	—			—	—	—	—	—	—	—	—	—	—	—
Low-Level Output Voltage V _{OL} CMOS Loads	V _{IL} or V _{OH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{OH}	4.5	—	—	—	0.1	—	0.1	—	0.1	—	V		
			4.5	—	—	0.1	—	0.1	—	0.1	—			—	—	—	—	—	—	—	—	—		
			6	—	—	0.1	—	0.1	—	0.1	—			V _{IL} or V _{OH}	4.5	—	—	0.26	—	0.33	—	0.4	—	V
TTL Loads Bus Driver	V _{IL} or V _{OH}	6 or 7.8	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL} or V _{OH}	4.5	—	—	—	0.26	—	0.33	—	0.4	—	V		
			6	—	—	0.26	—	0.33	—	0.4	—			—	—	—	—	—	—	—	—	—		
			—	—	—	—	—	—	—	—	—			—	—	—	—	—	—	—	—	—	—	—
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	μA		
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	—	160	μA		
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	490	μA		
3-State leakage current	V _{IL} or V _{OH}	V _O = V _{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V _{IL} or V _{OH}	5.5	—	—	±0.5	—	±5	—	±10	—	±10	μA		

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

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CD54/74HC670
CD54/74HCT670

HARRIS SEMICONDUCTOR

27E D ■ 4302271 0017862 1 ■ HAS

HCT Input Loading Table

Input	Unit Loads*
WE	0.3
WAO	0.2
WA1	0.4
RE	1.5
DATA	0.15
RA0	0.4
RA1	0.7

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS ($V_{CC} = 5 V$, $T_A = 25^\circ C$, Input $t_r = 6 ns$)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay	15	t_{PLH}	16	17	ns
Reading any word		t_{PHL}			
Write Enable to Output	15	t_{PLH} t_{PHL}	21	21	ns
Data to Output	15	t_{PLH} t_{PHL}	21	21	ns
Output Disable Time	15	t_{PLZ} t_{PHZ}	12	14	ns
Output Enable Time	15	t_{PZL} t_{PZH}	12	16	ns
Power Dissipation Capacitance*	—	C_{PD}	59	66	pF

* C_{PD} is used to determine the dynamic power consumption, per output.
 $PD = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where f_i = input frequency,
 f_o = output frequency,
 C_L = output load capacitance
 V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Set-up time Data to \overline{WE}	t_{su}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold time Data to \overline{WE}	t_h	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Set-up time Write to \overline{WE}	t_{su}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	18	—	15	—	23	—	18	—	27	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold time Write to \overline{WE}	t_h	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
\overline{WE} Pulsewidth	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Latch time \overline{WE} to RA0, RA1	t_{LATCH}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	25	—	25	—	31	—	30	—	38	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	

CD54/74HC670
CD54/74HCT670

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r = 6 ns,)

CHARACTERISTIC	SYMBOL	V _{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Reading any word	t _{PLH}	2	—	195	—	—	245	—	—	295	—	—	ns		
	t _{PHL}	4.5	—	39	—	40	—	49	—	50	—	60			
		6	—	33	—	—	42	—	—	50	—	—			
Write Enable to Output	t _{PLH}	2	—	250	—	—	315	—	—	375	—	—	ns		
	t _{PHL}	4.5	—	50	—	50	—	63	—	63	—	75			
		6	—	43	—	—	54	—	—	64	—	—			
Data to Output	t _{PLH}	2	—	256	—	—	315	—	—	375	—	—	ns		
	t _{PHL}	4.5	—	50	—	50	—	63	—	63	—	75			
		6	—	43	—	—	54	—	—	64	—	—			
Output Disable Time	t _{PLZ}	2	—	150	—	—	190	—	—	225	—	—	ns		
	t _{PHZ}	4.5	—	30	—	35	—	38	—	44	—	53			
		6	—	26	—	—	33	—	—	38	—	—			
Output Enable Time	t _{PZL}	2	—	150	—	—	190	—	—	225	—	—	ns		
	t _{PZH}	4.5	—	30	—	38	—	38	—	48	—	57			
		6	—	26	—	—	33	—	—	38	—	—			
Output Transition Time	t _{TLH}	2	—	75	—	—	95	—	—	110	—	—	ns		
	t _{THL}	4.5	—	15	—	15	—	19	—	19	—	22			
		6	—	13	—	—	10	—	—	19	—	—			
3-State Output Capacitance	C _O		—	20	—	20	—	20	—	20	—	20	pF		
Input Capacitance	C _I		—	10	—	10	—	10	—	10	—	10	pF		

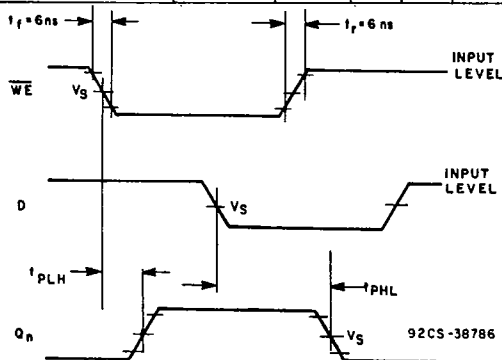


Fig. 2 — Propagation Delay, Write Enable and Data to Output

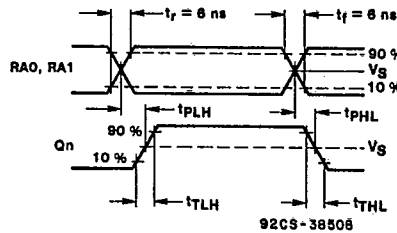


Fig. 3 — Propagation delay, Read Address to Output

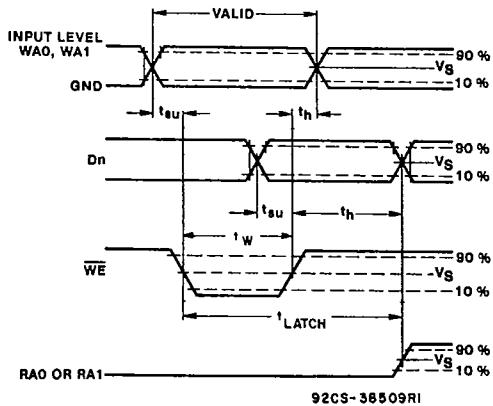


Fig. 4 — Setup and Hold Times, Write Address and Data to Write Enable

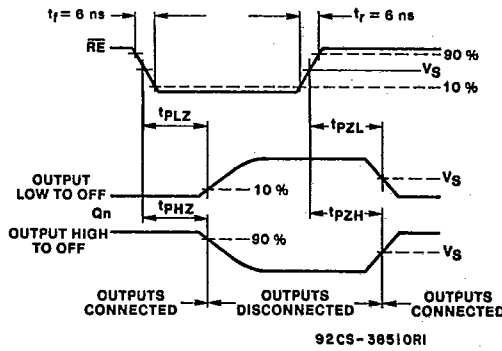


Fig. 5 — 3-State Enable and Disable Times

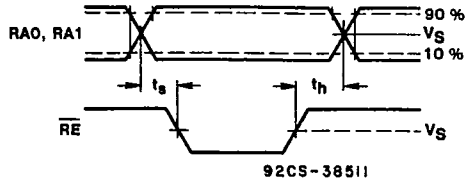
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CD54/74HCT670

HARRIS SEMICONDUCTOR

27E D

■ 4302271 0017864 5 ■ HAS



	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 6 — Setup and Hold times, Read Address to Read Enable

