TPS53114EVM-541

The TPS53114EVM-541 evaluation module can demonstrate a wide-input-voltage (5 V–22 V) to 1.20-V, 4-A application in a stand-alone module. This module allows a customer to evaluate the performance of the TPS53114 controller in a typical synchronous, buck (step-down) application. Specifications, test procedure and setup, design files, and typical performance are included for reference.

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1 Introduction

1.1 Description

TPS53114EVM-541 evaluation module is an example of a high-efficiency, single, synchronous buck converter providing 1.20 V at 4 A from 5-V to 22-V input using the TPS53114 single-channel D-CAP2™ mode controller. The TPS53114 provides the user the ability to evaluate the performance of the TPS53114 in a typical application including test points for simple, noninvasive monitoring of critical signals within the design. This user's guide contains a schematic, board layout, and bill of materials along with typical performance characteristics and test methodology

1.2 Applications

- Low-voltage microcontroller core or I/O supply
- Low-voltage DPS core supply
- FPGA core supply
- Low-cost, low-voltage, point-of-load converter

1.3 Features

- Wide 5-V to 22-V input voltage range
- Fixed 1.20-V output voltage
- 4-A steady-state current
- 350-kHz or 700-kHz switching frequency (350-kHz optimized power stage)
- Enable and frequency select switches
- Test points for noninvasive measurement of switching waveforms, and input and output voltages.

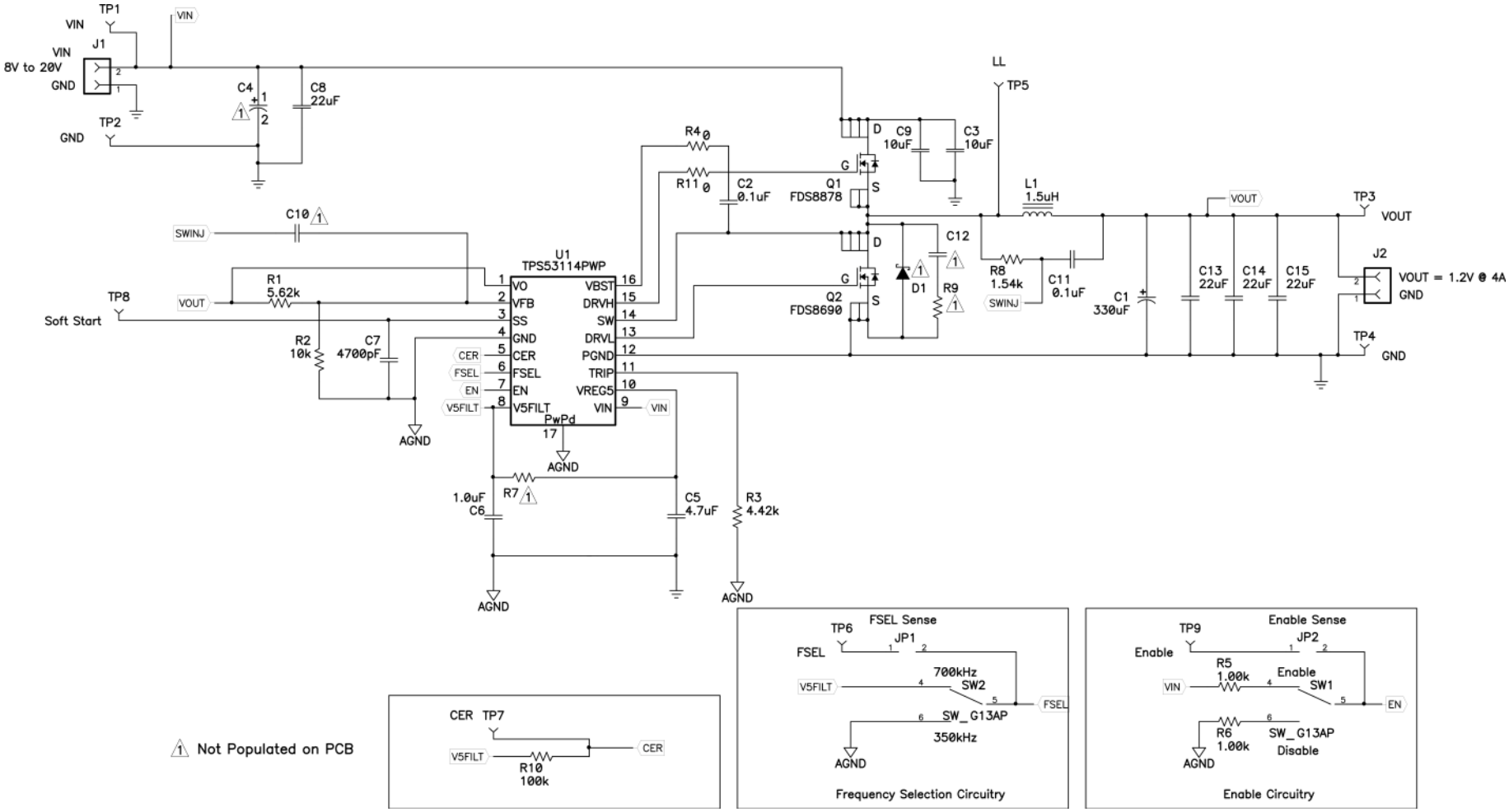
2 TPS53114EVM-541 Electrical Performance Specifications

Table 1. TPS53114EVM-541 Electrical and Performance Specifications

Parameter		Notes and Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{IN}	Input Voltage		5	12	22	V
I_{IN}	Input Current	V_{IN} = 12, $I_{OU}T$ = 4 A	–	0.43	0.45	A
	No Load Input Current	V_{IN} = 12, I_{OUT} = 0 A	–	19	22	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 4	3.8	4.2	4.5	V
Output Characteristics						
V_{OUT1}	Output Voltage 1	V_{IN} = 12, I_{OUT} = 2 A	1.17	1.20	1.23	V
	Line Regulation	V_{IN} = 5 V to 22 V	–	–	1%	
	Load Regulation	I_{OUT} = 0 A to 4 A	–	–	1%	
V_{OUT_ripple}	Output Voltage Ripple	V_{IN} = 12 V, I_{OUT} = 4 A	–	–	30	mVpp
I_{OUT1}	Output Current 1	V_{IN} = 5 V to 22 V	0		4	A
Systems Characteristics						
F_{SW}	Switching Frequency	SW2 = 350 kHz	300	350	400	kHz
ηpk	Peak Efficiency	V_{IN} =12 V, SW2 = 350 kHz	–	86%	–	
η	Full Load Efficiency	V_{IN} =12 V, I_{OUT} = 4 A, SW2 = 350 kHz	–	85%	–	

D-CAP2 is a trademark of Texas Instruments.

3 TPS53114EVM-541 Schematic



For reference only; see Table 3 for specific values.

Figure 1. TPS53114EVM-541 Schematic

4 Connector and Test Point Descriptions

4.1 Enable Switch and Enable Sense – SW1 and JP2

The TPS53115EVM-451 is equipped with a switch (SW1) to drive the EN pin of the TPS53114. When SW1 is in the EN position, EN is connected to VIN, and the TPS53114 is enabled and generates a regulated 1.20-V output. When SW1 is in the DIS position, EN is connected to GND, and the TPS53114 enters a high-impedance output state with approximately 15 kΩ to GND.

Installing JP2 connects the EN pin voltage to the Enable Sense test point (TP9) to allow the user to monitor the EN pin status.

4.2 Frequency Selection Switch and Frequency Sense – SW2 and JP1

The TPS53115EVM-451 is equipped with a switch (SW2) to drive the FSEL pin of the TPS53114. When SW2 is in the 350-kHz position, EN is connected to VIN, and the TPS53114 is programmed to switch as 350 kHz. When SW2 is in the 700-kHz position, FSEL is connected to GND, and the TPS53114 is programmed to switch at 700 kHz.

Installing JP1 connects the FSEL pin voltage to the Frequency Sense test point (TP6) to allow the user to monitor the FSEL pin status.

4.3 Test Point Descriptions

Table 2. Test Point Description

Test Point	Label	Use	Section
TP1	VIN	Monitor input voltage	4.3.1
TP2	PGND	Ground for input voltage	4.3.1
TP3	VOUT	Monitor output voltage	4.3.2
TP4	PGND	Ground for output voltage	4.3.2
TP5	LL	Monitor switch node voltage	4.3.3
TP6	FSEL	Monitor frequency select voltage	4.3.4
TP7	CER	Monitor output capacitor select pin voltage	4.3.5
TP8	SS	Monitor soft-start ramp voltage	4.3.6
TP9	EN	Monitor enable voltage	4.3.7

4.3.1 Input Voltage Monitoring –TP1 and TP2

The TPS53114EVM-541 provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connectors. All input voltage measurements must be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and negative terminal to TP2.

4.3.2 Output Voltage Monitoring – TP3 and TP4

The TPS53114EVM-541 provides two test points for measuring the output voltage generated by the module. This allows the user to measure the actual module voltage without losses from output cables and connectors. All output voltage measurements must be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive terminal to TP3 and negative terminal to TP4.

4.3.3 Switching (Phase) Voltage Monitoring – TP5 and TP4

The TPS53114EVM-541 provides a test point for measuring the switching or phase node voltage at the junction of the two MOSFETs. This allows the user to monitor the switching waveform without additional wires or cables. Basic switch node measurements made from TP5. To use TP5, connect an oscilloscope probe tip to TP5, and use TP4 for the ground clip.

4.3.4 Frequency Select Voltage Monitoring – TP6 and TP2

The TPS53114EVM-541 provides a test point for monitoring or driving the FSEL pin. This allows the user to monitor the voltage on the FSEL pin. To use TP6, Install a shunt in JP1, and connect a voltmeter positive terminal to TP6 and negative terminal to TP2.

4.3.5 Output Capacitor Select Pin Voltage Monitoring -TP7

The TPS53114EVM-541 provides a test point for the monitoring output capacitor selection pin of the TPS53114 controller. It is connected to V5FILT for conductive polymer electrolyte type output capacitor on the EVM.

4.3.6 Soft-Start – TP8 and TP2

The TPS53114EVM-541 provides a test point for monitoring the Soft-Start ramp voltage. This allows the user to monitor the soft-start voltage during power on. To use TP8, connect an oscilloscope probe tip to TP8, and use TP2 for the ground clip.

4.3.7 Enable– TP9

The TPS53114EVM-541 provides a test point for monitoring the Enable voltage. This allows the user to monitor the enable voltage during power on and power off. To use TP9, install a shunt in JP2, and connect an oscilloscope probe tip to TP9, and use TP2 for the ground clip.

5 Test Setup (Optional)

5.1 Equipment

5.1.1 Voltage Source

V_{IN} must be a voltage source capable of 0 Vdc to 22 Vdc at a minimum 1 A. Connect V_{IN} to J1 as shown in Figure 2.

5.1.2 Meters

A1: Input Current Meter. 0-Adc to 1-Adc ammeter
V1: Input Voltage Meter. 0-V to 22-V voltmeter
V2: Output Voltage Meter. 0-V to 2-V voltmeter

5.1.3 Loads

LOAD1: Output Load. Electronic load set for Constant Current or Constant Resistance capable of 0 Adc to 4 Adc at 1.20 Vdc. Connect LOAD1 to J2 as shown in Figure 2.

5.1.4 Oscilloscope

For Output Voltage Ripple: Oscilloscope must be an analog or digital oscilloscope set for ac-coupled measurement with a 20-MHz bandwidth limiting. Use 20-mV/division vertical resolution, 1-µs/division horizontal resolution.

For Switching Waveforms: Oscilloscope must be an analog or digital oscilloscope set for dc-coupled measurement with 20-MHz bandwidth limiting. Use 2-V/division or 5-V/division vertical resolution and 1-µs/division horizontal resolution.

5.1.5 Recommended Wire Gauge

VIN to J1: The connection between the source voltage (VIN) and J1 of TPS53114EVM-541 can carry as much as 1 Adc of current. The minimum recommended wire size is AWG 18 with the total length of wire less than 4 feet (2-foot input, 2-foot return).

J2 to LOAD1: The connection between the source voltage (VIN) and J1 of TPS53114EVM-541 can carry as much as 4 Adc of current. The minimum recommended wire size is AWG 16 with the total length of wire less than 2 feet (1-foot input, 1-foot return).

5.1.6 Other

Fan: The TPS53114EVM-541 evaluation module includes components that can become hot to the touch when operating. This evaluation module is not enclosed in order to allow probing of circuit nodes; therefore, a small fan capable of 200–400 lfm is recommended to reduce component temperatures when operating.

5.2 Equipment Setup

Figure 2 is the recommended basic test setup to evaluate the TPS53114EVM-541. Note that although the return for J1 and JP2 is the same system ground, the connections must remain separate as shown in Figure 2.

5.2.1 Procedure

1. When working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses also must be worn.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 1 A maximum. Ensure that V_{IN} is set initially to 0 V and connected as shown in Figure 2.
3. Connect VIN to J1 (Figure 2).
4. Connect ammeter A1 between VIN and J1 (Figure 2).
5. Connect voltmeter V1 to TP1 and TP2(Figure 2).
6. Connect voltmeter V2 to TP3 and TP4 (Figure 2).
7. Connect oscilloscope probes to desired test points per Table 2.
8. Position fan as shown in Figure 2 and turn it on, ensuring that the air blows directly across the evaluation module.

5.2.2 Diagram

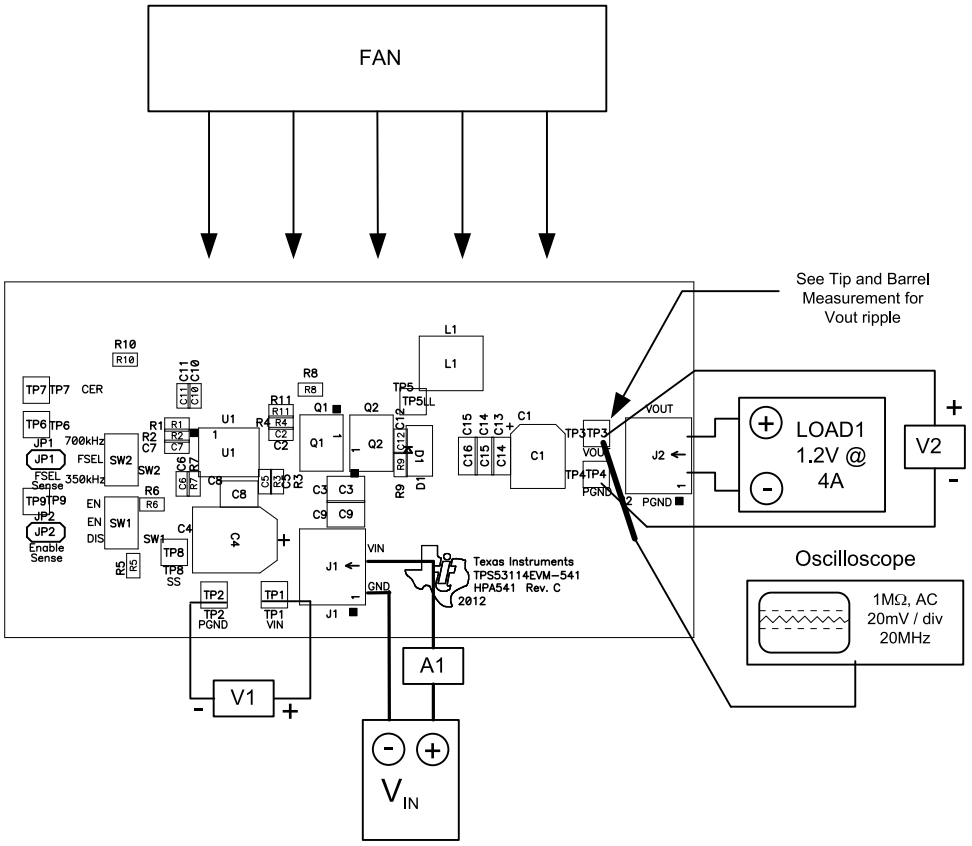


Figure 2. TPS53114EVM-541 Recommended Test Setup

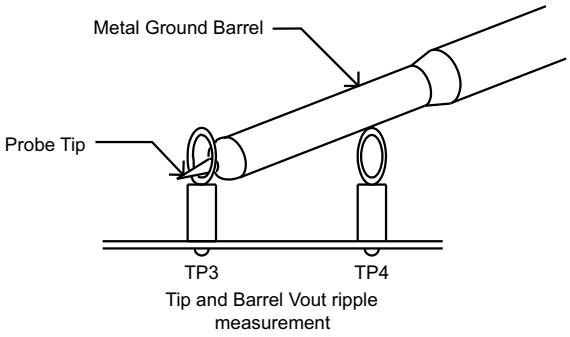


Figure 3. Output Ripple Measurement – Tip and Barrel Using TP3 and TP4

5.3 Start-Up/Shutdown Procedure

1. Verify switch positions:
   (a) SW1 DIS
   (b) SW2 350 kHz or 700 kHz as desired
2. Increase VIN from 0 Vdc to 12 Vdc.
3. Vary LOAD1 from 0 Adc to 4 Adc.
4. Vary VIN from 5 V to 22 V.
5. Decrease VIN to 0 V.
6. Decrease LOAD1 to 0 A.

5.4 Output Ripple Voltage Measurement Procedure

1. Follow Section 5.3 Steps 1-4 to set VIN and LOAD1 to desired operating condition.
2. Connect oscilloscope probe with exposed metal barrel to TP3 and TP4 per Figure 3.
3. Set oscilloscope per Section 5.1.4.
4. Follow Section 5.3 Steps 6 and 7 to power down.

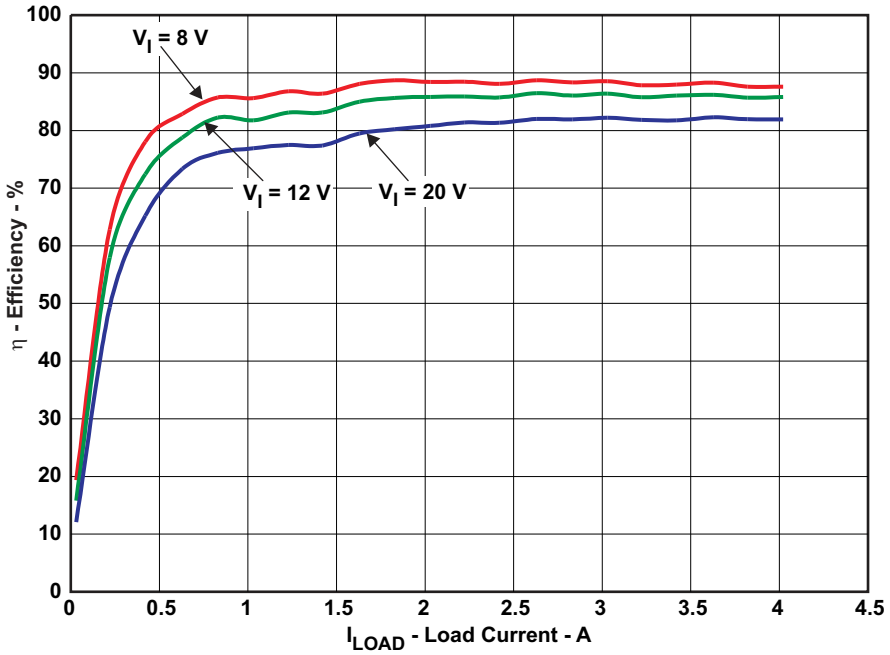
5.5 Equipment Shutdown

1. Shut down oscilloscope.
2. Shut down LOAD1.
3. Shut down VIN.
4. Shut down fan.

6 TPS53114EVM-541 Test Data

Figure 4 through Figure 7 present typical performance curves for the TPS53114EVM-541. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

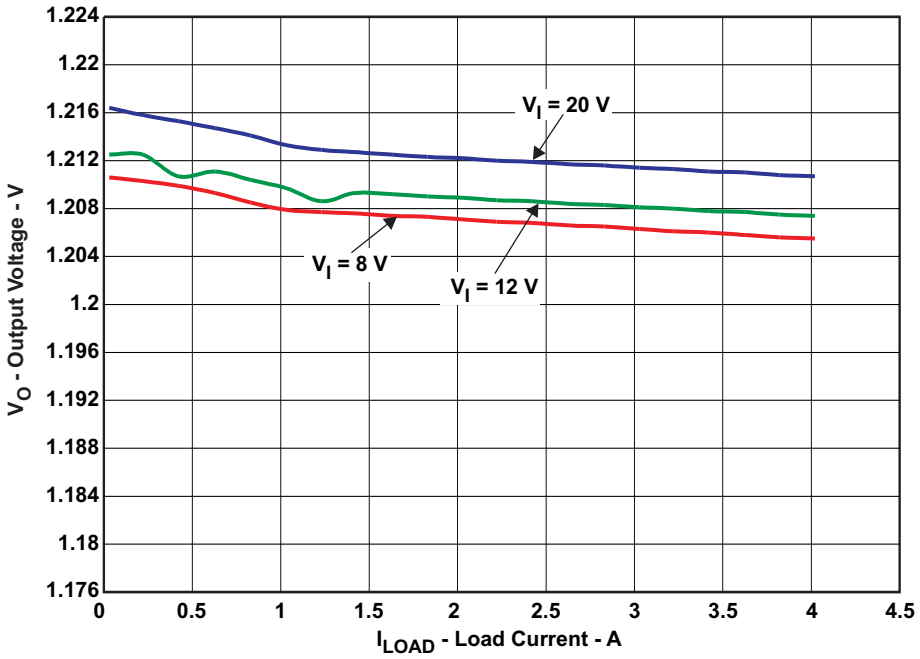
6.1 Efficiency



V_{IN} = 8 V – 20 V, V_{OUT} = 1.20 V, I_{OUT} = 4 A, SW2 = 350 kHz

Figure 4. TPS53114EVM-541 Efficiency Versus Load Current

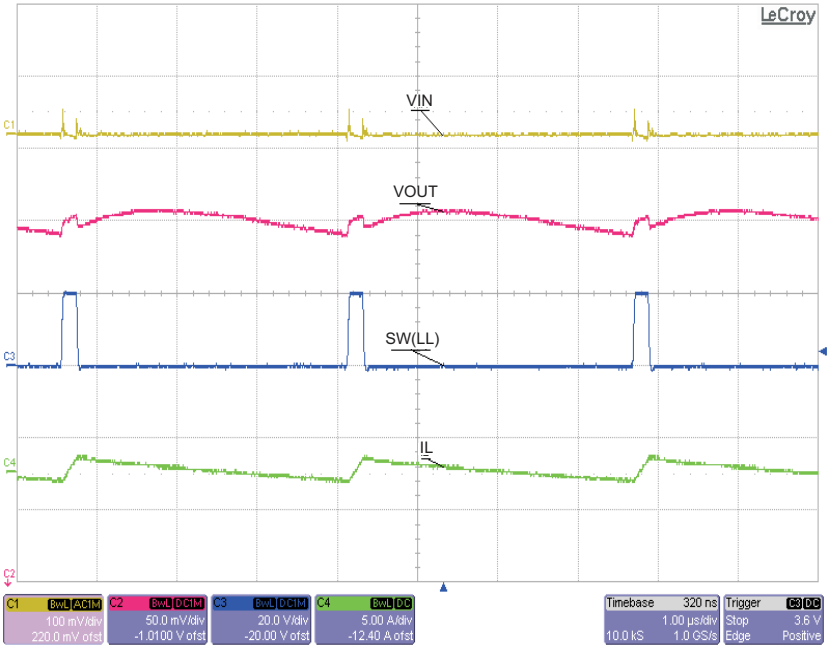
6.2 Line and Load Regulation



V_{IN} = 8 V – 20 V, V_{OUT} = 1.20 V, I_{OUT} = 4 A

Figure 5. TPS53114EVM-541 Output Voltage Versus Load Current

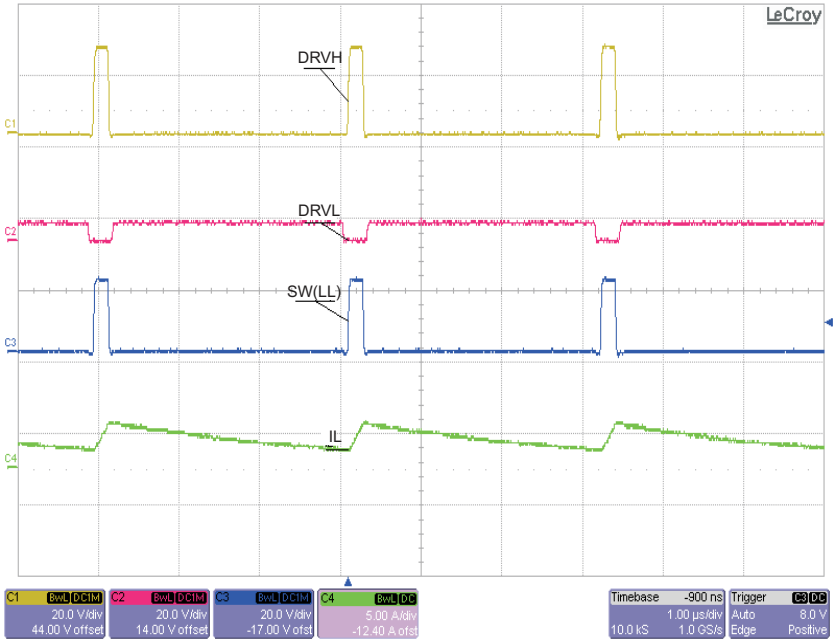
6.3 Output Voltage Ripple



V_{IN} = 20 V, V_{OUT} = 1.20 V, I_{OUT} = 2 A, SW2 = 350 kHz

Figure 6. TPS53114EVM-541 Output Voltage Ripple

6.4 Switch Node



V_{IN} = 20 V, I_{OUT} = 4 A, SW2 = 350 kHz
Ch1: DRVH (Pin 4 Q1), Ch2: DRVL (Pin 4 Q2) , Ch3: LL (TP5), Ch4: L1 Series Current

Figure 7. TPS53114EVM-541 Switching Waveforms

7 TPS53114EVM-541 Assembly Drawings and Layout

The following figures (Figure 8 through Figure 12) show the design of the TPS53114EVM-541 printed-circuit board (PCB). The EVM has been designed using a 4-layer, 2-oz, copper-clad circuit board 48 cm x 93 cm with all components on the top side to easily view, probe, and evaluate the TPS53114 control integrated circuit in a practical 4-layer application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

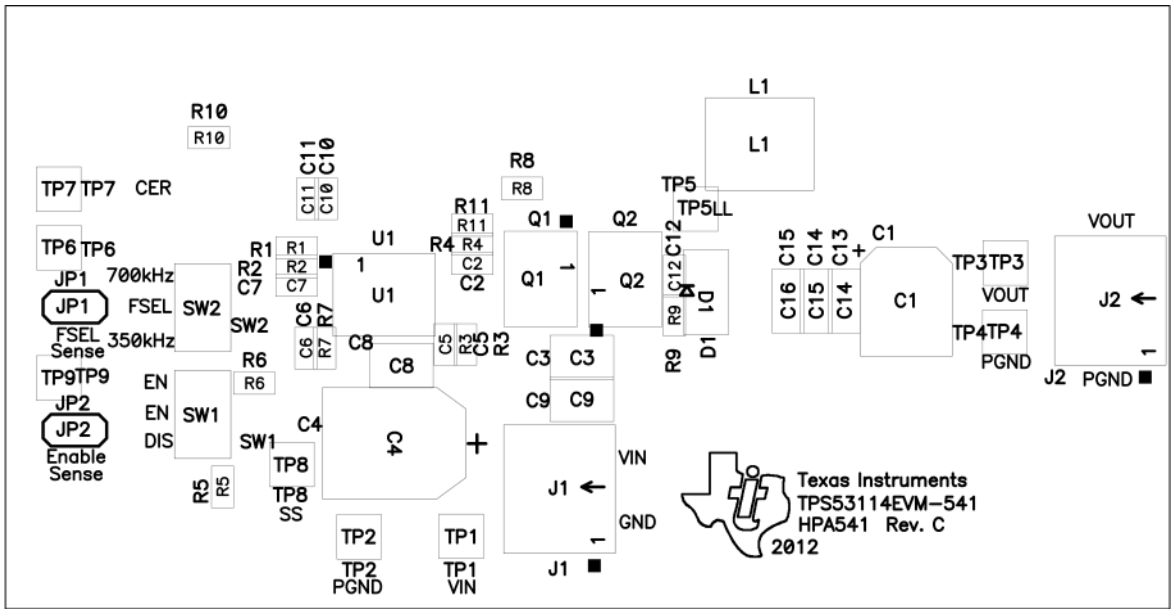


Figure 8. TPS53114EVM-541 Component Placement – Viewed From Top

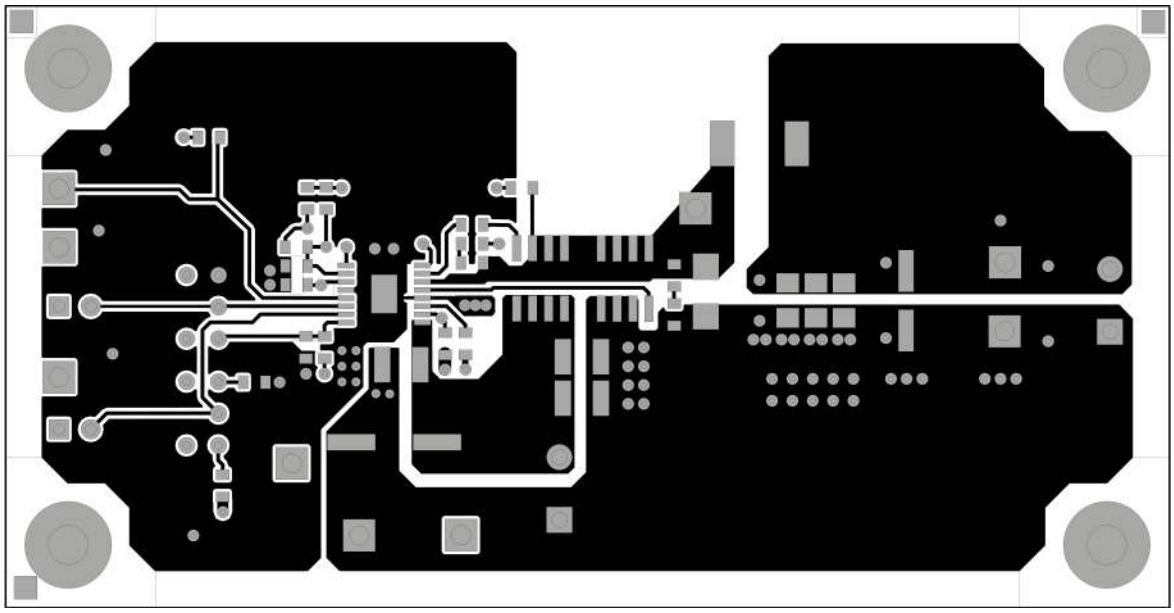


Figure 9. TPS53114EVM-541 Top Copper –Viewed From Top

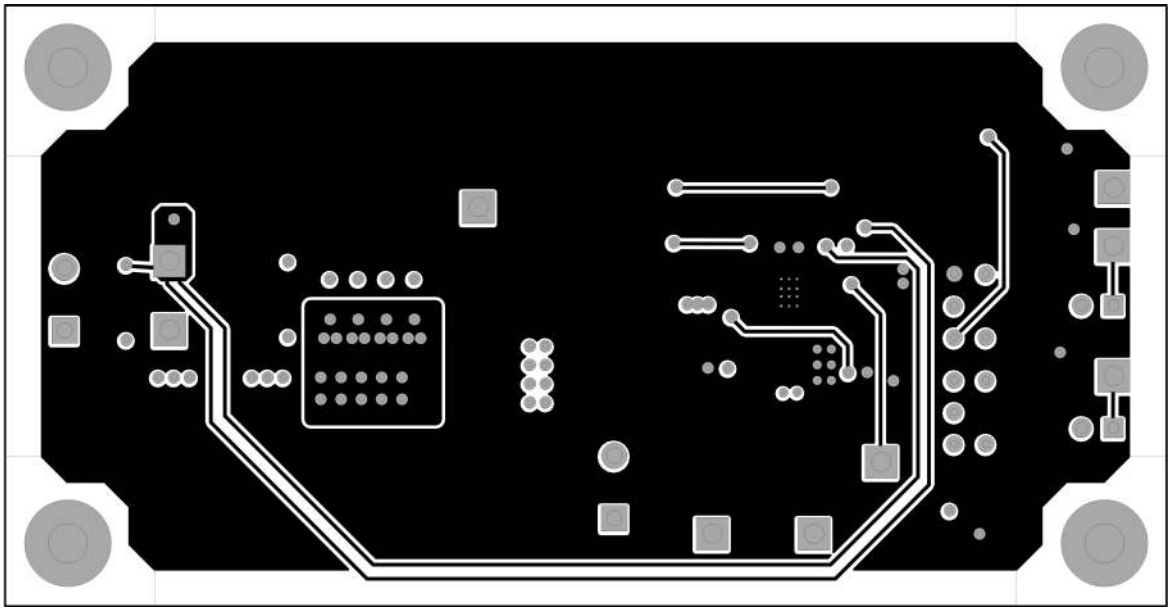


Figure 10. TPS53114EVM-541 Bottom Copper – Viewed From Bottom

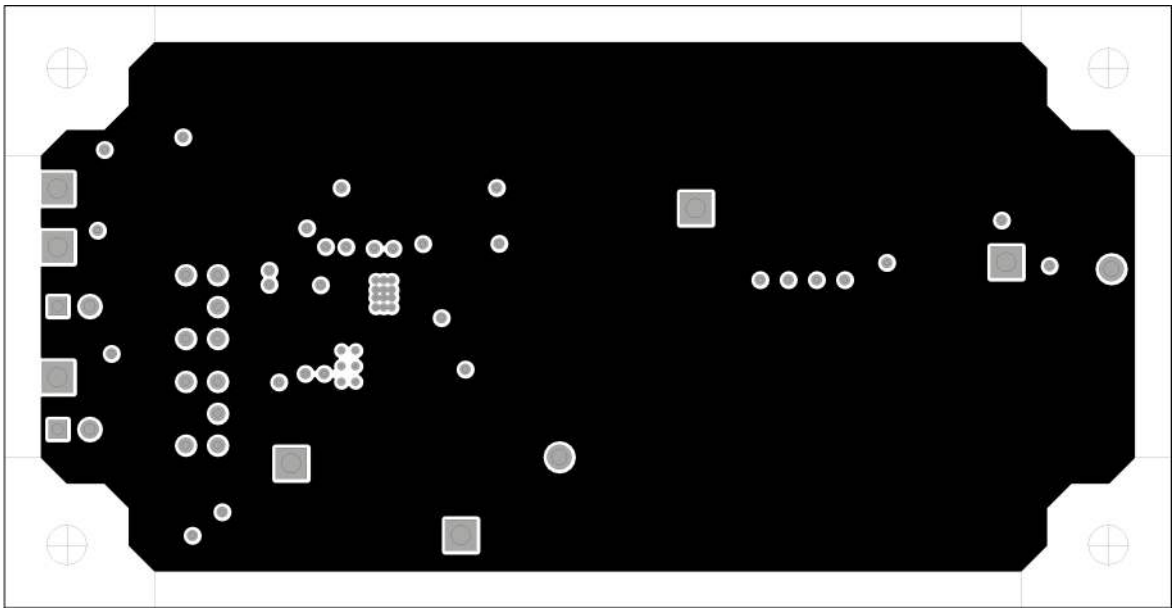


Figure 11. TPS53114EVM-541 Internal 1 - X-Ray View From Top

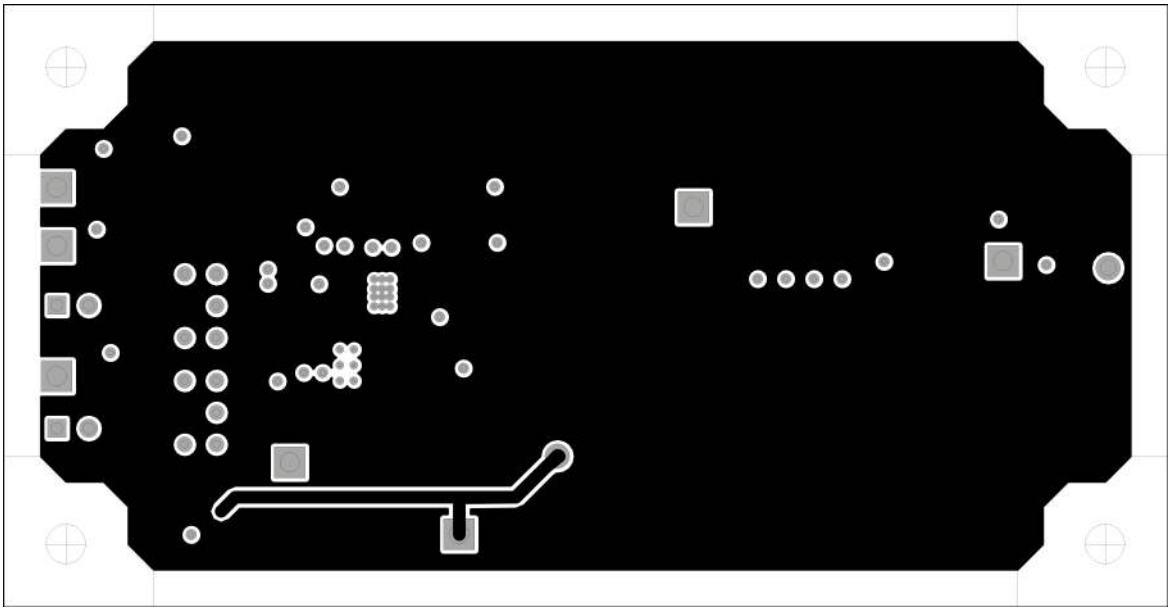


Figure 12. TPS53114EVM-541 Internal 2 – X-Ray View From Top

8 TPS53114EVM-541 Bill of Materials

Table 3 presents the bill of materials used for the TPS53114EVM-541 evaluation module.

Table 3. TPS53114EVM-541 Bill of Materials

Qty.	RefDes	Value	Description	Size	Part Number	MFR
1	C1	330 µF	Capacitor, Conductive Polymer, 4.0V, 20%	F61	APXE4R0ARA331M	Nippon Chemi-Con
0	C10	OPEN	Capacitor, Ceramic, Low Inductance, 16V, X7R, 10%	0603	Std	Std
1	C11	0.1 µF	Capacitor, Ceramic, Low Inductance, 16V, X7R, 10%	0603	Std	Std

Table 3. TPS53114EVM-541 Bill of Materials (continued)

Qty.	RefDes	Value	Description	Size	Part Number	MFR
0	C12	OPEN	Capacitor, Ceramic, Low Inductance, 25V, X5R, 20%	0603	Std	Std
3	C13– C15	22 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	Std
1	C2	0.1 µF	Capacitor, Ceramic, Low Inductance, 16V, X7R, 20%	0603	Std	Std
2	C3, C9	10 µF	Capacitor, Ceramic, 25V, X7R, 20%	1210	Std	Std
0	C4	OPEN	Capacitor, Aluminum, 25V, 20%	0.328 x 0.328 inch	Std	Panasonic
1	C5	4.7 µF	Capacitor, Ceramic, Low Inductance, 6.3V, X5R, 20%	0603	Std	Std
1	C6	1.0 µF	Capacitor, Ceramic, Low Inductance, 16V, X7R, 10%	0603	Std	Std
1	C7	4700 pF	Capacitor, Ceramic, Low Inductance, 25V, X7R, 10%	0603	Std	Std
1	C8	22 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
0	D1	OPEN	Diode, Schottky	SMA	Std	Std
2	J1, J2	1729018	Header, 2-pin Vertical, 5.0mm pitch, 300V 10A	8.10 x 10.00 mm	1729018	Phoenix Contact
2	JP1, JP2	PEC03SAAN	Header, 2-pin, 100mil spacing	0.100 inch x 2	PEC03SAAN	Sullins
1	L1	1.5 µH	Inductor, SMT, 11A, 9.7 mΩ	0.256 x 0.280 inch	SPM6530T-1R5M100	TDK
1	Q1	FDS8878	Transistor, MOSFET, N-Chan, 30V, 11.6A, Rds 10 mΩ	SO8	FDS8878	Fairchild
1	Q2	FDS8690	Transistor, MOSFET, N-Chan, 30V, 11.6A, Rds 10 mΩ	SO8	FDS8690	Fairchild
1	R1	5.62k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	1.54k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	4.42k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R4, R11	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R5, R6	1.00k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7, R12	OPEN	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R9	OPEN	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	SW1, SW2	G13AP-RO	Switch, ON-OFF-ON Mini Toggle	0.28 x 0.18 inch	G13AP-RO	NKK
2	TP1, TP3	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
2	TP2, TP4	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
5	TP5– TP9	5012	Test Point, White, Thru Hole	0.125 x 0.125 inch	5012	Keystone
1	U1*	TPS53114PWP	IC, Adaptive on-time D-CAP2 Mode Synchronous Buck Controller.	HTSSOP-16	TPS53114PWP	TI
2	–		Shunt, 100-mil, Black	0.1	929950-00	3M
1	–		PCB, 1.89 In x 3.66 In x 0.063 In		HPA541	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 22 V and the output voltage range of 1 V to 2 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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