# 450MHz Differential Twisted-Pair Drivers

## EL5173, EL5373

The EL5173 and EL5373 are single and triple high bandwidth amplifiers with a fixed gain of 2. They are primarily targeted for applications such as driving twisted-pair lines in component video applications. The inputs can be in either single-ended or differential form but the outputs are always in differential form.

The output common mode level for each channel is set by the associated REF pin, which has a -3dB bandwidth of over 190MHz. Generally, these pins are grounded but can be tied to any voltage reference.

All outputs are short circuit protected to withstand temporary overload condition.

The EL5173 and EL5373 are specified for operation over the full -40°C to +85°C temperature range.

## Features

• Fully differential inputs and outputs

• Differential input range ±2.3V

• 450MHz 3dB bandwidth at fixed gain of 2

• 900V/µs slew rate (EL5173)

• 1100V/µs slew rate (EL5373)

• Single 5V or dual ±5V supplies

• 40mA maximum output current

• Low power - 12mA per channel

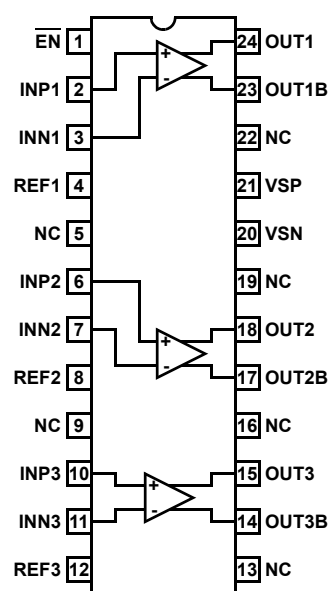• Pb-free available (RoHS compliant)

## Applications

• Twisted-pair drivers

• Differential line drivers

• VGA over twisted-pairs

• ADSL/HDSL drivers

• Single-ended to differential amplification

• Transmission of analog signals in a noisy environment

## Pinouts



EL5173
(8 LD SOIC, MSOP)
TOP VIEW
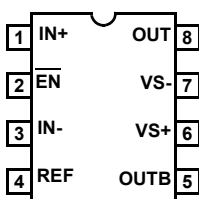
EL5373
(24 LD QSOP)
TOP VIEW

# Pin Descriptions

| EL5173 | | EL5373 | | |
|---|---|---|---|---|
| PIN NUMBER | PIN NAME | PIN NUMBER | PIN NAME | PIN FUNCTION |
| 1 | IN+ | 2, 6, 10 | INP1, INP2, INP3 | Non-inverting inputs |
| 2 | $\overline{EN}$ | 1 | $\overline{EN}$ | ENABLE |
| 3 | IN- | 3, 7, 11 | INN1, INN2, INN3 | Inverting inputs, note that on EL5173, this pin is also the REF pin |
| 4 | REF | 4, 8, 12 | REF1, REF2, REF3 | Reference inputs, sets common-mode output voltage |
| 5 | OUTB | 14, 17, 23 | OUT3B, OUT2B, OUT1B | Inverting outputs |
| 6 | VS+ | 21 | VSP | Positive supply |
| 7 | VS- | 20 | VSN | Negative supply |
| 8 | OUT | 15, 18, 24 | OUT3, OUT2, OUT1 | Non-inverting outputs |
| - | NC | 5, 9, 13, 16, 19, 22 | NC | No connect; grounded for best crosstalk performance |

# Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|
| EL5173ISZ | 5173ISZ | 8 Ld SOIC | M8.15E |
| EL5173IYZ (No longer available, recommended replacement: EL5173ISZ) | BAAYA | 8 Ld MSOP | M8.118A |
| EL5373IUZ | EL5373IUZ | 24 Ld QSOP | MDP0040 |

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for EL5173, EL5373. For more information on MSL please see tech brief TB363.

## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply Voltage ($V_S$+ to $V_S$-) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12.6V
Supply Voltage Slew Rate . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .1V/µs max.
Supply Voltage Rate-of-rise (dV/dT) . . . . . . . . . . . . . . . . . . . . . . . . . . 1V/µs
Input Voltage (IN+, IN- to $V_S$+, $V_S$-) . . . . . . . . . . . . $V_S$- - 0.3V to $V_S$+ + 0.3V
Differential Input Voltage (IN+ to IN-). . . . . . . . . . . . . . . . . . . . . . . . . . ±4.8V
Maximum Output Current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±60mA

## Thermal Information

Operating Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .+135°C
Recommended Operating Temperature . . . . . . . . . . . . . . .-40°C to +85°C
Storage Temperature Range. . . . . . . . . . . . . . . . . . . . . . . . .-65°C to +150°C
Power Dissipation. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . See Curves
Pb-Free Reflow Profile . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . see link below
[http://www.intersil.com/pbfree/Pb-FreeReflow.asp](http://www.intersil.com/pbfree/Pb-FreeReflow.asp)

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

*IMPORTANT NOTE:  All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications   $V_S$+ = +5V, $V_S$- = -5V, $T_A$ = +25°C, $V_{IN}$ = 0V, $R_{LD}$ = 200Ω, $C_{LD}$ = 1pF, Unless Otherwise Specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| BW | -3dB Bandwidth | | | 450 | | MHz |
| BW | ±0.1dB Bandwidth | | | 60 | | MHz |
| SR | Slew Rate - EL5173 | $V_{OUT}$ = 2$V_{P-P}$, 20% to 80% | 750 | 900 | | V/µs |
| | Slew Rate - EL5373 | $V_{OUT}$ = 2$V_{P-P}$, 20% to 80% | 900 | 1100 | | V/µs |
| $t_{STL}$ | Settling Time to 0.1% | $V_{OUT}$ = 2$V_{P-P}$ | | 10 | | ns |
| OS | Overshoot | $V_{ODP-P}$ = 2V | | 10 | | % |
| $t_{OVR}$ | Output Overdrive Recovery Time | | | 10 | | ns |
| $V_{REF}$BW (-3dB) | $V_{REF}$ -3dB Bandwidth | $A_V$ =1, $C_{LD}$ = 2.7pF | | 190 | | MHz |
| $V_{REF}$SR+ | $V_{REF}$ Slew Rate - Rise | $V_{OUT}$ = 2$V_{P-P}$, 20% to 80% | | 200 | | V/µs |
| $V_{REF}$SR- | $V_{REF}$ Slew Rate - Fall | $V_{OUT}$ = 2$V_{P-P}$, 20% to 80% | | 125 | | V/µs |
| $V_N$ | Input Voltage Noise | f = 10kHz | | 25 | | nV/√Hz |
| HD2 | Second Harmonic Distortion | $V_{OUT}$ = 2$V_{P-P}$, 5MHz | | 84 | | dBc |
| HD2 | Second Harmonic Distortion | $V_{OUT}$ = 2$V_{P-P}$, 20MHz | | 71 | | dBc |
| HD3 | Third Harmonic Distortion | $V_{OUT}$ = 2$V_{P-P}$, 5MHz | | 62 | | dBc |
| HD3 | Third Harmonic Distortion | $V_{OUT}$ = 2$V_{P-P}$, 20MHz | | 53 | | dBc |
| dG | Differential Gain at 3.58MHz | $R_{LD}$ = 300Ω, $A_V$ = 2 | | 0.05 | | % |
| dθ | Differential Phase at 3.58MHz | $R_{LD}$ = 300Ω, $A_V$ = 2 | | 0.08 | | ° |
| $e_S$ | Channel Separation - for EL5373 only | at 1MHz | | 90 | | dB |
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{OS}$ | Input Referred Offset Voltage | | | ±3 | ±30 | mV |
| $I_{IN}$ | Input Bias Current ($V_{IN}$, $V_{INB}$) | EL5173 | -21 | -11 | -5 | µA |
| | | EL5373 | -21 | -13 | -5 | µA |
| $I_{REF}$ | INput Bias Current at REF | $V_{REF}$ = +3.2V | 1 | | 5 | µA |
| | | $V_{REF}$ = -3.2V | -1 | | +1 | µA |
| Gain | Gain Accuracy | $V_{IN}$ = ±1V | 1.97 | 1.99 | 2.01 | V |
| $R_{IN}$ | Differential Input Resistance | | | 150 | | kΩ |
| $C_{IN}$ | Differential Input Capacitance | | | 1 | | pF |
| DMIR | Differential Mode Input Range | | ±2 | ±2.3 | | V |

## Electrical Specifications
$V_S+$ = +5V, $V_S-$ = -5V, $T_A$ = +25°C, $V_{IN}$ = 0V, $R_{LD}$ = 200Ω, $C_{LD}$ = 1pF, Unless Otherwise Specified. **(Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|---|---|---|---|---|---|---|
| CMIR+ | Common Mode Positive Input Range at $V_{IN}+$, $V_{IN}-$ | | 3.1 | 3.4 | | V |
| CMIR- | Common Mode Negative Input Range at $V_{IN}+$, $V_{IN}-$ | | | -4.5 | -4.2 | V |
| $V_{REFIN}+$ | Reference Input - Positive | $V_{IN}+$ = $V_{IN}-$ = 0V | 3.3 | 3.7 | | V |
| $V_{REFIN}-$ | Reference Input - Negative | $V_{IN}+$ = $V_{IN}-$ = 0V | | -3.3 | -3 | V |
| $V_{REFOS}$ | Output Offset Relative to $V_{REF}$ | | -100 | 50 | +100 | mV |
| CMRR | Input Common Mode Rejection Ratio | $V_{IN}$ = ±2.5V | 60 | 80 | | dB |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ (EL5173) | Positive Output Voltage Swing | $R_{LD}$ = 200Ω | 3.3 | 3.67 | | V |
| | Negative Output Voltage Swing | | | -3.3 | -3 | V |
| $V_{OUT}$ (EL5373) | Positive Output Voltage Swing | $R_{LD}$ = 200Ω | 3.7 | 4 | | V |
| | Negative Output Voltage Swing | | | -3.7 | -3.4 | V |
| $I_{OUT}$(Max) | Maximum Output Current | $R_L$ = 10Ω (EL5173) | ±45 | ±55 | | mA |
| | | $R_L$ = 10Ω (EL5373) | ±40 | ±50 | | mA |
| $R_{OUT}$ | Output Impedance | | | 60 | | mΩ |
| **SUPPLY** | | | | | | |
| $V_{SUPPLY}$ | Supply Operating Range | $V_S+$ to $V_S-$ | 4.75 | | 11 | V |
| $I_{S(ON)}$ | Power Supply Current - Per Channel | | 9 | 12 | 14 | mA |
| $I_{S(OFF)}+$ (EL5173) | Positive Power Supply Current - Disabled | $\overline{EN}$ pin tied to 4.8V | 60 | 80 | 100 | μA |
| $I_{S(OFF)}-$ (EL5173) | Negative Power Supply Current - Disabled | | -150 | -120 | -90 | μA |
| $I_{S(OFF)}+$ (EL5373) | Positive Power Supply Current - Disabled | $\overline{EN}$ pin tied to 4.8V | 0.5 | 2 | 10 | μA |
| $I_{S(OFF)}-$ (EL5373) | Negative Power Supply Current - Disabled | | -150 | -120 | -90 | μA |
| PSRR | Power Supply Rejection Ratio | $V_S$ from ±4.5V to ±5.5V | 60 | 73 | | dB |
| **ENABLE** | | | | | | |
| $t_{EN}$ | Enable Time | | | 100 | | ns |
| $t_{DS}$ | Disable Time | | | 1.2 | | μs |
| $V_{IH}$ | $\overline{EN}$ Pin Voltage for Power-Up | | | | $V_S+$ - 1.5 | V |
| $V_{IL}$ | $\overline{EN}$ Pin Voltage for Shut-Down | | $V_S+$ - 0.5 | | | V |
| $I_{IH-EN}$ | $\overline{EN}$ Pin Input Current High - Per Channel | At $V_{EN}$ = 5V | | 40 | 60 | μA |
| $I_{IL-EN}$ | $\overline{EN}$ Pin Input Current Low - Per Channel | At $V_{EN}$ = 0V | -5 | -2.5 | | μA |

NOTE:

4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

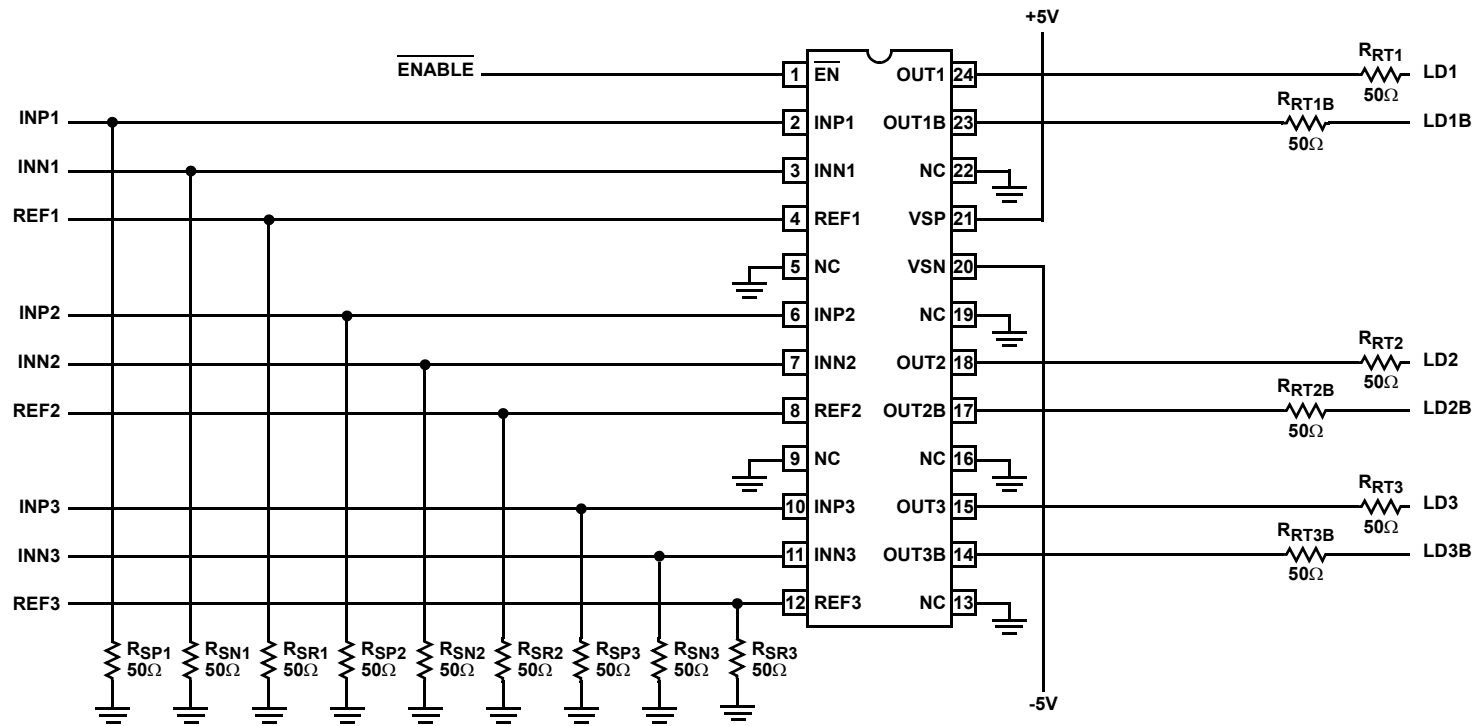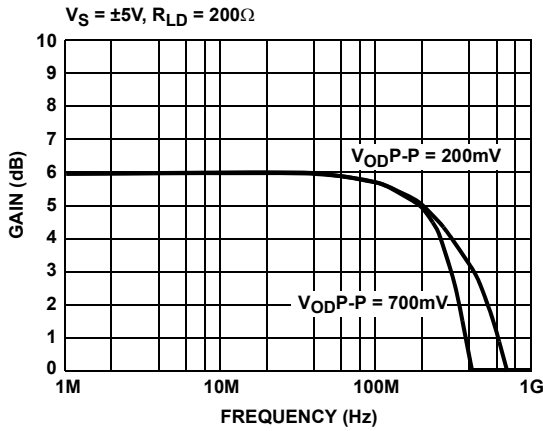# Connection Diagrams
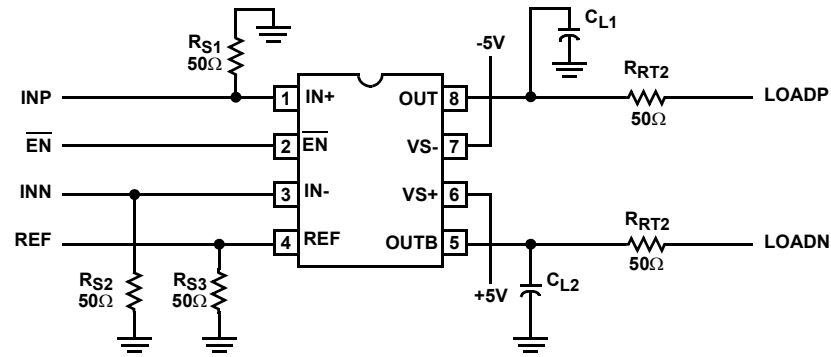


FIGURE 1. EL5173



FIGURE 2. EL5373

EL5173, EL5373

# Typical Performance Curves

$V_S = \pm5V$, $R_{LD} = 200\Omega$



**FIGURE 3. FREQUENCY RESPONSE**

$V_S = \pm5V$, $C_{LD} = 1pF$
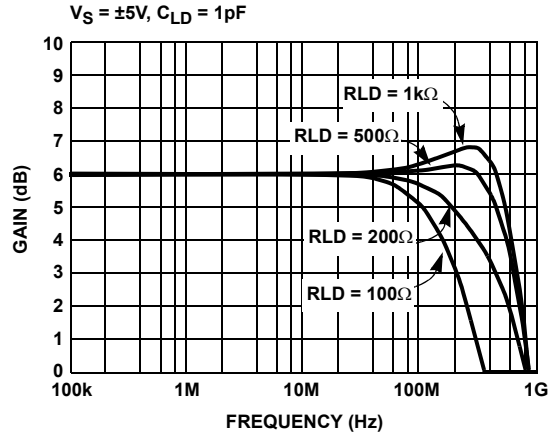


**FIGURE 4. FREQUENCY RESPONSE vs $R_{LD}$**

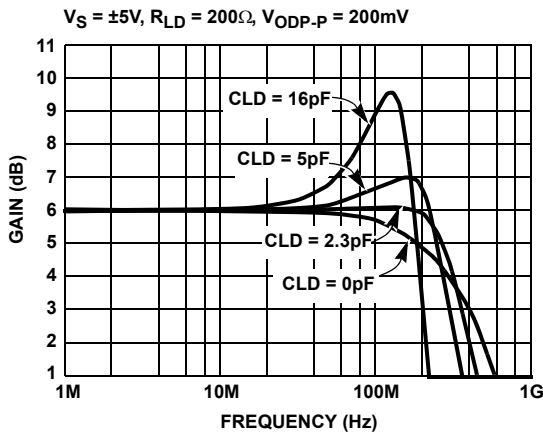$V_S = \pm5V$, $R_{LD} = 200\Omega$, $V_{ODP\text{-}P} = 200mV$



**FIGURE 5. SMALL SIGNAL FREQUENCY RESPONSE vs $C_{LD}$**
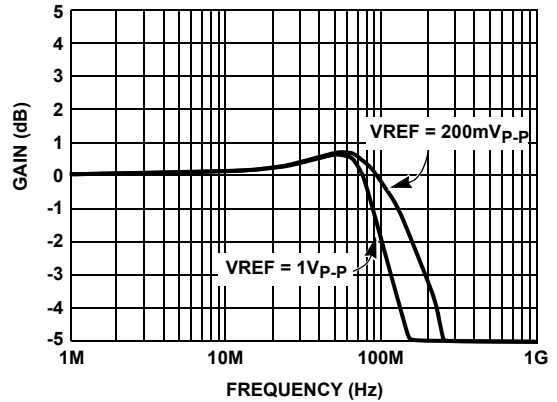


**FIGURE 6. FREQUENCY RESPONSE vs $V_{REF}$**
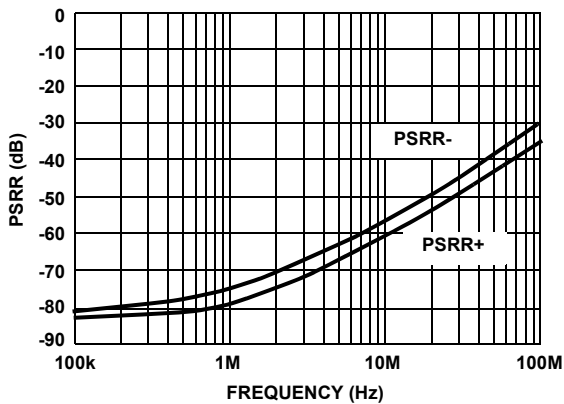


**FIGURE 7. PSRR vs FREQUENCY**
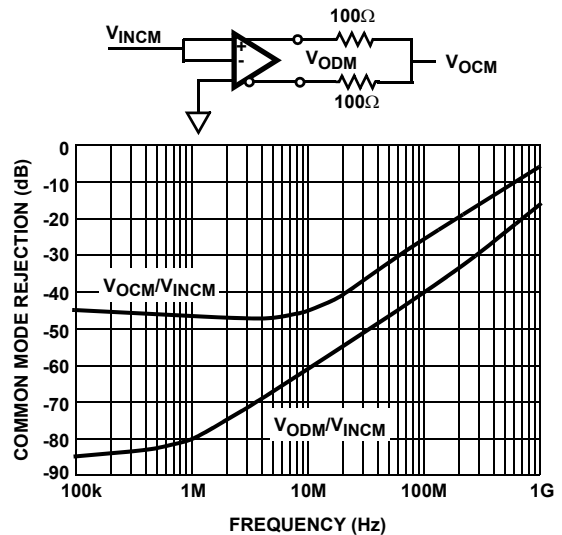


**FIGURE 8. COMMON MODE REJECTION vs FREQUENCY**

## Typical Performance Curves (Continued)
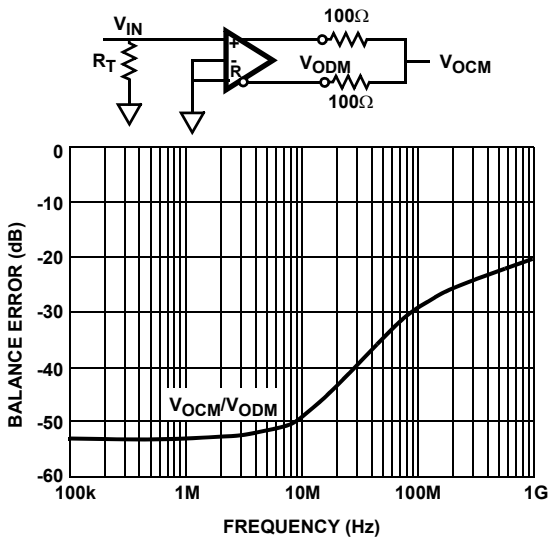


FIGURE 9. DIFFERENTIAL MODE OUTPUT BALANCE ERROR vs FREQUENCY
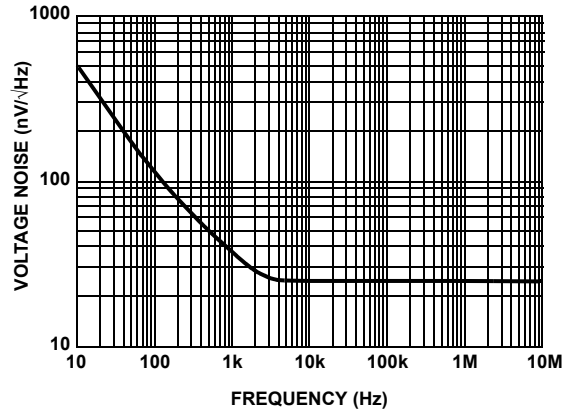


FIGURE 10. INPUT VOLTAGE NOISE vs FREQUENCY
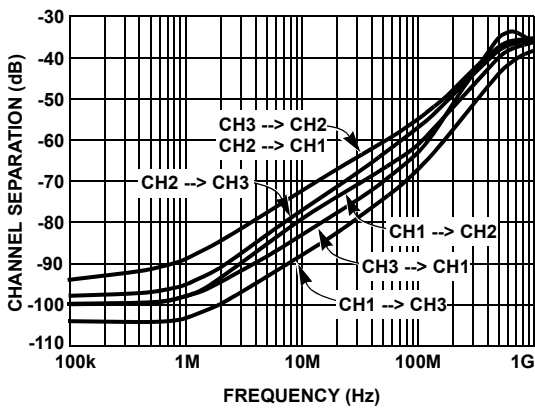


FIGURE 11. CHANNEL SEPARATION vs FREQUENCY
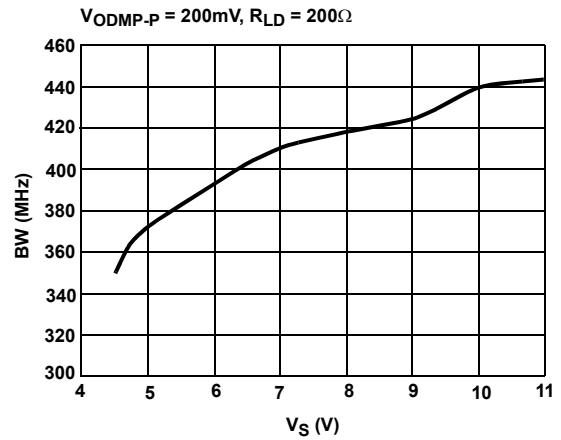


FIGURE 12. SMALL SIGNAL BANDWIDTH vs SUPPLY VOLTAGE
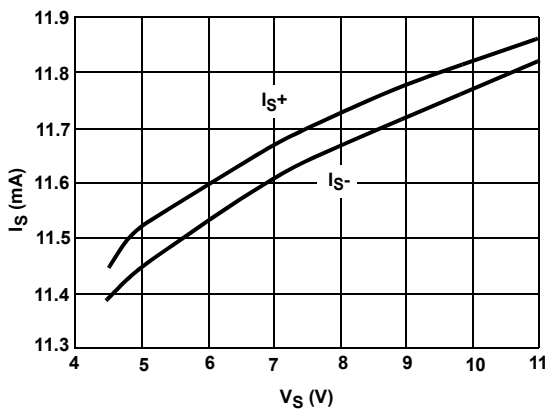


FIGURE 13. SUPPLY CURRENT vs SUPPLY VOLTAGE
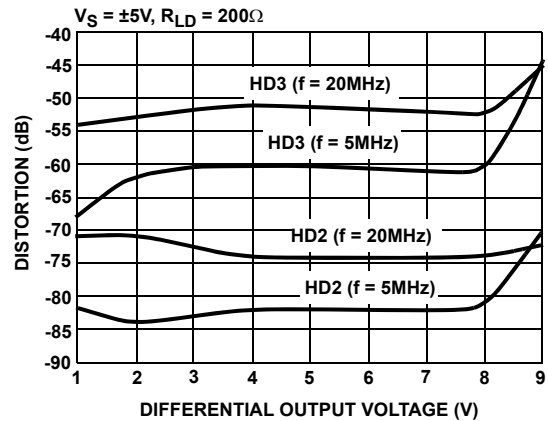


FIGURE 14. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

## Typical Performance Curves (Continued)

VS = ±5V, VODMP-P = 2V
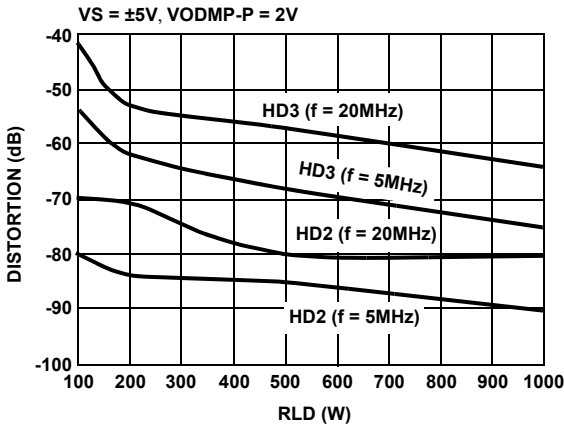


FIGURE 15. HARMONIC DISTORTION vs R_LD

$V_S$ = ±5V, $R_{LD}$ = 200$\Omega$, VODMP-P = 2V
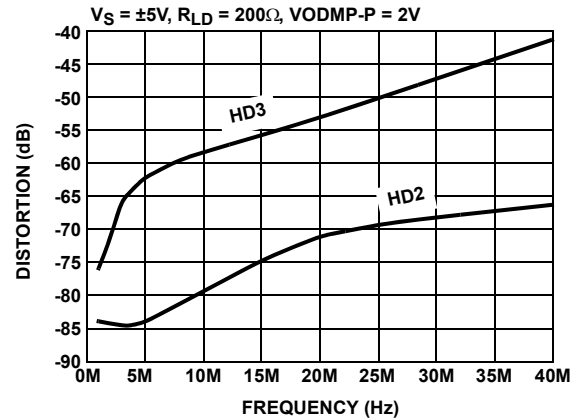


FIGURE 16. HARMONIC DISTORTION vs FREQUENCY
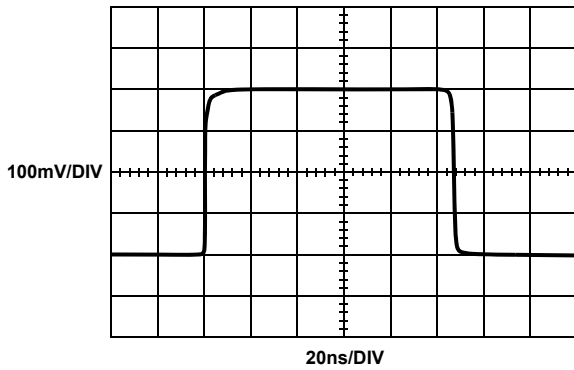


FIGURE 17. SMALL SIGNAL TRANSIENT RESPONSE
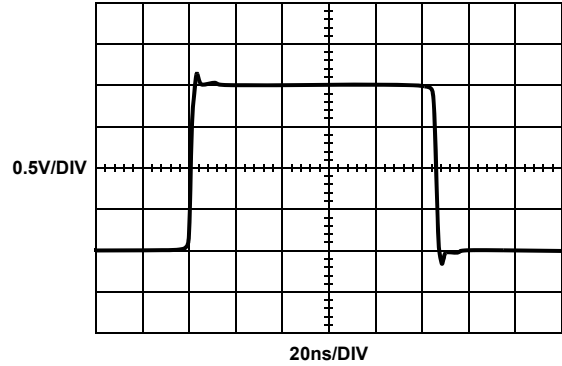


FIGURE 18. LARGE SIGNAL TRANSIENT RESPONSE
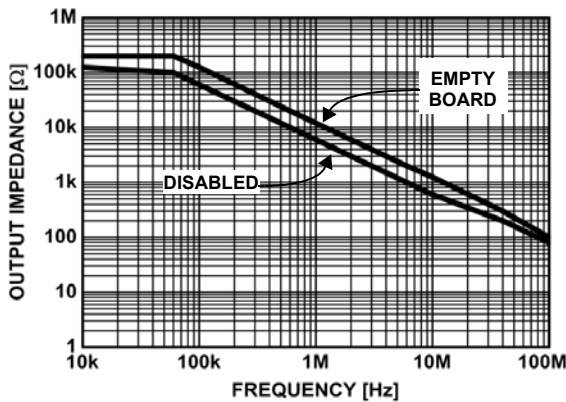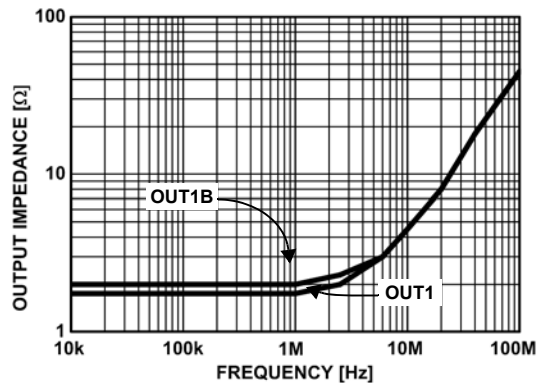


FIGURE 19. OUTPUT IMPEDANCE (DISABLED)



FIGURE 20. OUTPUT IMPEDANCE (ENABLED)
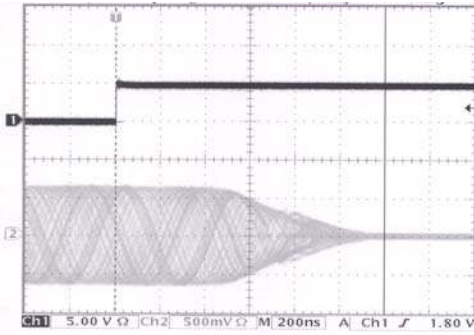
## Typical Performance Curves (Continued)
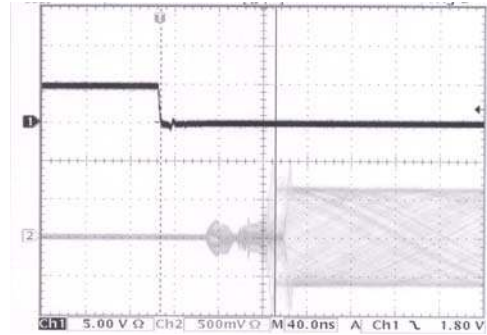


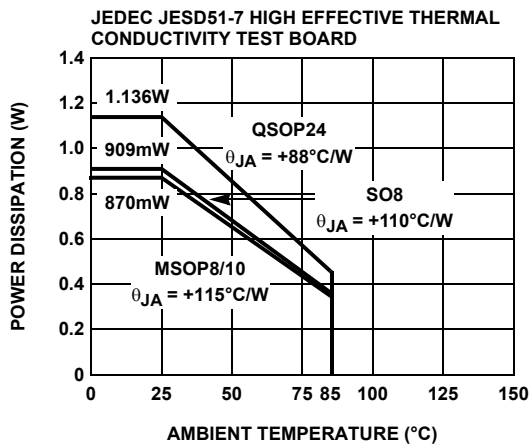FIGURE 21. DISABLED RESPONSE



FIGURE 22. ENABLED RESPONSE



FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT
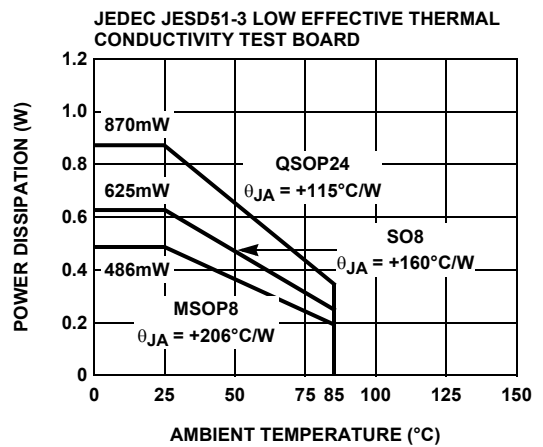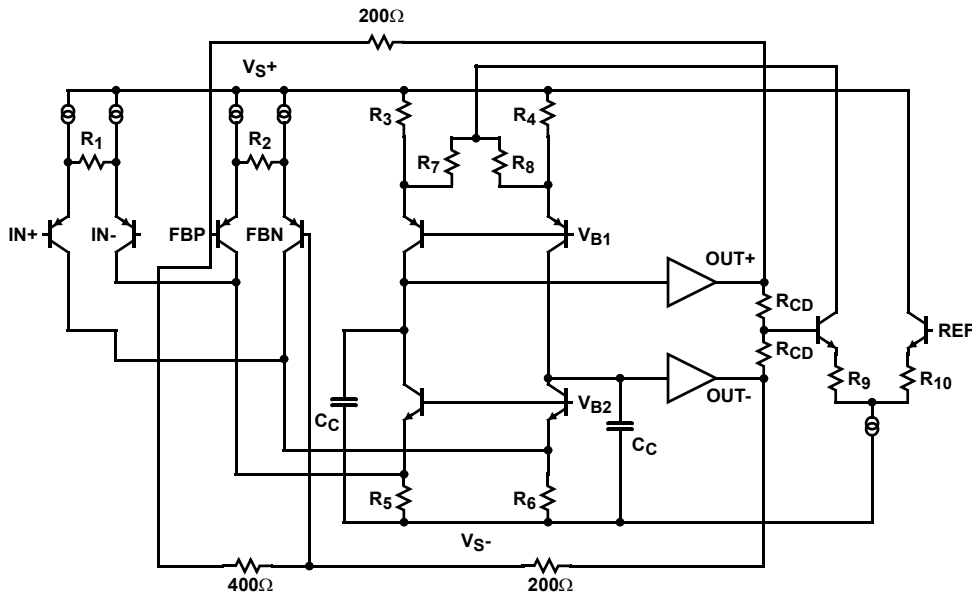TEMPERATURE



FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT
TEMPERATURE

## Simplified Schematic

# Description of Operation and Application Information

## Product Description

The EL5173 and EL5373 are wide bandwidth, low power and single/differential ended to differential output amplifiers. They have a fixed gain of 2. The EL5173 is a single channel differential amplifier. The EL5373 is a triple channel differential amplifier. The EL5173 and EL5373 have a -3dB bandwidth of 450MHz while driving a 200$\Omega$ differential load. The EL5173 and EL5373 are available with a power-down feature to reduce the power while the amplifiers are disabled.

## Input, Output and Supply Voltage Range

The EL5173 and EL5373 have been designed to operate with a single supply voltage of 5V to 10V or split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.5V to 3.4V for ±5V supply. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the REF pin is from -3.3V to 3.7V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal to become distorted.

The output of the EL5173 and EL5373 can swing from -3.3V to 3.6V at 200$\Omega$ differential load at ±5V supply. As the load resistance becomes lower, the output swing is reduced.

## Differential and Common Mode Gain Settings

As shown in the "Simplified Schematic" on page 9, since the feedback resistors RF and the gain resistor are integrated with 200$\Omega$ and 400$\Omega$, the EL5173 and EL5373 have a fixed gain of 2. The common mode gain is always one.

## Driving Capacitive Loads and Cables

The EL5173 and EL5373 can drive 16pF differential capacitor in parallel with 200$\Omega$ differential load with less than 3.5dB of peaking. If less peaking is desired in applications, a small series resistor (usually between 5$\Omega$ to 50$\Omega$) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

## Disable/Power-Down

The EL5173 and EL5373 can be disabled and placed their outputs in a high impedance state. The turn-off time is about 1.2μs and the turn-on time is about 100ns. When disabled, the amplifier's supply current is reduced to 40μA for $I_S$+ and 2.5μA for $I_S$- typically, thereby effectively eliminating the power consumption. The amplifier's power-down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied logic signal is relative to $V_S$+ pin. Letting the $\overline{EN}$ pin float or applying a signal that is less than 1.5V below $V_S$+ will enable the amplifier. The amplifier will be disabled when the signal at $\overline{EN}$ pin is above $V_S$+ - 0.5V.

## Output Drive Capability

The EL5173 and EL5373 have internal short circuit protection. Its typical short circuit current is ±55mA. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnect.

## Power Dissipation

With the high output drive capability of the EL5173 and EL5373, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \qquad \text{(EQ. 1)}$$

Where:

- $T_{JMAX}$ = Maximum junction temperature
- $T_{AMAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or as expressed in Equation 2:

$$PD = i \times \left( V_{STOT} \times I_{SMAX} + (V_{STOT} - \Delta V_O) \times \frac{\Delta V_O}{R_{LD}} \right) \qquad \text{(EQ. 2)}$$

Where:

$V_{STOT}$ = Total supply voltage = $V_S$+ - $V_S$-

$I_{SMAX}$ = Maximum quiescent supply current per channel

$\Delta V_O$ = Maximum differential output voltage of the application

$R_{LD}$ = Differential load resistance

$I_{LOAD}$ = Load current

i = Number of channels

By setting the two $PD_{MAX}$ equations equal to each other, we can solve the output current and $R_{LOAD}$ to avoid the device overheat.

_intersil_

## Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the $V_S$- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from $V_S$+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the $V_S$- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire-wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.
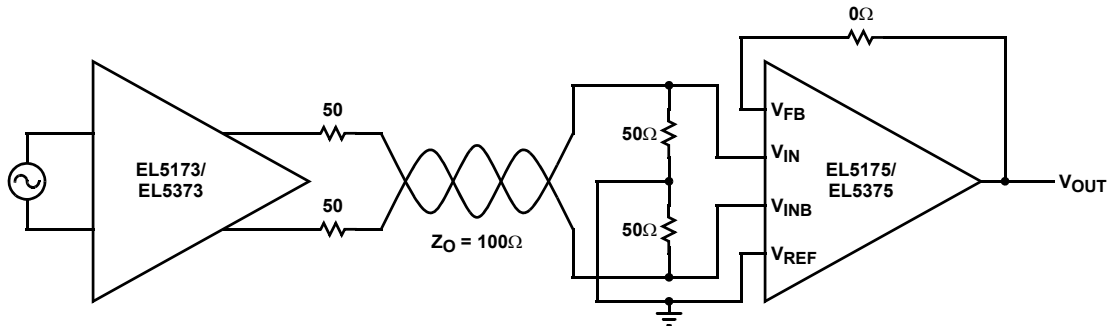
# Typical Applications



FIGURE 25. TWISTED PAIR CABLE DRIVER

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| August 25, 2015 | FN7312.10 | - Ordering Information Table on page 2.<br>- Added Revision History and About Intersil sections. |

# About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

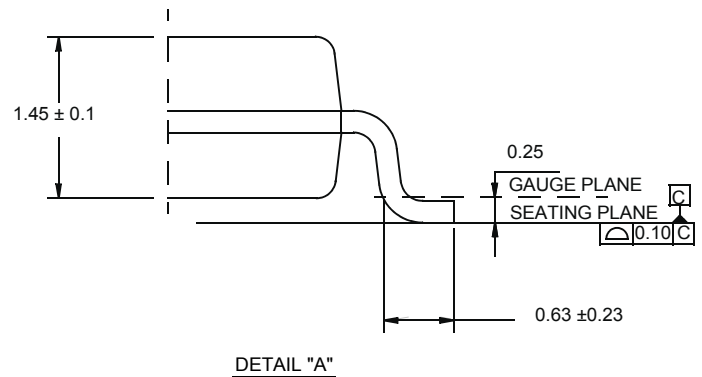You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.
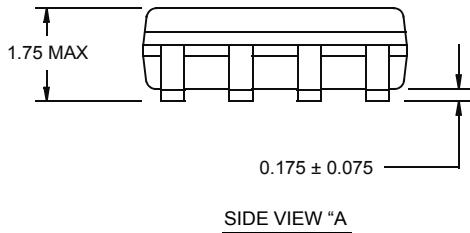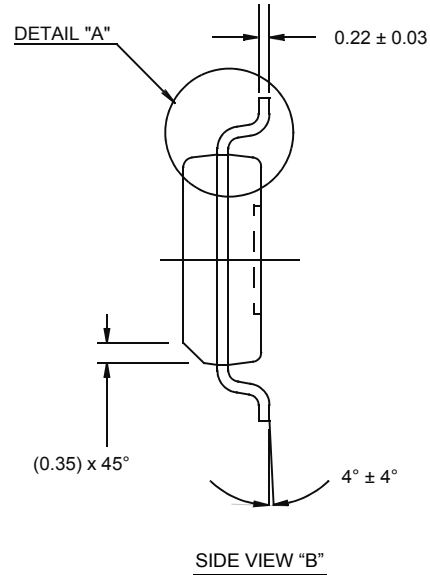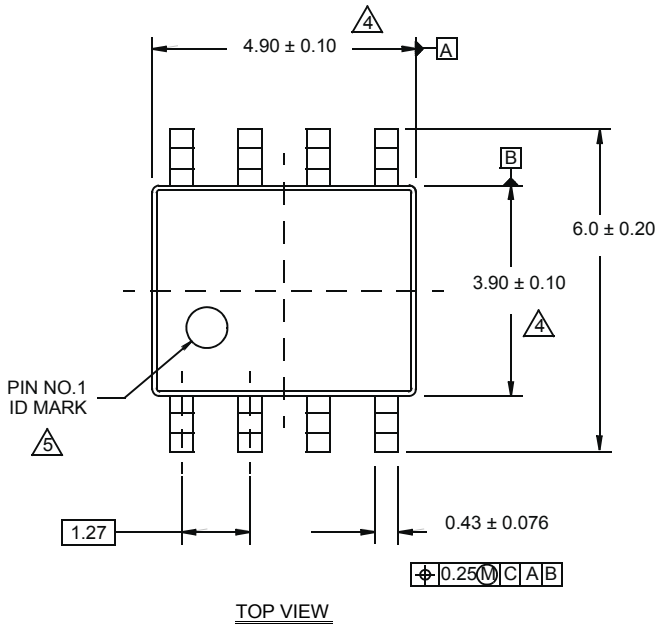
Reliability reports are also available from our website at www.intersil.com/support

# Package Outline Drawing

## M8.15E

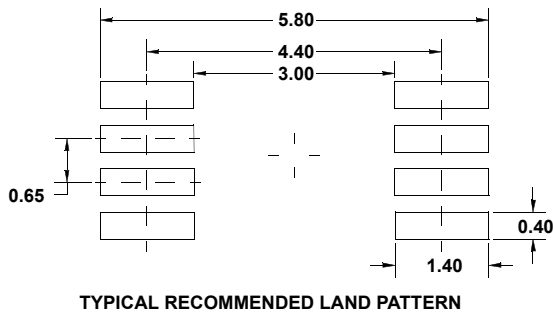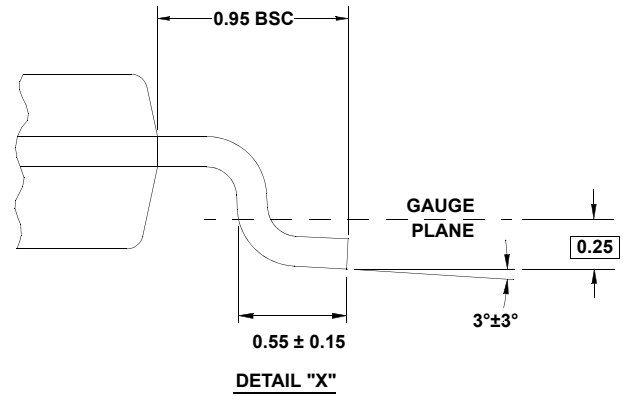**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

**Rev 0, 08/09**

TOP VIEW

SIDE VIEW "B"

DETAIL "A"

0.22 ± 0.03

(0.35) x 45°

4° ± 4°

4.90 ± 0.10

6.0 ± 0.20

3.90 ± 0.10

PIN NO.1
ID MARK

1.27

0.43 ± 0.076

0.25 (M) C A B

SIDE VIEW "A"

1.75 MAX

0.175 ± 0.075

1.45 ± 0.1

0.25
GAUGE PLANE
SEATING PLANE

0.10 C

0.63 ±0.23

DETAIL "A"

TYPICAL RECOMMENDED LAND PATTERN
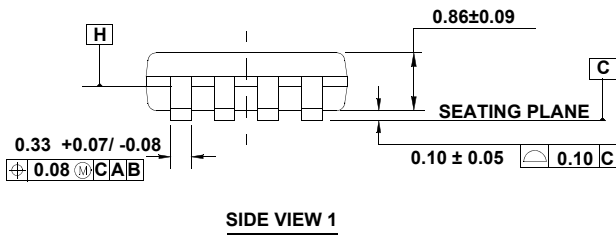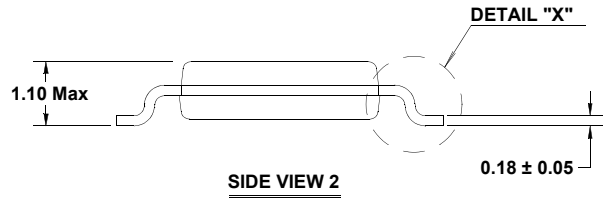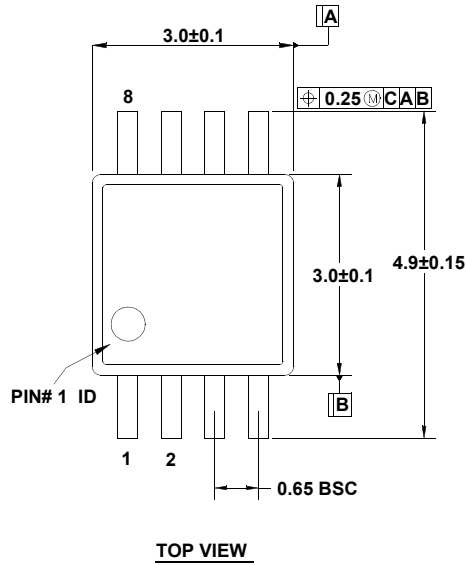
(1.27)

(0.60)

(1.50)

(5.40)
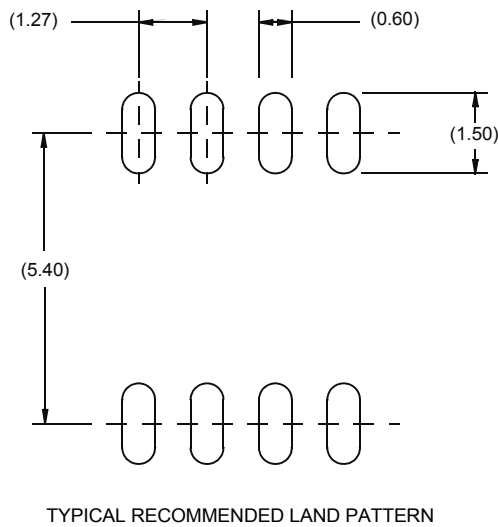
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.

5. The pin #1 identifier may be either a mold or mark feature.

6. Reference to JEDEC MS-012.

# Package Outline Drawing

## M8.118A
**8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)**
**Rev 0, 9/09**



**TOP VIEW**

A

3.0±0.1

8

⊕ 0.25 Ⓜ C A B

3.0±0.1    4.9±0.15

PIN# 1 ID

B

1    2

0.65 BSC

**SIDE VIEW 2**

DETAIL "X"

1.10 Max

0.18 ± 0.05

**SIDE VIEW 1**

H

0.86±0.09

C

SEATING PLANE

0.33  +0.07/ -0.08

0.10 ± 0.05    ⌒ 0.10 C

⊕ 0.08 Ⓜ C A B

**DETAIL "X"**

0.95 BSC

GAUGE
PLANE

0.25

0.55 ± 0.15

3°±3°

**TYPICAL RECOMMENDED LAND PATTERN**

5.80

4.40

3.00

0.65

0.40

1.40

**NOTES:**

1. Dimensions are in millimeters.

2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.

3. Plastic or metal protrusions of 0.15mm max per side are not included.

4. Plastic interlead protrusions of 0.25mm max per side are not included.

5. Dimensions "D" and "E1" are measured at Datum Plane "H".

6. This replaces existing drawing # MDP0043 MSOP 8L.

## *Quarter Size Outline Plastic Packages Family (QSOP)*
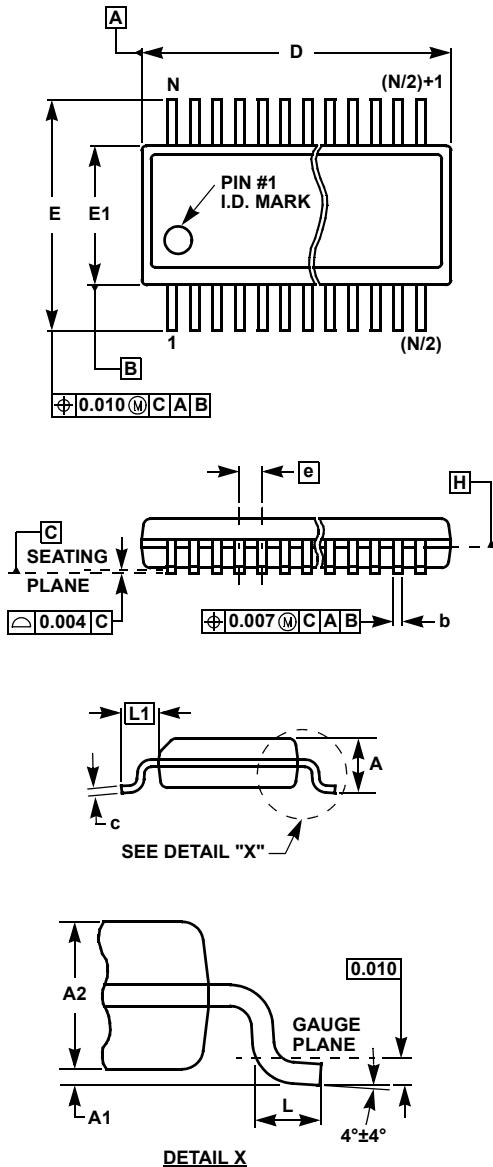


### MDP0040
**QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY**

| SYMBOL | INCHES | | | TOLERANCE | NOTES |
|--------|--------|--------|--------|-----------|-------|
| | QSOP16 | QSOP24 | QSOP28 | | |
| A | 0.068 | 0.068 | 0.068 | Max. | - |
| A1 | 0.006 | 0.006 | 0.006 | ±0.002 | - |
| A2 | 0.056 | 0.056 | 0.056 | ±0.004 | - |
| b | 0.010 | 0.010 | 0.010 | ±0.002 | - |
| c | 0.008 | 0.008 | 0.008 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | ±0.004 | 2, 3 |
| e | 0.025 | 0.025 | 0.025 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | Basic | - |
| N | 16 | 24 | 28 | Reference | - |

Rev. F 2/07

NOTES:
1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.