

# SN54GTL16622A, SN74GTL16622A 18-BIT LVTTTL-TO-GTL/GTL+ BUS TRANSCEIVERS

SCBS673D – AUGUST 1996 – REVISED DECEMBER 1999

- **Members of the Texas Instruments Widebus™ Family**
- **D-Type Flip-Flops With Qualified Storage Enable**
- **Translate Between GTL/GTL+ Signal Levels and LVTTTL Logic Levels**
- **Support Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **I<sub>off</sub> Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Distributed V<sub>CC</sub> and GND-Pin Configuration Minimizes High-Speed Noise**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Ceramic Quad Flat (HV) Packages**

SN74GTL16622A . . . DGG PACKAGE  
(TOP VIEW)

OEAB	1	64	CLKAB
1A1	2	63	1CEAB
GND	3	62	1CEBA
1A2	4	61	1B1
1A3	5	60	GND
GND	6	59	1B2
V <sub>CC</sub>	7	58	1B3
1A4	8	57	V <sub>CC</sub>
GND	9	56	1B4
1A5	10	55	1B5
1A6	11	54	1B6
GND	12	53	GND
1A7	13	52	1B7
1A8	14	51	1B8
GND	15	50	GND
1A9	16	49	1B9
2A1	17	48	2B1
GND	18	47	GND
2A2	19	46	2B2
2A3	20	45	2B3
GND	21	44	GND
2A4	22	43	2B4
2A5	23	42	2B5
GND	24	41	2B6
2A6	25	40	V <sub>REF</sub>
V <sub>CC</sub>	26	39	2B7
GND	27	38	2B8
2A7	28	37	GND
2A8	29	36	2B9
GND	30	35	2CEBA
2A9	31	34	2CEAB
OEBA	32	33	CLKBA

## description

The 'GTL16622A devices are 18-bit registered bus transceivers that provide LVTTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTTL signal-level translation. They are partitioned as two separate 9-bit transceivers with individual clock-enable controls and contain D-type flip-flops for temporary storage of data flowing in either direction. The devices provide an interface between cards operating at LVTTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and output edge control (OEC™).

The user has the flexibility of using this device at either GTL ( $V_{TT} = 1.2$  V and  $V_{REF} = 0.8$  V) or the preferred higher noise margin GTL+ ( $V_{TT} = 1.5$  V and  $V_{REF} = 1$  V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTTL logic levels and are 5-V tolerant.  $V_{REF}$  is the reference input voltage for the B port.



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 **TEXAS  
INSTRUMENTS**

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## description (continued)

Data flow in each direction is controlled by the output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ) and clock (CLKAB and CLKBA) inputs. The clock-enable ( $\overline{CEAB}$  and  $\overline{CEBA}$ ) inputs are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if  $\overline{CEAB}$  is low. When  $\overline{OEAB}$  is low, the outputs are active. When  $\overline{OEAB}$  is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses  $\overline{OEBA}$ , CLKBA, and  $\overline{CEBA}$ .

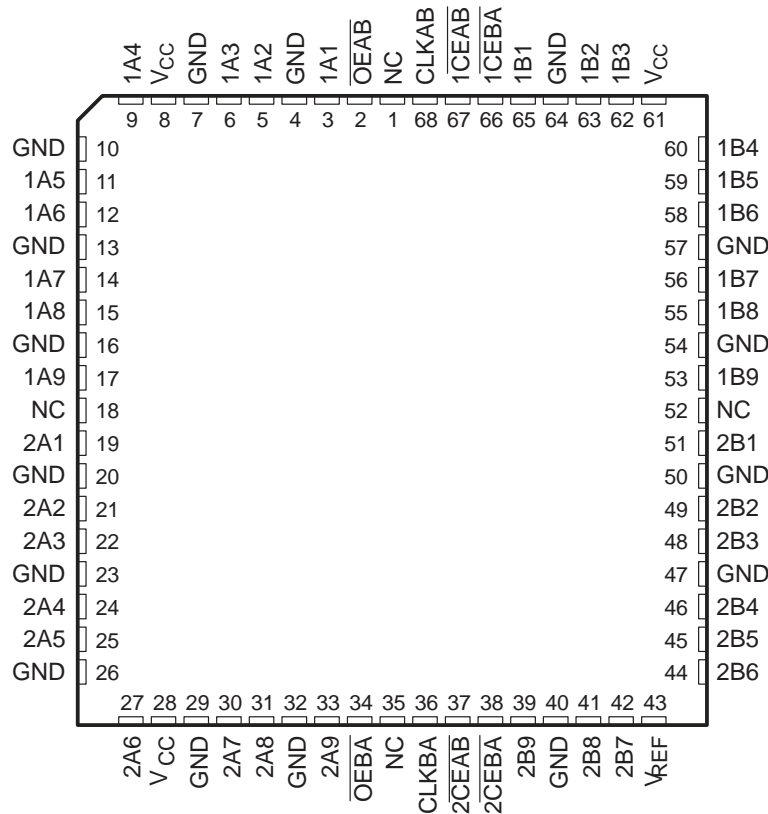
These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16622A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74GTL16622A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54GTL16622A . . . HV PACKAGE  
(TOP VIEW)



NC – No internal connection



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FUNCTION TABLE†

INPUTS				OUTPUT B	MODE
CEAB	OEAB	CLKAB	A		
X	H	X	X	Z	Isolation
H	L	X	X	B <sub>0</sub> ‡	Latched storage of A data
X	L	H or L	X	B <sub>0</sub> ‡	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

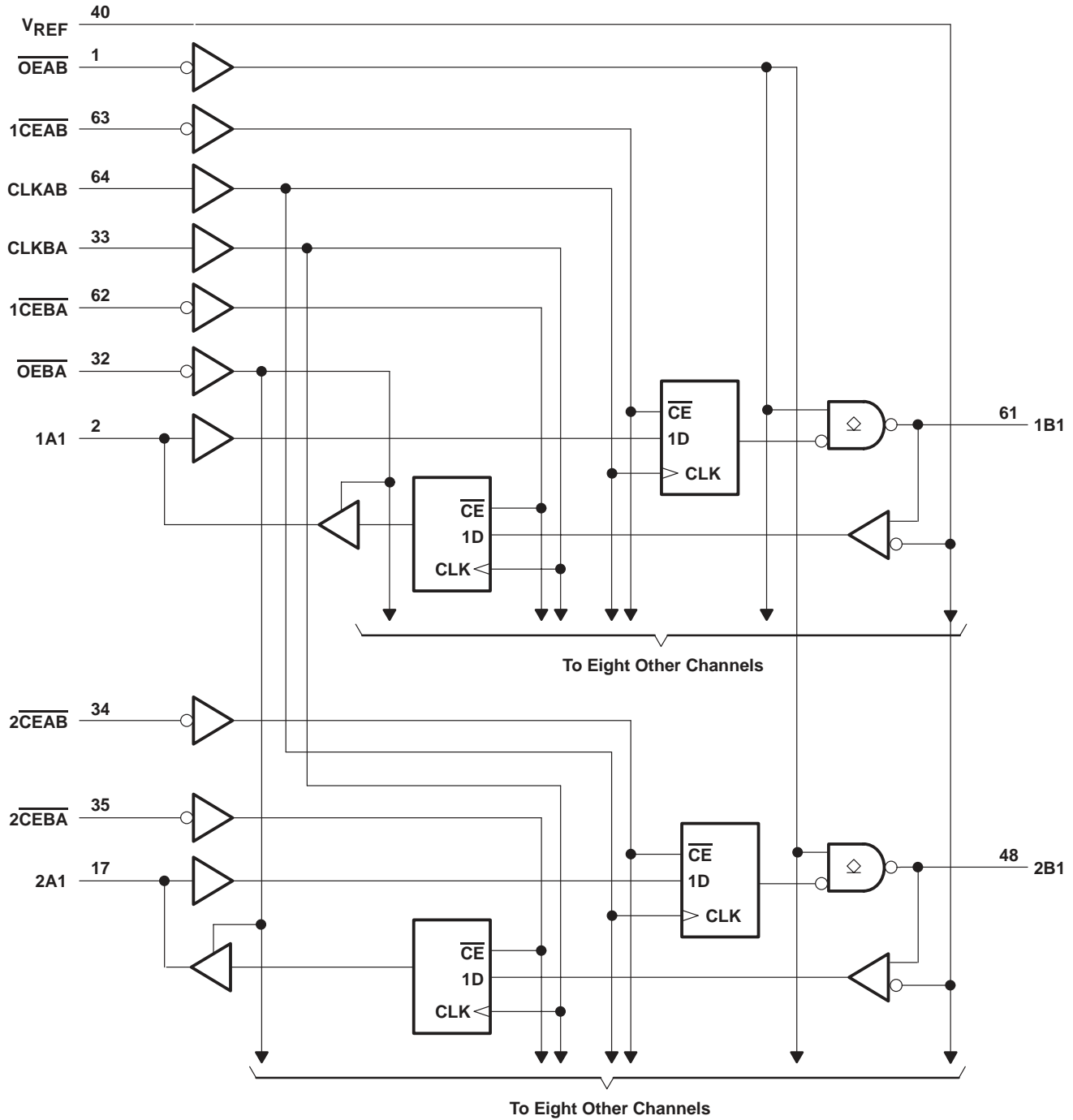
† A-to-B data flow is shown. B-to-A data flow is similar, but uses OEBA, CLKBA, and CEBA.

‡ Output level before the indicated steady-state input conditions are established

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## logic diagram (positive logic)



Pin numbers shown are for the DGG package.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1): A-port and control inputs .....	–0.5 V to 6.5 V
B port and $V_{REF}$ .....	–0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, $V_O$ (see Note 1): A port .....	–0.5 V to 6.5 V
B port .....	–0.5 V to 4.6 V
Current into any output in the low state, $I_O$ : A port .....	48 mA
B port .....	100 mA
Current into any A-port output in the high state, $I_O$ (see Note 2) .....	48 mA
Continuous current through each $V_{CC}$ or GND .....	±100 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	55°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Notes 4 through 6)

		SN54GTL16622A			SN74GTL16622A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
$V_{CC}$	Supply voltage	3.15	3.3	3.45	3.15	3.3	3.45	V	
$V_{TT}$	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	V
$V_{REF}$	Supply voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	V
$V_I$	Input voltage	B port	$V_{TT}$			$V_{TT}$			V
		Except B port	5.5			5.5			V
$V_{IH}$	High-level input voltage	B port	$V_{REF}+50$ mV			$V_{REF}+50$ mV			V
		Except B port	2			2			V
$V_{IL}$	Low-level input voltage	B port	$V_{REF}-50$ mV			$V_{REF}-50$ mV			V
		Except B port	0.8			0.8			V
$I_{IK}$	Input clamp current	–18			–18			mA	
$I_{OH}$	High-level output current	A port			–24			mA	
$I_{OL}$	Low-level output current	A port			24			mA	
		B port			50				
$T_A$	Operating free-air temperature	–55	125		–40	85		°C	

- NOTES: 4. All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.  
 5. Normal connection sequence is GND first and  $V_{CC} = 3.3$  V, I/O, control inputs,  $V_{TT}$  and  $V_{REF}$  (any order) last.  
 6.  $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute  $I_{OL}$  ratings. Similarly,  $V_{REF}$  can be adjusted to optimize noise margins, but normally is  $2/3 V_{TT}$ .

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electrical characteristics over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54GTL16622A			SN74GTL16622A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 3.15\text{ V}$ , $I_I = -18\text{ mA}$	-1.2			-1.2			V
$V_{OH}$	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$	V
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -12\text{ mA}$	2.4		2.4		
$V_{OL}$	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 12\text{ mA}$	0.4		0.4		
			$I_{OL} = 24\text{ mA}$	0.5		0.5		
	B port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 10\text{ mA}$	0.2		0.2		
			$I_{OL} = 40\text{ mA}$	0.4		0.4		
$I_I$	B port	$V_{CC} = 3.45\text{ V}$	$V_I = V_{TT}$ or GND		$\pm 5$		$\pm 5$	$\mu\text{A}$
	A-port and control inputs	$V_{CC} = 3.45\text{ V}$	$V_I = V_{CC}$ or GND		$\pm 5$			
			$V_I = 5.5\text{ V}$ or GND		$\pm 20$			
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to $5.5\text{ V}$		100		100	$\mu\text{A}$	
$I_I(\text{hold})$	A port	$V_{CC} = 3.15\text{ V}$	$V_I = 0.8\text{ V}$	75		75		$\mu\text{A}$
			$V_I = 2\text{ V}$	-75		-75		
		$V_{CC} = 3.45\text{ V}^\ddagger$ ,	$V_I = 0.8\text{ V to } 2\text{ V}$		$\pm 500$		$\pm 500$	
$I_{OZ}^\S$	A port	$V_{CC} = 3.45\text{ V}$ ,	$V_O = V_{CC}$ or GND		$\pm 10$		$\pm 10$	$\mu\text{A}$
$I_{OZH}$	B port	$V_{CC} = 3.45\text{ V}$ ,	$V_O = 1.5\text{ V}$		10		10	$\mu\text{A}$
$I_{CC}$	A or B port	$V_{CC} = 3.45\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		60		60	mA
			Outputs low		60		60	
			Outputs disabled		60		60	
$\Delta I_{CC}^\parallel$		$V_{CC} = 3.45\text{ V}$ , A-port or control inputs at $V_{CC}$ or GND, One input at $V_{CC} - 0.6\text{ V}$		500		500	$\mu\text{A}$	
$C_i$	Control inputs	$V_I = 3.15\text{ V}$ or 0		2.5 3		2.5 3	pF	
$C_{io}$	A port	$V_O = 3.15\text{ V}$ or 0		6 8.5		6 8	pF	
	B port			7 9.5		6.5 8.5		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)**

		SN54GTL16622A		SN74GTL16622A		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	200		200		MHz
$t_w$	Pulse duration, CLK high or low	2.5		2.5		ns
$t_{\text{su}}$	Setup time	Data before CLK $\uparrow$	2.5	2.1		ns
		$\overline{\text{CE}}$ before CLK $\uparrow$	3.5	3.3		
$t_h$	Hold time	Data after CLK $\uparrow$	0.3	0.3		ns
		$\overline{\text{CE}}$ after CLK $\uparrow$	0.3	0		

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16622A			SN74GTL16622A			UNIT
			MIN	TYP $\dagger$	MAX	MIN	TYP $\dagger$	MAX	
$f_{\text{max}}$			200			200			MHz
$t_{\text{PLH}}$	CLKAB	B	2.4		5.7	2.5		5.5	ns
$t_{\text{PHL}}$			2.1		5.7	2.2		5.5	
$t_{\text{dis}}$	OEAB	B	1.6		5	1.7		4.8	ns
$t_{\text{en}}$			2.1		5.5	2.2		5.2	
Slew rate	Both transitions (B port)		0.5			0.5			V/ns
$t_r$	Transition time, B outputs (0.6 V to 1 V)		0.5		2.3	0.6		2.2	ns
$t_f$	Transition time, B outputs (1 V to 0.6 V)		0.3		1.7	0.4		1.5	ns
$t_{\text{PLH}}$	CLKBA	A	1.9		5.5	2.1		5.3	ns
$t_{\text{PHL}}$			1.8		5.3	2.1		5	
$t_{\text{en}}$	$\overline{\text{OEBA}}$	A	1.6		5.3	1.7		5	ns
$t_{\text{dis}}$			2		5.8	2.3		5.5	

$\dagger$  All typical values are at  $V_{\text{CC}} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

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timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

		SN54GTL16622A		SN74GTL16622A		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	200		200		MHz
$t_w$	Pulse duration, CLK high or low	2.5		2.5		ns
$t_{\text{su}}$	Setup time	Data before CLK $\uparrow$	2.5	2.4		ns
		$\overline{\text{CE}}$ before CLK $\uparrow$	3.4	3.2		
$t_h$	Hold time	Data after CLK $\uparrow$	0.3	0.2		ns
		$\overline{\text{CE}}$ after CLK $\uparrow$	0.1	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16622A			SN74GTL16622A			UNIT
			MIN	TYP $\dagger$	MAX	MIN	TYP $\dagger$	MAX	
$f_{\text{max}}$			200			200			MHz
$t_{\text{PLH}}$	CLKAB	B	2.5		5.8	2.6	4	5.6	ns
$t_{\text{PHL}}$			2.2		6.1	2.3	4	5.7	
$t_{\text{PLH}}$	OEAB	B	2.3		5.5	2.4	3.8	5.2	ns
$t_{\text{PHL}}$			1.7		5.3	1.8	3.4	5	
Slew rate	Both transitions (B port)		0.5			0.5			V/ns
$t_r$	Transition time, B outputs (0.6 V to 1.3 V)		0.9		2.8	1	1.6	2.7	ns
$t_f$	Transition time, B outputs (1.3 V to 0.6 V)		0.4		3.7	0.5	1.1	3.2	ns
$t_{\text{PLH}}$	CLKBA	A	1.9		5.5	2	3.8	5.3	ns
$t_{\text{PHL}}$			1.8		5.3	1.9	3.6	5	
$t_{\text{en}}$	$\overline{\text{OEBA}}$	A	1.8		5.3	1.9	3.6	5	ns
$t_{\text{dis}}$			2		5.8	2.1	4	5.5	

$\dagger$  All typical values are at  $V_{\text{CC}} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

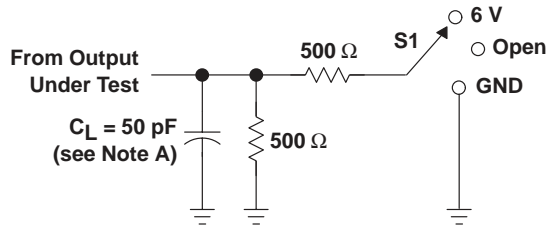
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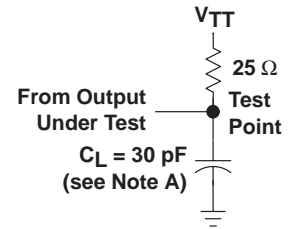


PARAMETER MEASUREMENT INFORMATION

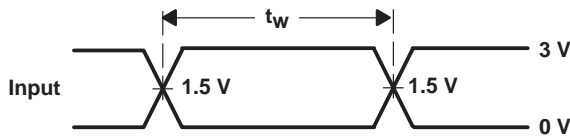


LOAD CIRCUIT FOR A OUTPUTS

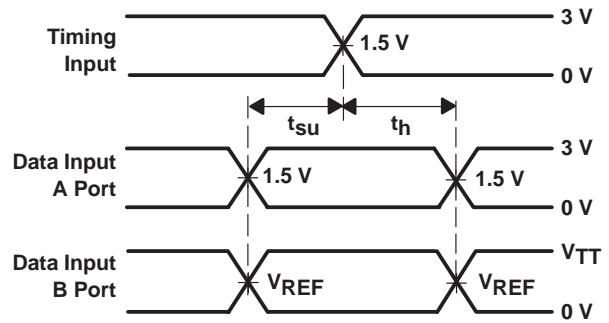
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



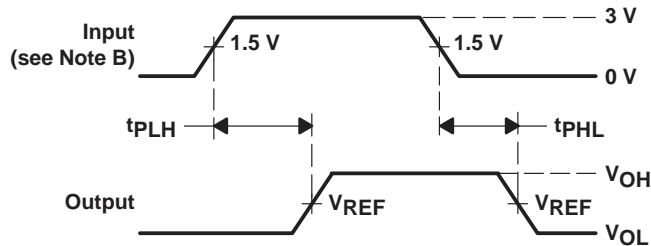
LOAD CIRCUIT FOR B OUTPUTS



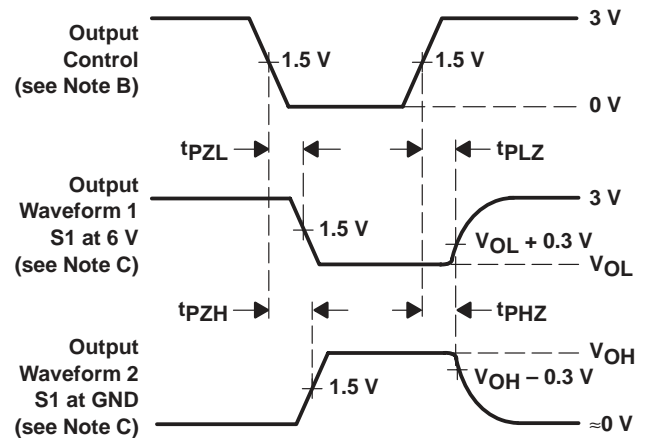
VOLTAGE WAVEFORMS  
PULSE DURATION



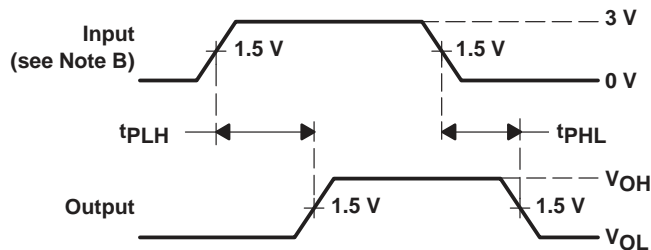
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(CLKAB to B port)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
(OEBA to A port)



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(CLKBA to A port)

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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