Evaluation Board for Dual Ultrafast Voltage Comparator

EVAL-ADCMP565

FEATURES

Standard SMA input/output connections
High speed testing capability
Dual ADCMP565 voltage comparator included
Banana jack power supplies
DC/AC inputs

APPLICATIONS

General evaluation of the ADCMP565
Dual voltage comparator
Assist future PCB layouts using the ADCMP565

PRODUCT DESCRIPTION

The ADCMP565 evaluation board provides users with a straightforward means of examining the performance capabilities of the ADCMP565. It also enables general functionality of the ADCMP565. Currently, the evaluation board accommodates high performance testing; however, it has not yet been fully optimized to enable the highest bandwidth operations produced by the ADCMP565.

Banana jacks are used to supply all necessary power to the evaluation board. The ADCMP565 requires supplies of −5.2 V and +5.0 V. The ADCMP565 evaluation board uses a −4.0 V supply that provides appropriate ECL termination for the outputs. Two dc threshold inputs are also user-supplied. If a dc threshold is desired, the two are routed on the board to threshold outputs where they must be jumpered to either the inverting or noninverting input for each comparator.

All ac inputs, including the latch enables, should be directly connected using a 50 Ω source and 50 Ω cable with SMA connectors. Likewise, the Q outputs should be monitored using an instrument that provides a 50 Ω termination.

Note that this board is designed to enable full testing capability for both sides of the dual comparator. If testing only one side, no attention needs to be paid to the untested side. Latches, inputs, and outputs can be left unconnected on the unused side.

ADCMP565 DEVICE DESCRIPTION

The ADCMP565 is an ultrafast voltage comparator fabricated on Analog Devices' proprietary XFCB process. The device features 300 ps propagation delay with less than 50 ps overdrive dispersion. Overdrive dispersion, a particularly important characteristic of high speed comparators, is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from −2.0 V to +3.0 V. Outputs are complementary digital signals fully compatible with ECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to −2 V. A latch input is included, which permits tracking, track-and-hold, or sample-and-hold modes of operation.

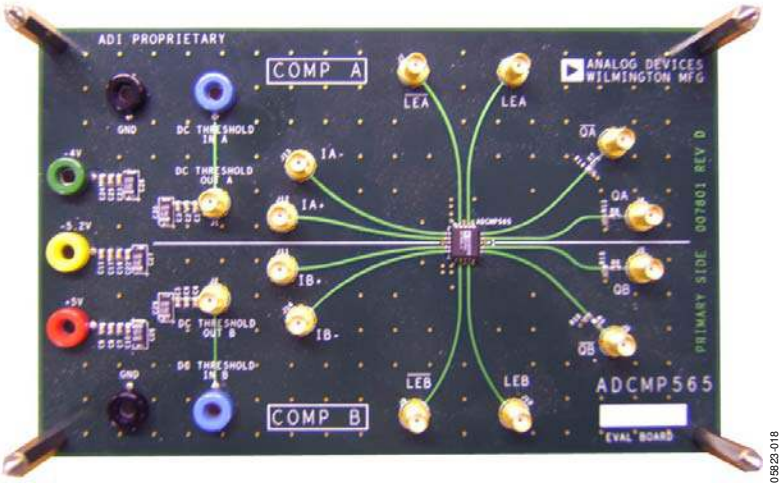

Figure 1. Evaluation Board

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

1/06—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Power is supplied via color-coded banana jack plugs and all are decoupled on the board.

- Red is +5 V.
- Yellow is –5.2 V.
- Green is –4 V. The –4 V is not required by the part. Rather, this voltage is used to provide proper on-board ECL terminations for the part.
- Two black jacks are for ground.
- Two blue jacks are labeled DC THRESHOLD IN. For proper use of the blue jacks, see the Inputs section.

Table 1. Connector Functions

Name	Function
J1	Threshold_A Out
J2	Threshold_B Out
J3	QAbar
J4	QA
J5	QB
J6	QBbar
J7	LEAbar
J8	LEA
J9	LEBbar
J10	LEB
J11	IB+
J12	IA+
J13	IA–
J14	IB–
TP1 (Black)	GND
TP2 (Red)	VCC
TP3 (Yellow)	VEE
TP4 (Green)	–4V
TP5 (Blue)	Threshold_A In
TP6 (Blue)	Threshold_B In
TP9 (Black)	GND

INPUTS

There are four separate input pins on the ADCMP565. Likewise, there are four input SMA connectors distinctively labeled on this evaluation board. AC signals should be directly applied to one of these four input SMAs. If a dc threshold is desired, a small network is supplied that allows one dc source to be connected to any input pin and then changed as desired. The actual threshold is supplied via the blue banana jacks on both COMP A and COMP B. A connection is then from the banana jack (DC THRESHOLD IN) to an SMA connector (DC THRESHOLD OUT). From this point, the threshold can be jumpered using an SMA cable to any input pin desired.

Note that every input trace continues by the pin and through a 50 Ω resistor to ground. This provides the option of using high speed AD signals for every input being used. If using a dc threshold on one of the input pins is desired, it is advisable to remove the 50 Ω resistor for that pin depending on how much current the supply can deliver. R1, R2, R3, and R4 correspond respectively to inputs IB, IA, $\overline{IB}$, and $\overline{IA}$.

LATCHES

Each half of the dual comparator has a latch enable and an inverted latch enable pin. These pins should be directly driven by connecting a source to each SMA connector. It is important to remember that the latches cannot be left unconnected. Proper levels must be provided for the ADCMP565 to function correctly. For correct logic levels in both compare and latch modes, please refer to the pin description in the ADCMP565 data sheet.

OUTPUTS

A resistor network on each output trace provides a very accurate ECL 50 Ω path to the output SMA connectors. By using any SMA-compatible cable, the outputs can be monitored on the 50 Ω equipment of the user's choice.

EVALUATION BOARD LAYOUT

The EVAL-ADCMP565 is designed to ensure that a high fidelity 50 Ω environment is maintained from input to output. Trace widths are carefully matched with the PCB material to produce a 50 Ω transmission line. Trace lengths are matched exactly for all inputs and latches. All outputs are also matched in length to each other. For specific part/pin information on the ADCMP565, please refer to the data sheet.

TYPICAL CONNECTION DIAGRAM

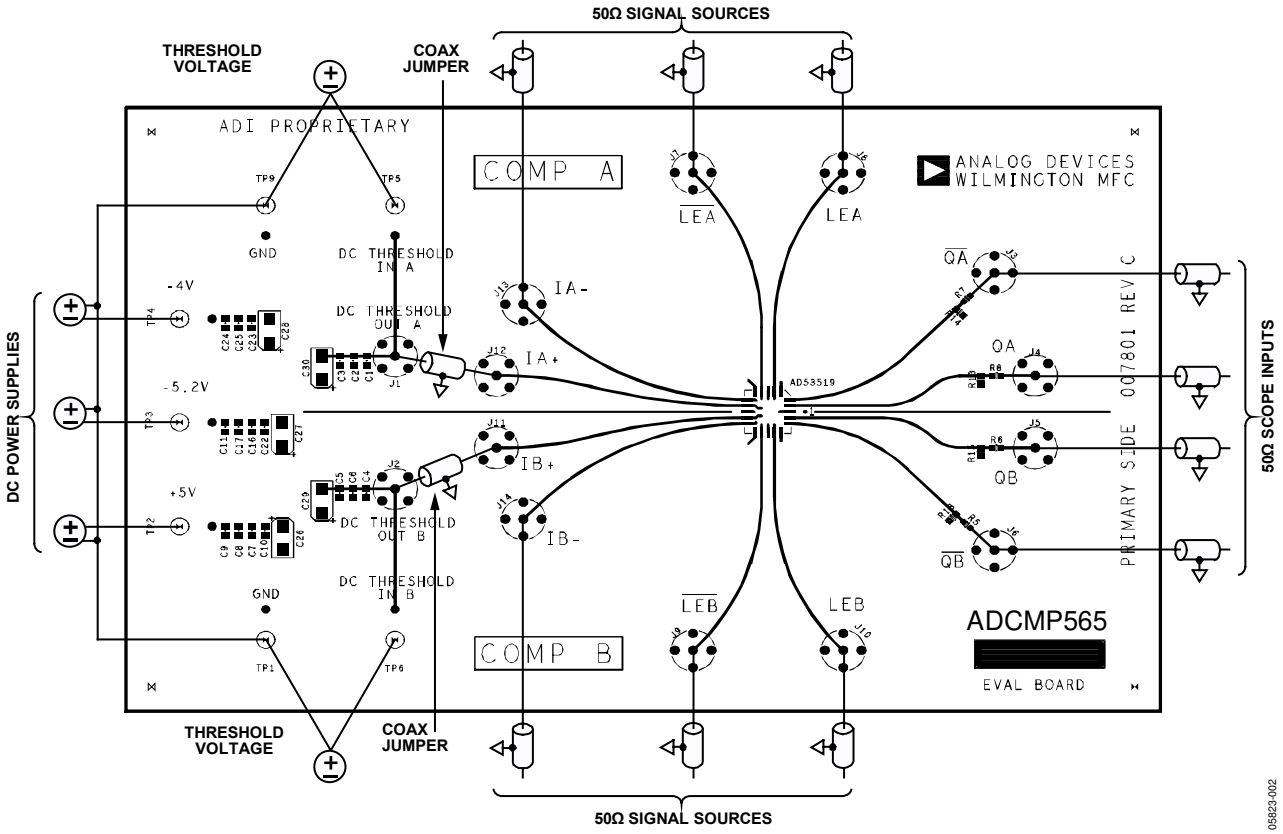

Figure 2.

SCHEMATIC

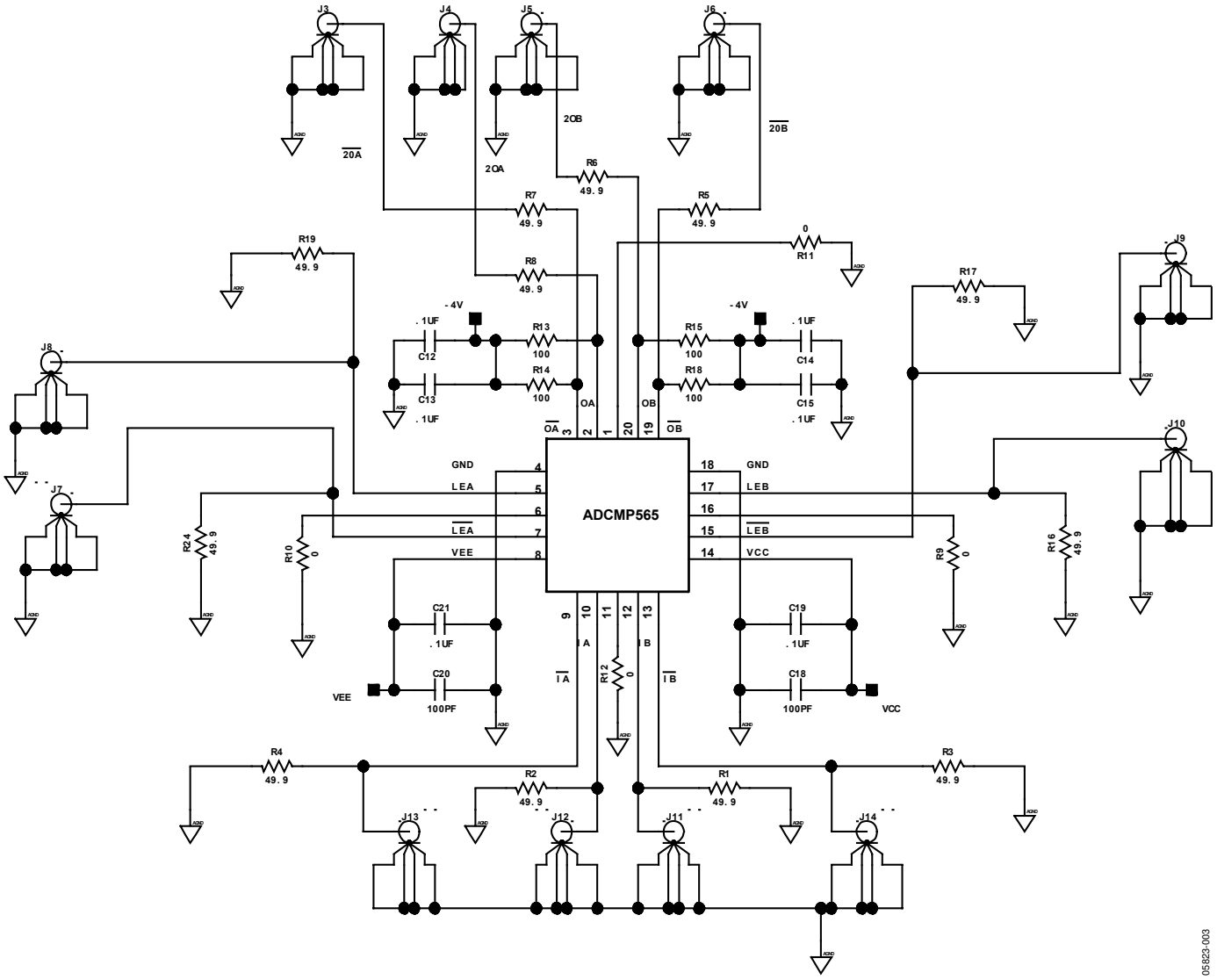

Figure 3.EVAL-ADCMP565 Schematic, Page 1 of 2

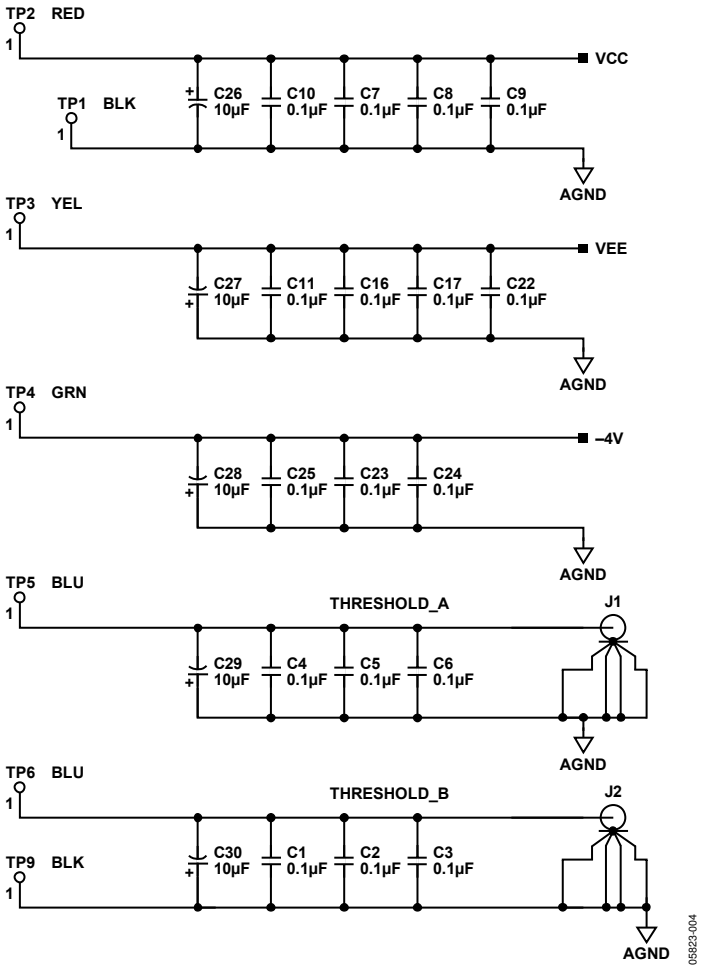

Figure 4. EVAL-ADCMP565 Schematic, Page 2 of 2

LAYERS

The ADCMP565 evaluation board consists of eight layers (including both signal and power planes). The following pages represent these layers.

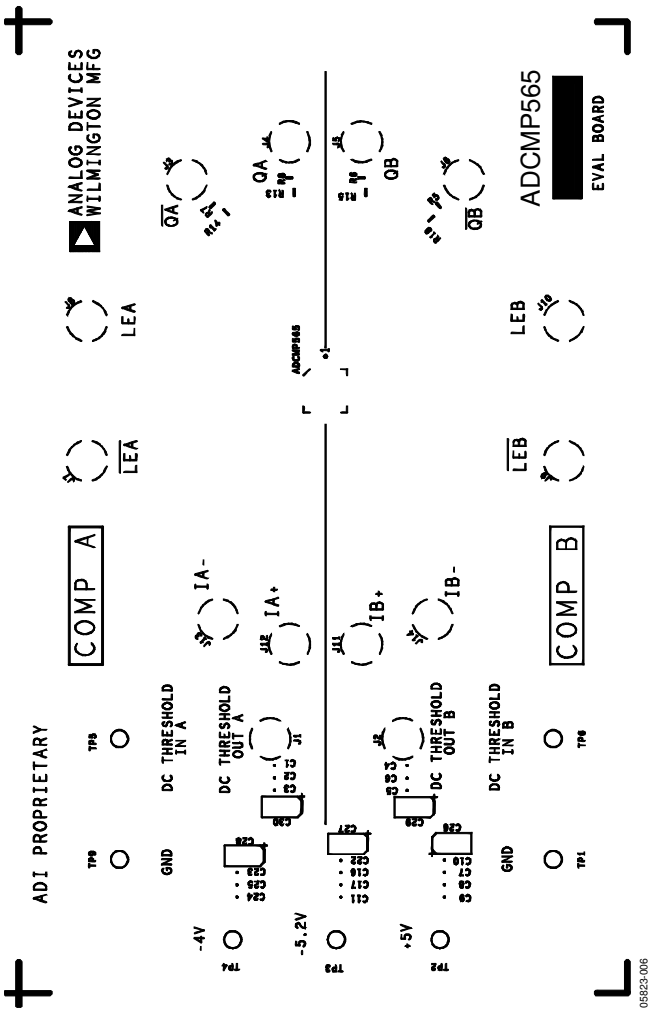

Figure 5. Primary Silkscreen

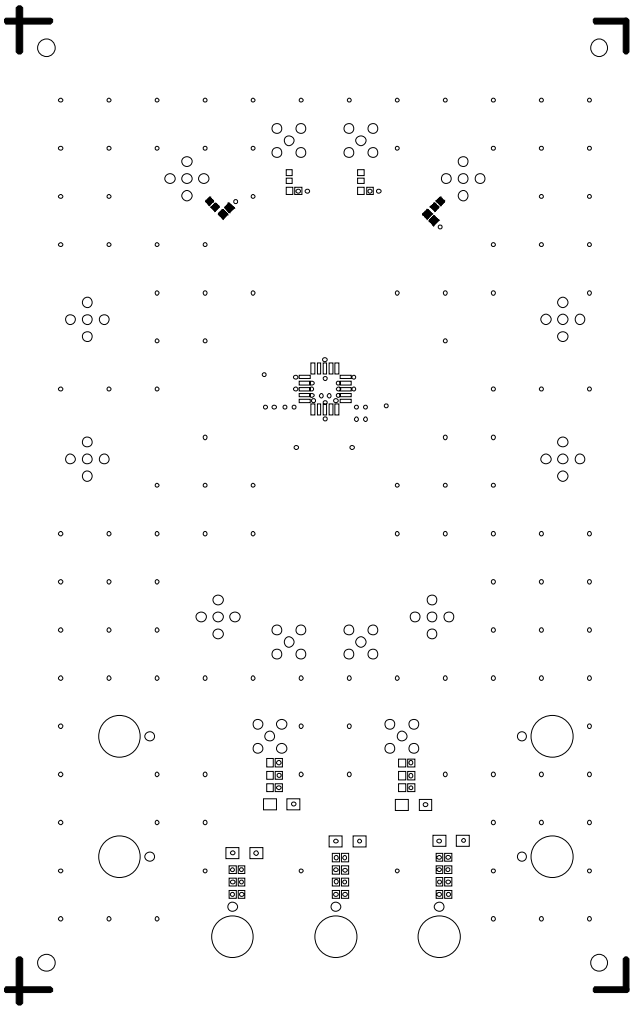

Figure 6. Primary Solder Mask

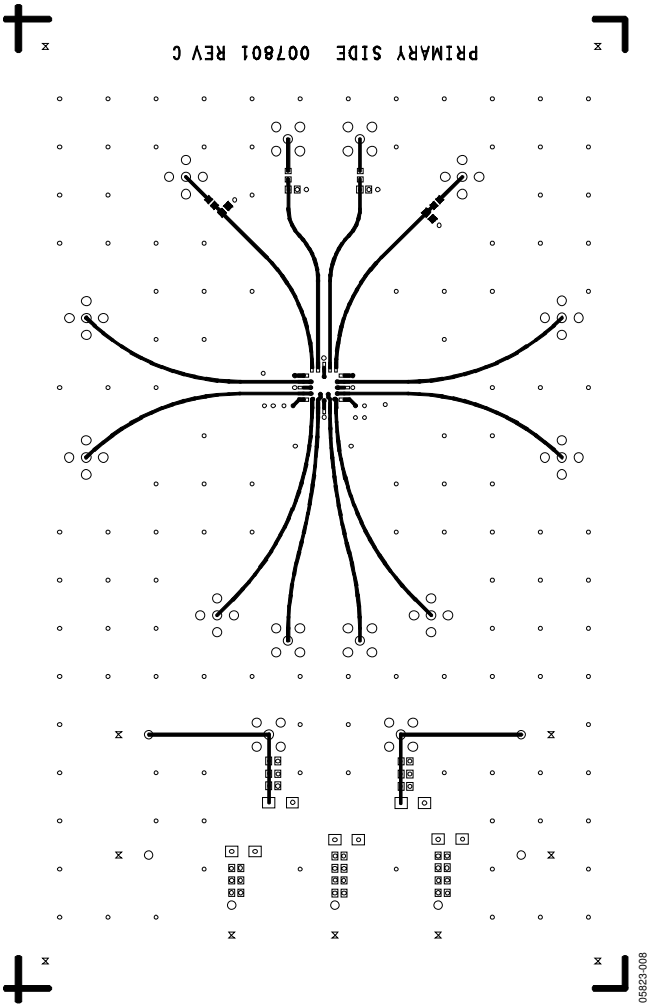

Figure 7. Layer 1 (Signal)

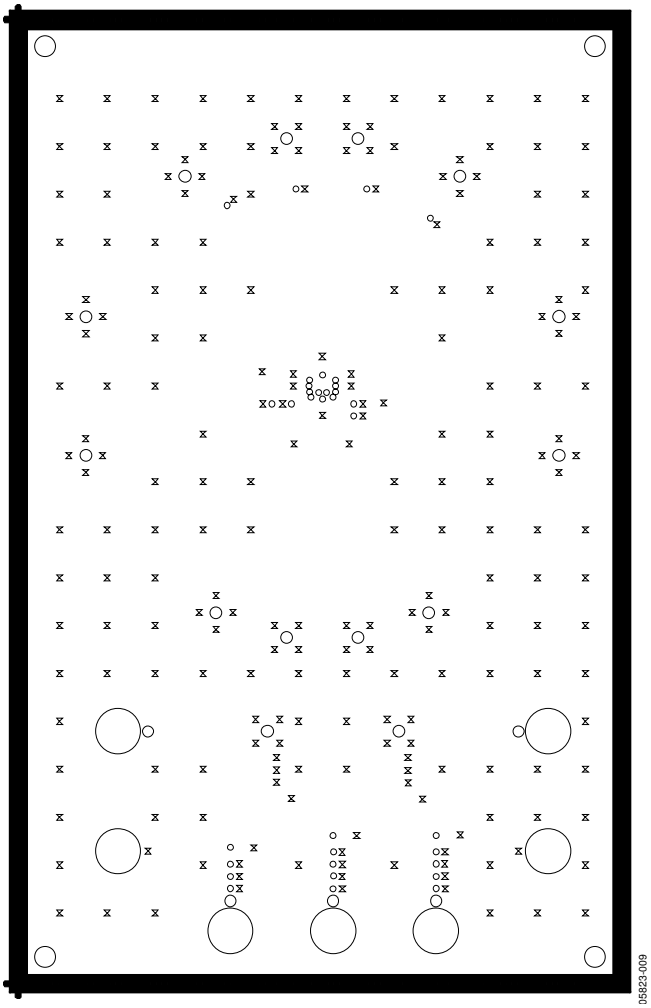

Figure 8. Layer 2 (GND 1)

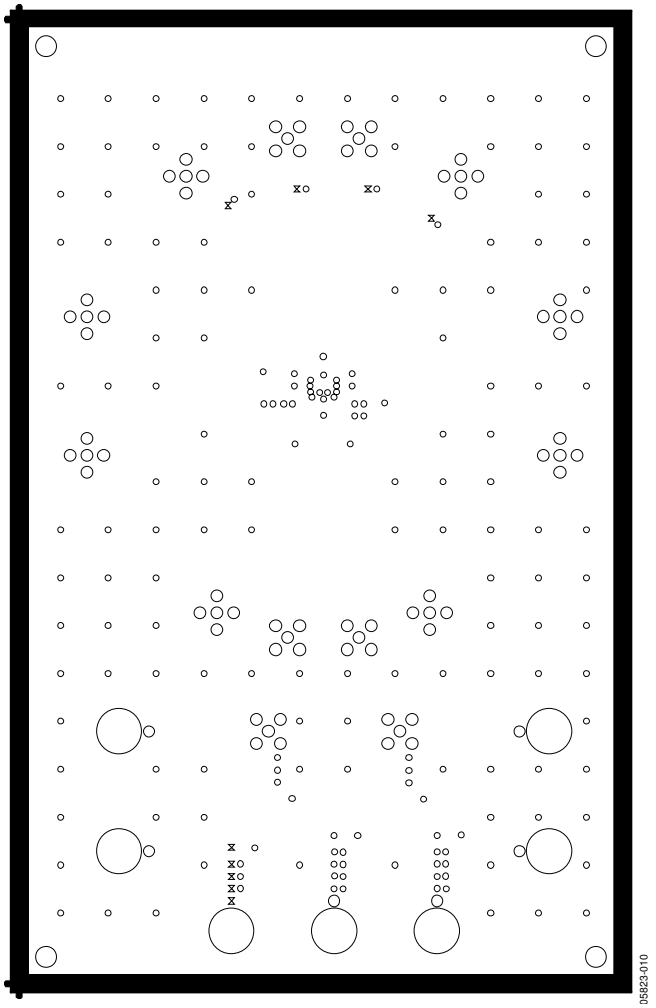

Figure 9. Layer 3 (−4 V)

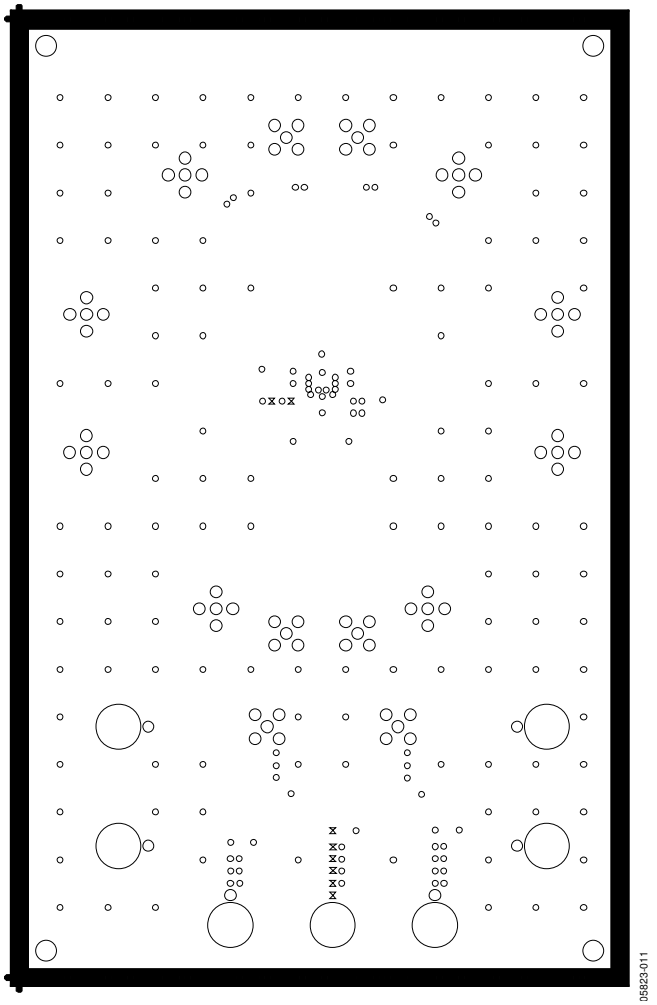

Figure 10. Layer 4 (VEE)

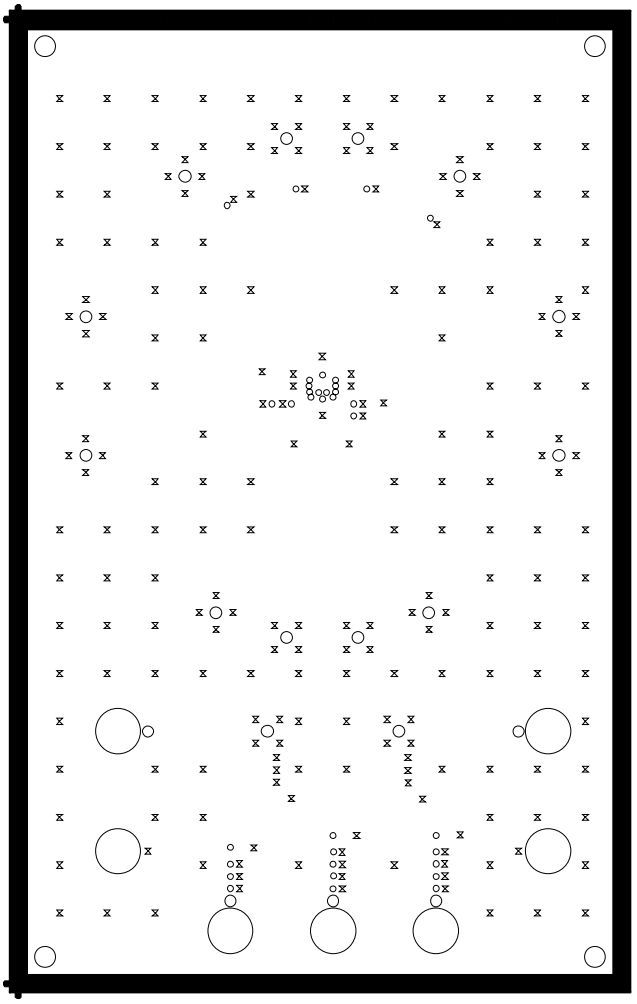

Figure 11. Layer 5 (GND2)

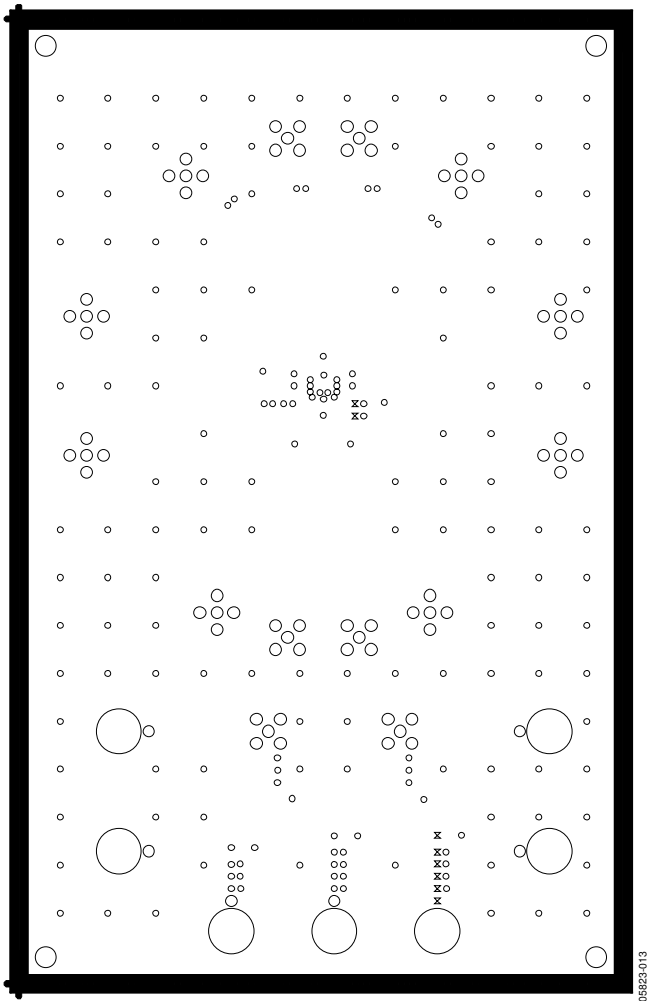

Figure 12. Layer 6 (VCC)

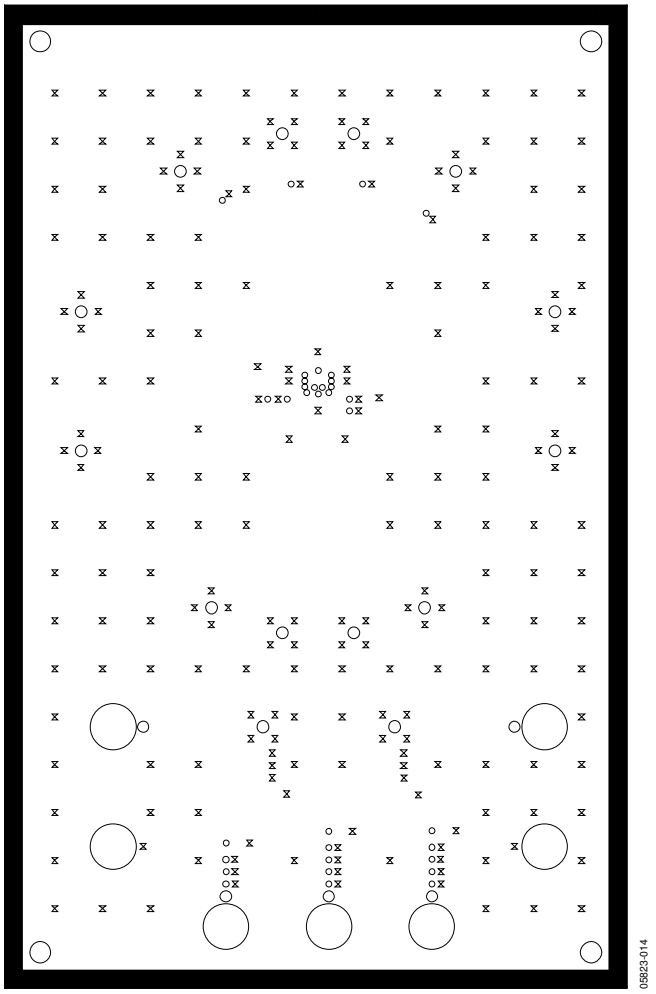

Figure 13. Layer 7 (GND 3)

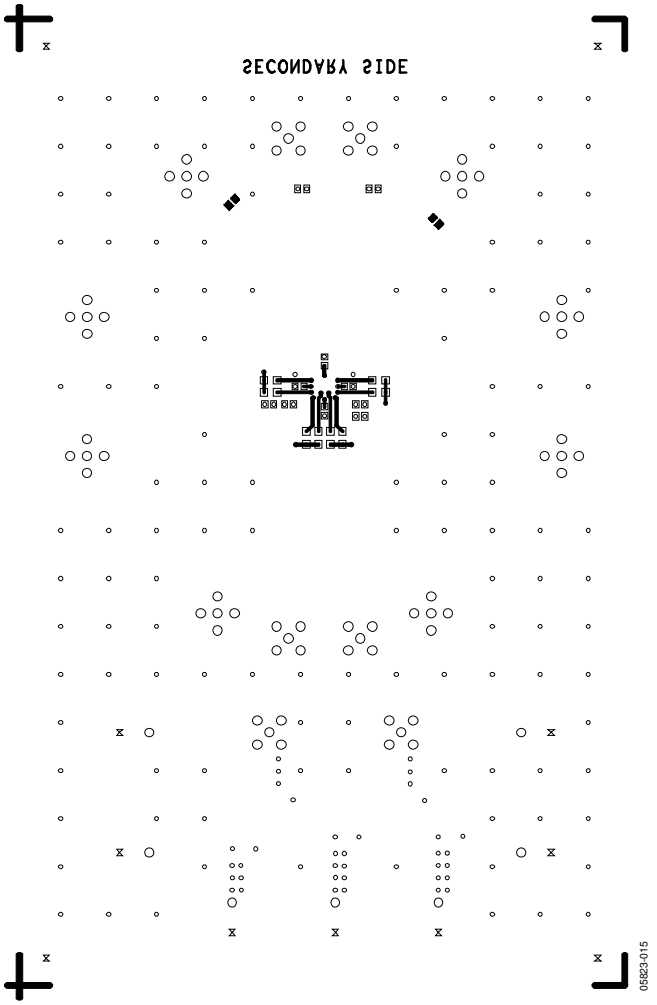

Figure 14. Layer 8 (Signal)

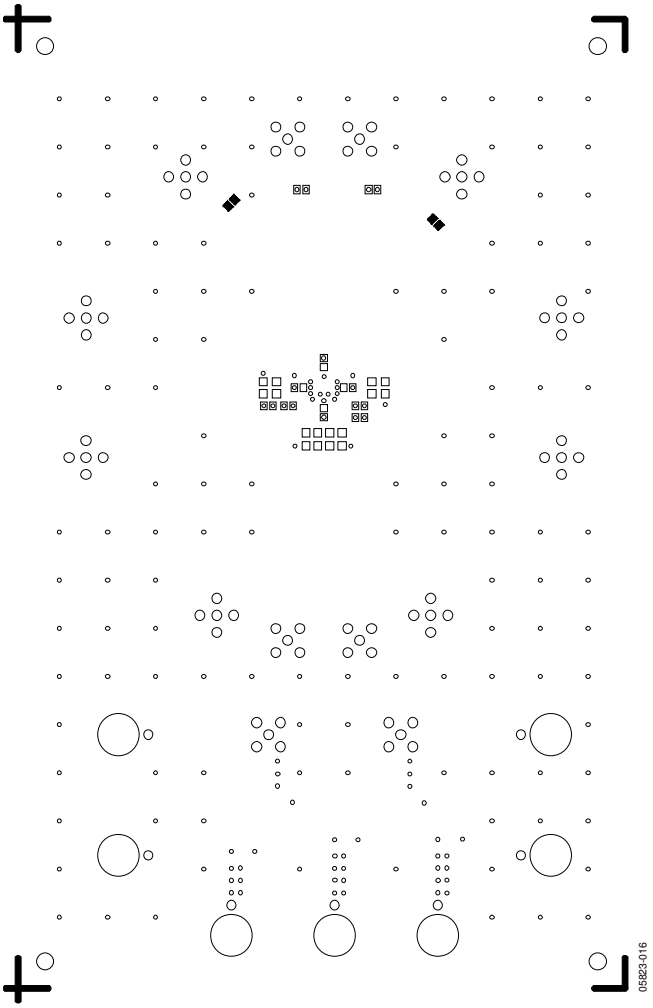

Figure 15. Secondary Solder Mask

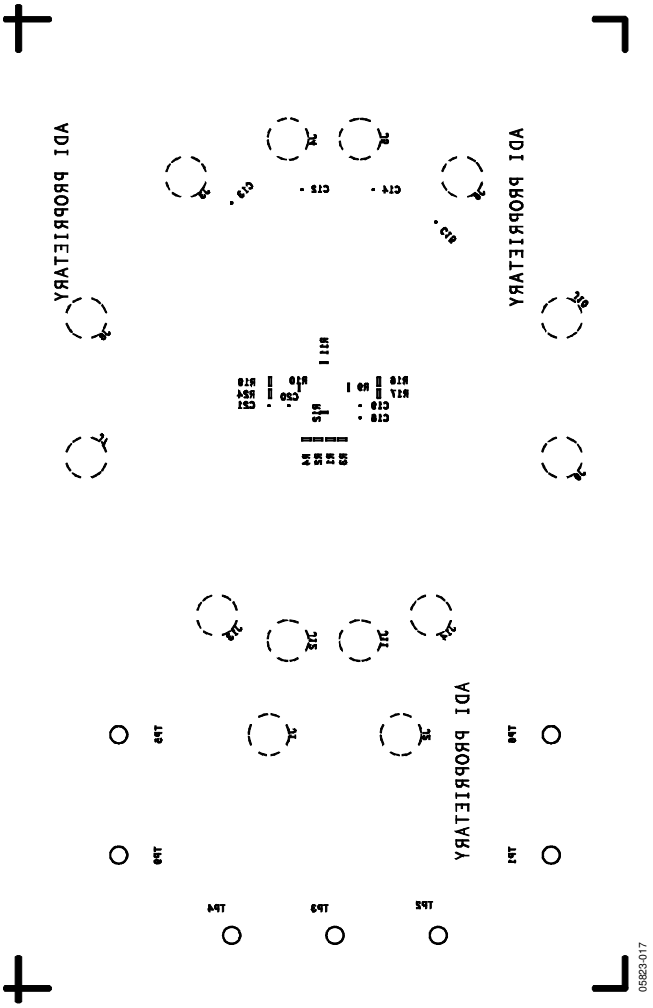

Figure 16. Secondary Silkscreen

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
EVAL-ADCMP565BP	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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