CY23FP12

200 MHz Field Programmable Zero Delay Buffer

Features

- Fully field-programmable
  - Input and output dividers
  - Inverting/non-inverting outputs
  - Phase-locked loop (PLL) or fanout buffer configuration
- 10 MHz to 200 MHz operating range
- Split 2.5 V or 3.3 V outputs
- Two LVCMOS reference inputs
- Twelve low skew outputs
  - 35 ps typical output-to-output skew (same frequency)
- 110 ps typical cycle-cycle jitter (same frequency)
- Three-stateable outputs
- Less than 50 µA shutdown current
- Spread aware
- 28-pin SSOP
- 3.3 V operation
- Industrial temperature available

Functional Description

The CY23FP12 is a high performance fully field-programmable 200 MHz zero delay buffer designed for high speed clock distribution. The integrated PLL is designed for low jitter and optimized for noise rejection. These parameters are critical for reference clock distribution in systems using high performance ASICs and microprocessors.

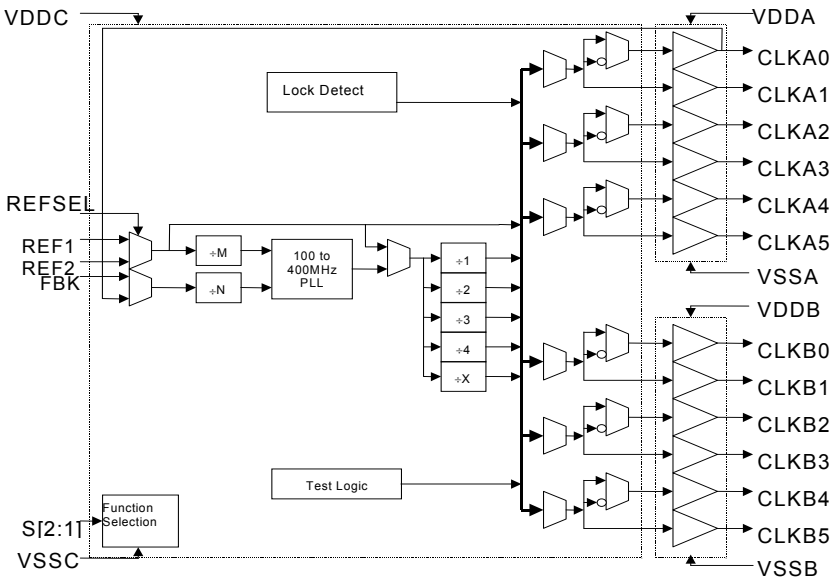
The CY23FP12 is fully programmable through volume or prototype programmers, enabling the user to define an application-specific Zero Delay Buffer with customized input and output dividers, feedback topology (internal/external), output inversions, and output drive strengths. For additional flexibility, the user can mix and match multiple functions listed in Table 2, and assign a particular function set to any one of the four possible S1-S2 control bit combinations. This feature enables the implementation of four distinct personalities, selectable with S1-S2 bits, on a single programmed silicon. The CY23FP12 also features a proprietary auto power down circuit that shuts down the device in case of a REF failure, resulting in less than 50 µA of current draw.

The CY23FP12 provides 12 outputs grouped in two banks with separate power supply pins which can be connected independently to either a 2.5 V or a 3.3 V rail.

Selectable reference input is a fault tolerance feature which enables glitch-free switch over to a secondary clock source when REFSEL is asserted/de-asserted.

For a complete list of related documentation, click here.

Logic Block Diagram

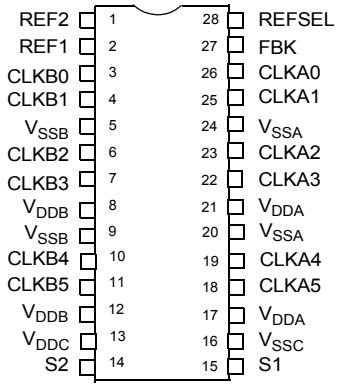


Contents

Pin Configuration

Figure 1. 28-pin SSOP pinout

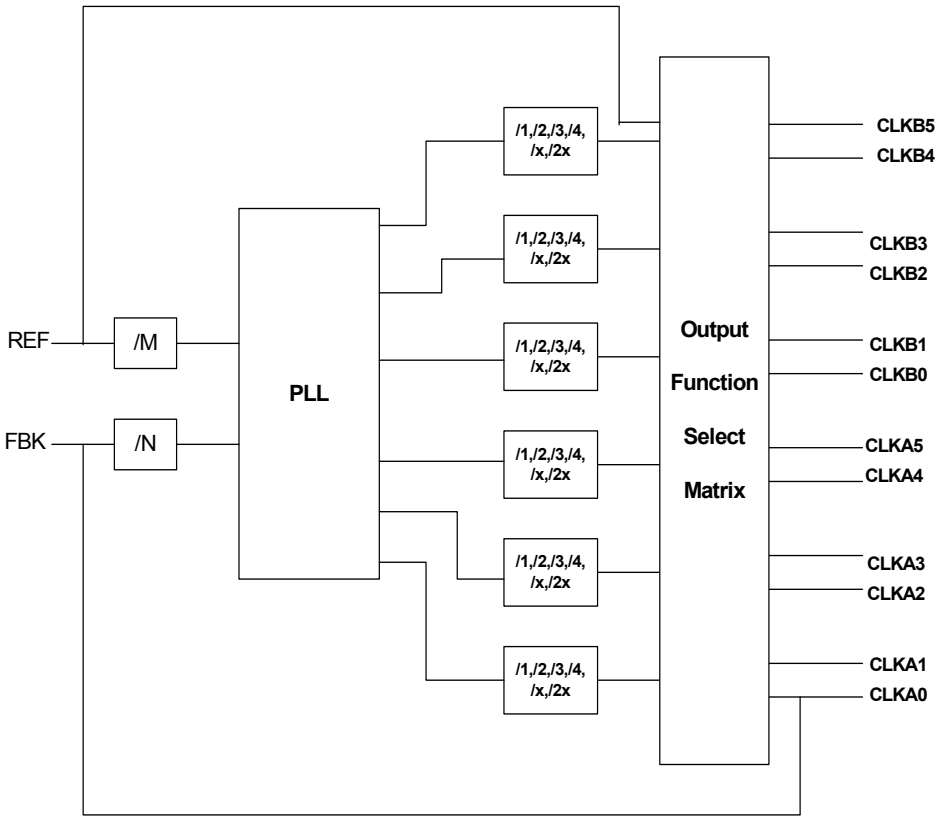
Top View



Pin Description

Pin No.	Name	I/O	Type	Description
1	REF2	I	LVTTL/LVCMOS	Input reference frequency, 5 V tolerant input.
2	REF1	I	LVTTL/LVCMOS	Input reference frequency, 5 V tolerant input.
3	CLKB0	O	LVTTL	Clock output, Bank B.
4	CLKB1	O	LVTTL	Clock output, Bank B.
5	V_{SSB}	PWR	POWER	Ground for Bank B.
6	CLKB2	O	LVTTL	Clock output, Bank B.
7	CLKB3	O	LVTTL	Clock output, Bank B.
8	V_{DDB}	PWR	POWER	2.5 V or 3.3 V supply, Bank B.
9	V_{SSB}	PWR	POWER	Ground for Bank B.
10	CLKB4	O	LVTTL	Clock output, Bank B.
11	CLKB5	O	LVTTL	Clock output, Bank B.
12	V_{DDB}	PWR	POWER	2.5 V or 3.3 V supply, Bank B.
13	V_{DDC}	PWR	POWER	3.3 V core supply.
14	S2	I	LVTTL	Select input.
15	S1	I	LVTTL	Select input.
16	V_{SSC}	PWR	POWER	Ground for core.
17	V_{DDA}	PWR	POWER	2.5 V or 3.3 V supply, Bank A.
18	CLKA5	O	LVTTL	Clock output, Bank A.
19	CLKA4	O	LVTTL	Clock output, Bank A.
20	V_{SSA}	PWR	POWER	Ground for Bank A.
21	V_{DDA}	PWR	POWER	2.5 V or 3.3 V supply Bank A.
22	CLKA3	O	LVTTL	Clock output, Bank A.
23	CLKA2	O	LVTTL	Clock output, Bank A.
24	V_{SSA}	PWR	POWER	Ground for Bank A.
25	CLKA1	O	LVTTL	Clock output, Bank A.
26	CLKA0	O	LVTTL	CLock output, Bank A.
27	FBK	I	LVTTL	PLL feedback input.
28	REFSEL	I	LVTTL	Reference select input. When REFSEL = 0, REF1 is selected. When REFSEL = 1, REF2 is selected.

Basic PLL Block Diagram



Programmable Functions

The following table lists independent functions that can be programmed with a volume or prototype programmer on the “default” silicon.

Table 1. Programmable Functions

Configuration	Description	Default
DC Drive Bank A	Programs the drive strength of Bank A outputs. The user can select one out of two possible drive strength settings that produce output DC currents in the range of ±16 mA to ±20 mA.	±16 mA
DC Drive Bank B	Programs the drive strength of Bank B outputs. The user can select one out of two possible drive strength settings that produce output DC currents in the range of ±16 mA to ±20 mA.	±16 mA
Output Enable for Bank B clocks	Enables/Disables CLKB[5:0] outputs. Each of the six outputs can be disabled *individually* if not used, to minimize electromagnetic interference (EMI) and switching noise.	Enable
Output Enable for Bank A clocks	Enables/Disables CLKA[5:0] outputs. Each of the six outputs can be disabled *individually* if not used, to minimize EMI and switching noise.	Enable
Inv CLKA0	Generates an inverted clock on the CLKA0 output. When this option is programmed, CLKA0 and CLKA1 will become complimentary pairs.	Non-invert
Inv CLKA2	Generates an inverted clock on the CLKA2 output. When this option is programmed, CLKA2 and CLKA3 will become complimentary pairs.	Non-invert
Inv CLKA4	Generates an inverted clock on the CLKA4 output. When this option is programmed, CLKA4 and CLKA5 will become complimentary pairs.	Non-invert
Inv CLKB0	Generates an inverted clock on the CLKB0 output. When this option is programmed, CLKB0 and CLKB1 will become complimentary pairs.	Non-invert
Inv CLKB2	Generates an inverted clock on the CLKB2 output. When this option is programmed, CLKB2 and CLKB3 will become complimentary pairs.	Non-invert
Inv CLKB4	Generates an inverted clock on the CLKB4 output. When this option is programmed, CLKB4 and CLKB5 will become complimentary pairs.	Non-invert
Pull-down Enable	Enables/Disables internal pulldowns on all outputs	Enable
Fbk Pull-down Enable	Enables/Disables internal pulldowns on the feedback path (applicable to both internal and external feedback topologies)	Enable
Fbk Sel	Selects between the internal and the external feedback topologies	External

Table 2 lists independent functions that can be assigned to each of the four S1 and S2 combinations. When a particular S1 and S2 combination is selected, the device assumes the configuration (which is essentially a set of functions given in Table 2) that has been preassigned to that particular combination.

Table 2. Programmable Functions for S1/S2 Combinations

Function	Description	Default
Output Enable CLKB[5:4]	Enables/Disables CLKB[5:4] output pair	See Table 4 on page 8
Output Enable CLKB[3:2]	Enables/Disables CLKB[3:2] output pair	See Table 4 on page 8
Output Enable CLKB[1:0]	Enables/Disables CLKB[1:0] output pair	See Table 4 on page 8
Output Enable CLKA[5:4]	Enables/Disables CLKA[5:4] output pair	See Table 4 on page 8
Output Enable CLKA[3:2]	Enables/Disables CLKA[3:2] output pair	See Table 4 on page 8
Output Enable CLKA[1:0]	Enables/Disables CLKA[1:0] output pair	See Table 4 on page 8
Auto Power-down Enable	Enables/Disables the auto power down circuit, which monitors the reference clock rising edges and shuts down the device in case of a reference “failure.” This failure is triggered by a drift in reference frequency below a set limit. This auto power down circuit is disabled internally when one or more of the outputs are configured to be driven directly from the reference clock.	Enable
PLL Power-down	Shuts down the PLL when the device is configured as a non-PLL fanout buffer.	PLL Enabled
M[7:0]	Assigns an eight-bit value to reference divider –M. The divider can be any integer value from 1 to 256; however, the PLL input frequency cannot be lower than 10 MHz.	2
N[7:0]	Assigns an eight-bit value to feedback divider –N. The divider can be any integer value from 1 to 256; however, the PLL input frequency cannot be lower than 10 MHz.	2
X[6:0]	Assigns a seven-bit value to output divider –X. The divider can be any integer value from 5 to 130. Divide by 1,2,3, and 4 are preprogrammed on the device and can be activated by the appropriate output mux setting.	1
Divider Source	Selects between the PLL output and the reference clock as the source clock for the output dividers.	See Table 4 on page 8
CLKA54 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA5 and CLKA4 pair. Please refer to Table 3 on page 8 for a list of divider values.	Divide by 2
CLKA32 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA3 and CLKA2 pair. Please refer to Table 3 on page 8 for a list of divider values.	Divide by 2
CLKA10 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA1 and CLKA0 pair. Please refer to Table 3 on page 8 for a list of divider values.	Divide by 2
CLKB54 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB5 and CLKB4 pair. Please refer to Table 3 on page 8 for a list of divider values.	Divide by 2
CLKB32 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB3 and CLKB2 pair. Please refer to Table 3 on page 8 for a list of divider values.	Divide by 2
CLKB10 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB1 and CLKB0 pair. Please refer to Table 3 on page 8 for a list of divider values.	Divide by 2

Table 3 is a list of output dividers that are independently selected to connect to each output pair.

In the default (unprogrammed) state of the device, S1 and S2 pins will function as indicated in Table 4.

Table 3. Output Dividers

CLKA/B Source	Output Connects To
0 [000]	REF
1 [001]	Divide by 1
2 [010]	Divide by 2
3 [011]	Divide by 3
4 [100]	Divide by 4
5 [101]	Divide by X
6 [110]	Divide by 2X[1]
7 [111]	TEST mode [LOCK signal][2]

Table 4. S1/S2 Default Functionality

S2	S1	CLKA[5:0]	CLKB[5:0]	Divider Source
0	0	Three-state	Three-state	PLL
0	1	Driven	Three-state	PLL
1	0	Driven	Driven	Reference
1	1	Driven	Driven	PLL

Field Programming the CY23FP12

The CY23FP12 must be programmed in a device programmer prior to being installed in a circuit. The CY23FP12 is based on flash technology, so it can be reprogrammed up to 100 times. This enables fast and easy design changes and product updates, and eliminates any issues with old and out-of-date inventory.

Samples and small prototype quantities can be programmed on the CY3672-USB programmer. Cypress's value-added distribution partners and third-party programming systems from BP Microsystems, HiLo Systems, and others are available for large production quantities.

CyberClocks™ Software

CyberClocks is an easy-to-use software application that allows the user to custom-configure the CY23FP12. Users can specify the REF frequency, PLL frequency, output frequencies and/or post-dividers, and different functional options. CyberClocks outputs an industry standard JEDEC file used for programming the CY23FP12.

CyberClocks can be downloaded free of charge from the Cypress website at www.cypress.com.

CY3672-USB Development Kit

The Cypress CY3672-USB Development Kit, in combination with the CY3692 Socket Adapter, is used to program samples and small prototype quantities of the CY23FP12. This portable programmer connects to a PC via a USB interface.

CY23FP12 Frequency Calculation

The CY23FP12 is an extremely flexible clock buffer with up to twelve individual outputs, generated from an integrated PLL. Four variables are used to determine the final output frequency. These are the input Reference Frequency, the M and N dividers, and the post divider.

The basic PLL block diagram is shown in Basic PLL Block Diagram on page 5. Each of the six clock output pairs has many post divider options available to it. There are six post divider options: /1, /2, /3, /4, /X, and /2X. X is a programmable value between 5 and 130, and 2X is twice that value. The post divider options can be applied to the calculated PLL frequency or to the REF directly. The feedback is connected either internally to CLKA0 or externally to any output.

A programmable divider, M, is inserted between the reference input, REF, and the phase detector. The divider M can be any integer 1 to 256. The PLL input frequency cannot be lower than 10 MHz or higher than 200 MHz.

A programmable divider, N, is inserted between the feedback input, FBK, and the phase detector. The divider N can be any integer 1 to 256. The PLL input frequency cannot be lower than 10 MHz or higher than 200 MHz.

The output can be calculated as follows:

$F_{REF} / M = F_{FBK} / N.$

$F_{PLL} = (F_{REF} \times N \times \text{post divider}) / M.$

$F_{OUT} = F_{PLL} / \text{post divider}.$

In addition to above divider options, the following option bypasses the PLL and passes the REF directly to the output.

$F_{OUT} = F_{REF}.$

Notes
1. Outputs will be rising edge aligned only to those outputs using this same device setting.
2. When the source of an output pair is set to [111], the output pair becomes lock indicator signal. For example, if the source of an output pair (CLKA0, CLKA1) is set to [111], the CLKA0 and CLKA1, becomes lock indicator signals. In non-invert mode, CLKA0 and CLKA1 signals will be high when the PLL is in lock mode. If CLKA0 is in an invert mode, the CLKA0 will be low and the CLKA1 will be high when the PLL is in lock mode.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Non-functional	–0.5	7	VDC
V_{IN}	Input voltage REF	Relative to V_{CC}	–0.5	V_{DD} + 0.5	VDC
V_{IN}	Input voltage except REF	Relative to V_{CC}	–0.5	V_{DD} + 0.5	VDC
LU_I	Latch-up immunity	Functional	300		mA
T_S	Temperature, storage	Non-functional	–65	125	°C
T_J	Junction temperature		–	125	°C
ESD_h	ESD protection (Human body model)		2000		V
M_{SL}	Moisture sensitivity level		MSL – 3		class
G_{ATES}	Total functional gate count	Assembled Die	21375		each
UL–94	Flammability rating	At 1/8 in.	V–0		class
FIT	Failure in time	Manufacturing test	10		ppm

Operating Conditions

Parameter	Description	Test Conditions	Min	Max	Unit
V_{DDC}	Core supply voltage		3.135	3.465	V
V_{DDA}, V_{DDB}	Bank A, Bank B supply voltage		3.135	3.465	V
			2.375	2.625	V
T_A	Temperature, operating ambient	Commercial temperature	0	70	°C
		Industrial temperature	–40	85	
t_{PU}	Power-up time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic)		0.05	500	ms

DC Electrical Specifications

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW voltage[3]		–	–	0.3 × V_{DD}	V
V_{IH}	Input HIGH voltage[3]		0.7 × V_{DD}	–	–	V
I_{IL}	Input LOW current[3]	V_{IN} = 0 V	–	–	50	µA
I_{IH}	Input HIGH current[3]	V_{IN} = V_{DD}	–	–	50	µA
V_{OL}	Output LOW voltage[4]	V_{DDA}/V_{DDB} = 3.3 V, I_{OL} = 16 mA (standard drive) V_{DDA}/V_{DDB} = 3.3 V, I_{OL} = 20 mA (high drive) V_{DDA}/V_{DDB} = 2.5 V, I_{OL} = 16 mA (high drive)	–	–	0.5	V
V_{OH}	Output HIGH voltage[4]	V_{DDA}/V_{DDB} = 3.3 V, I_{OH} = –16 mA (standard drive) V_{DDA}/V_{DDB} = 3.3 V, I_{OH} = –20 mA (high drive) V_{DDA}/V_{DDB} = 2.5 V, I_{OH} = –16 mA (high drive)	V_{DD} – 0.5	–	–	V
I_{DDS}	Power-down supply current	REF = 0 MHz	–	12	50	µA
I_{DD}	Supply current	V_{DDA} = V_{DDB} = 2.5 V, Unloaded outputs at 166 MHz	–	40	65	mA
		V_{DDA} = V_{DDB} = 2.5 V, Loaded outputs at 166 MHz, C_L = 15 pF	–	65	100	
		V_{DDA} = V_{DDB} = 3.3 V, Unloaded outputs at 166 MHz	–	50	80	
		V_{DDA} = V_{DDB} = 3.3 V, Loaded outputs at166 MHz, C_L = 15 pF	–	100	120	

Thermal Resistance

Parameter [5]	Description	Test Conditions	28-pin SSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	65	°C/W
θ_{JC}	Thermal resistance (junction to case)		30	°C/W

Notes
3. Applies to both REF Clock and FBK.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.
5. These parameters are guaranteed by design and are not tested.

Switching Characteristics

Parameter [6]	Description	Test Conditions	Min	Typ	Max	Unit
f_{REF}	Reference frequency[7]	Commercial temperature	10	–	200	MHz
		Industrial temperature	10	–	166.7	
ER_{REF}	Reference edge rate		1	–	–	V/ns
DC_{REF}	Reference duty cycle		25	–	75	%
f_{OUT}	Output frequency[8]	C_L = 15 pF, Commercial temperature	10	–	200	MHz
		C_L = 15 pF, Industrial temperature	10	–	166.7	
		C_L = 30 pF, Commercial temperature	10	–	100	
		C_L = 30 pF, Industrial temperature	10	–	83.3	
DC_{OUT}	Output duty cycle[6]	$V_{DDA/B}$ = 3.3 V, measured at $V_{DD}/2$	45	50	55	%
		$V_{DDA/B}$ = 2.5 V, measured at $V_{DD}/2$	40	50	60	
t_3	Rise time[6]	$V_{DDA/B}$ = 3.3 V, 0.8 V to 2.0 V, C_L = 30 pF (standard drive and high drive)	–	–	1.6	ns
		$V_{DDA/B}$ = 3.3 V, 0.8 V,10 V to 2.0 V, C_L = 15 pF (standard drive and high drive)	–	–	0.8	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 30 pF (high drive only)	–	–	2.0	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 15 pF (high drive only)	–	–	1.0	
t_4	Fall time[6]	$V_{DDA/B}$ = 3.3 V, 0.8 V to 2.0 V, C_L = 30 pF (standard drive and high drive)	–	–	1.6	ns
		$V_{DDA/B}$ = 3.3 V, 0.8 V to 2.0 V, C_L = 15 pF (standard drive and high drive)	–	–	0.8	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 30 pF (high drive only)	–	–	1.6	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 15 pF (high drive only)	–	–	0.8	

Notes
6. All parameters are specified with loaded outputs.
7. When the device is configured as a non-PLL fanout buffer (PLL Power-down enabled), the reference frequency can be lower than 10 MHz. With auto power-down disabled and PLL power-down enabled, the reference frequency can be as low as DC level.
8. When the device is configured as a non-PLL fanout buffer (PLL Power-down enabled), the output frequency can be lower than 10 MHz. With auto power-down disabled and PLL power-down enabled, the output frequency can be as low as DC level.

Switching Characteristics (continued)

Parameter [6]	Description	Test Conditions	Min	Typ	Max	Unit
TTB	Total timing budget [9, 10], Bank A and B same frequency	Outputs at 200 MHz, tracking skew not included	–	–	650	ps
	Total timing budget, Bank A and B different frequency		–	–	850	
t_5	Output to output skew[11]	All outputs equally loaded	–	35[12]	200	ps
	Bank to bank skew	Same frequency	–	–	200	
	Bank to bank skew	Different frequency	–	–	400	
	Bank to bank skew	Different voltage, same frequency	–	–	400	
t_6	Input to output skew (static phase offset)[11]	Measured at $V_{DD}/2$, REF to FBK	–	0	250	ps
t_7	Device-to-device skew[11]	Measured at $V_{DD}/2$	–	0	500	ps
t_J	Cycle-to-cycle jitter[11] (Peak)	Banks A and B at same frequency	–	110[13]	200	ps
	Cycle-to-cycle jitter[11] (Peak)	Banks A and B at different frequencies	–	–	400	
t_{TSK}	Tracking skew	Input reference clock at < 50 KHz modulation with ±3.75% spread	–	–	200	ps
t_{LOCK}	PLL lock time[11]	Stable power supply, valid clock at REF	–	–	1.0	ms
t_{LD}	Inserted loop delay	Max loop delay for PLL Lock (stable frequency)	–	–	7	ns
		Max loop delay to meet Tracking Skew Spec	–	–	4	ns

Notes

9. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
10. TTB is the window between the earliest and the latest output clocks with respect to the input reference clock across variations in output frequency, supply voltage, operating temperature, input clock edge rate, and process. The measurements are taken with the AC test load specified and include output-output skew, cycle-cycle jitter, and dynamic phase error.TTB will be equal to or smaller than the maximum specified value at a given frequency.
11. All parameters are specified with loaded outputs.
12. Same frequency, 15 pF load, high drive.
13. Same frequency, 15 pF load, low drive.

Switching Waveforms

Figure 2. Duty Cycle Timing

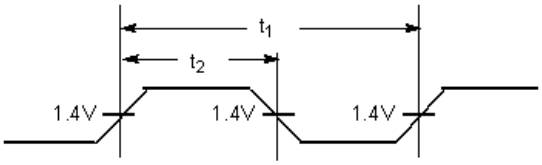


Figure 3. All Outputs Rise/Fall Time

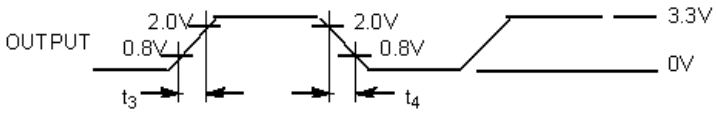


Figure 4. Output-Output Skew

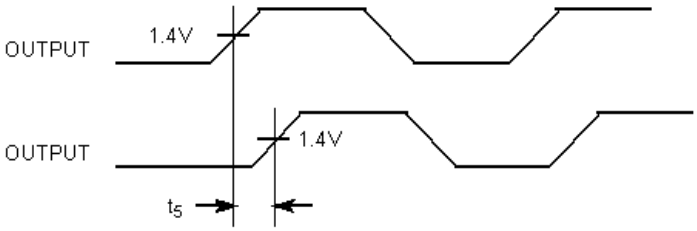


Figure 5. Input-Output Propagation Delay

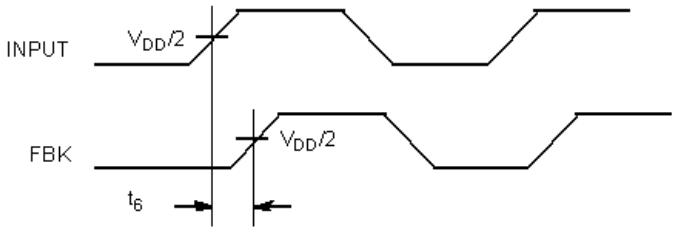
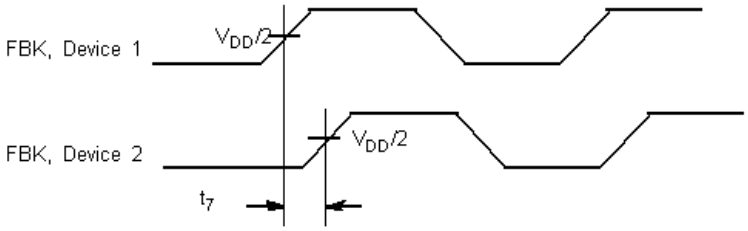
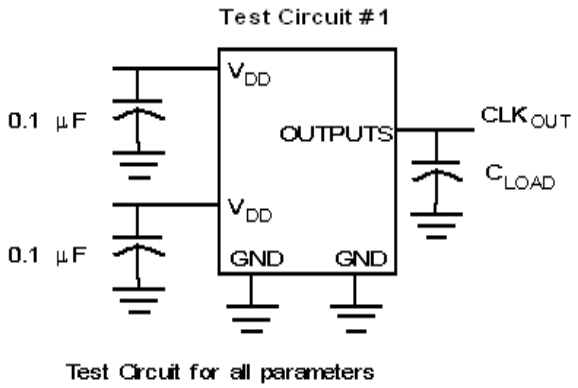


Figure 6. Device-Device Skew



Test Circuits

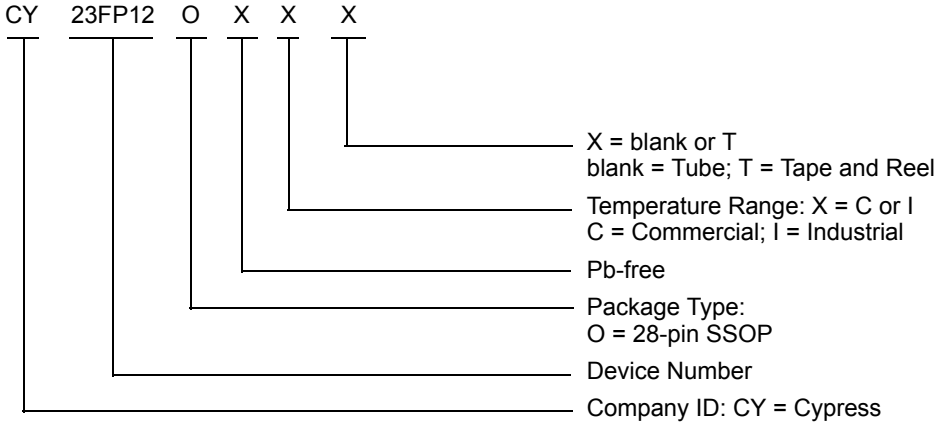
Figure 7. Test Circuits



Ordering Information

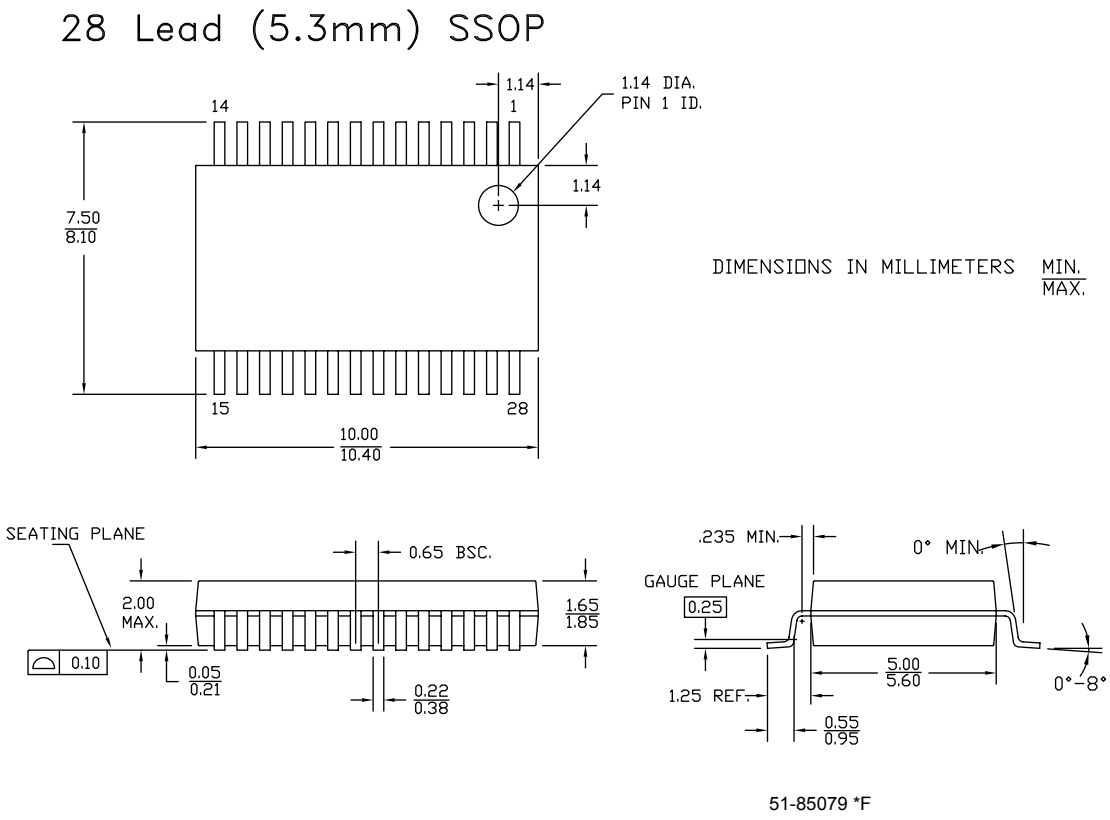
Ordering Code	Package Type	Operating Range
Pb-free		
CY23FP12OXC	28-pin SSOP	Commercial, 0 °C to 70 °C
CY23FP12OXCT	28-pin SSOP – Tape and Reel	Commercial, 0 °C to 70 °C
CY23FP12OXI	28-pin SSOP	Industrial, –40 °C to 85 °C
CY23FP12OXIT	28-pin SSOP – Tape and Reel	Industrial, –40 °C to 85 °C
Programmer		
CY3672-USB	Programmer with USB Interface	
CY3692	CY23FP12 Socket Adapter for CY3672-USB Programmer (Labeled CY3672 ADP006)	

Ordering Code Definitions



Package Drawing and Dimensions

Figure 8. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *F

Acronyms

Acronym	Description
DCXO	Digitally Controlled Crystal Oscillator
ESD	Electrostatic Discharge
PLL	Phase Locked Loop
RMS	Root Mean Square
SSOP	Shrunk Small Outline Package
XTAL	Crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY23FP12, 200 MHz Field Programmable Zero Delay Buffer Document Number: 38-07246				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	115158	07/03/02	HWT	New data sheet.
*A	121880	12/14/02	RBI	Power-up requirements added to Absolute Maximum Ratings information
*B	124523	03/19/03	RGL	Final data sheet Changed title to “200 MHz Field Programmable Zero Delay Buffer”
*C	126938	06/16/03	RGL	Interchanged REF2 in the Pin Configuration diagram Replaced all divide by 2 default value to divide by 2 in Table 2 Fixed the formula in the Frequency Calculation section
*D	129364	09/10/03	RGL	Changed the CyClocksRT trademark to CyberClocks Added Note 2 in the TEST mode in Table 3 Added T_{LD} specifications in the Switching Characteristics table
*E	299718	See ECN	RGL	Added lead-free devices Added typical values
*F	2865396	01/25/2010	KVM	Added captions to tables 1-4. Added Operating Conditions table. Various edits to text. Removed “FTG” from text about the CY3672 programmer. Specified separate commercial and industrial max values for f_{REF} Removed part numbers CY23FP12OC, CY23FP12OCT, CY23FP12OI and CY23FP12OIT. Changed part number CY3672 to CY3672-USB. Updated package drawing. Updated to new template.
*G	3146083	01/18/11	BASH	Modified V_{IN} max value from 7 to V_{DD} + 0.5 in “Absolute Maximum Conditions” on page 8. Added Ordering Code Definitions under Ordering Information. Added Acronyms and Units of Measure.
*H	4291450	02/25/2014	CINM	Updated Package Drawing and Dimensions: spec 51-85079 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*I	4580603	11/26/2014	AJU	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*J	5276049	05/27/2016	PSR	Updated Absolute Maximum Conditions: Removed ØJc, ØJa parameters and their details. Changed value of M_{SL} parameter from “MSL – 1” to “MSL – 3”. Added Thermal Resistance. Updated Package Drawing and Dimensions: spec 51-85079 – Changed revision from *E to *F. Updated to new template.
*K	5663650	03/17/2017	PAWK	Updated to new template. Completing Sunset Review.

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