

### STH270N4F3-6

### N-channel 40 V, 1.40 mΩ 180 A, H<sup>2</sup>PAK STripFET™ III Power MOSFET

#### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub> <sup>(1)</sup>
STH270N4F3-6	40 V	$<$ 1.7 m $\Omega$	180 A

- 1. Current limited by package
- Conduction losses reduced
- Low profile, very low parasitic inductance, high current package

### **Applications**

- Switching application
  - Automotive



This STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

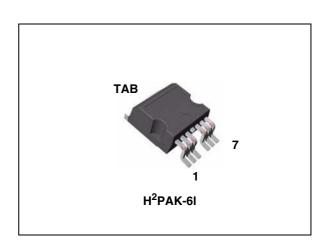


Figure 1. Internal schematic diagram

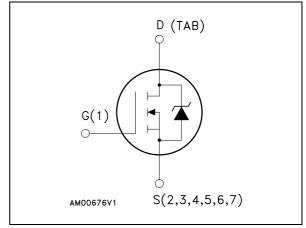


Table 1. Device summary

Order code	Marking	Package	Packaging
STH270N4F3-6	270N4F3	H <sup>2</sup> PAK	Tape and reel

Contents STH270N4F3-6

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STH270N4F3-6 Electrical ratings

## 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (v <sub>gs</sub> = 0)	40	V
V <sub>GS</sub>	Gate-source voltage	± 20	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	180	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	180	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	720	Α
P <sub>TOT</sub> (2)	Total dissipation at T <sub>C</sub> = 25 °C	300	W
	Derating factor	2	W/°C
E <sub>AS</sub> (3)	Single pulse avalanche energy	1000	mJ
T <sub>stg</sub>	Storage temperature	-55 to 175	
T <sub>j</sub>	Operating junction temperature	-55 to 175	°C

<sup>1.</sup> Current limited by package

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.5	°C/W
R <sub>thj-pcb</sub> (1)	Thermal resistance junction-pcb max	35	°C/W

<sup>1.</sup> When mounted on 1 inch2 FR-4 2 oz Cu.

<sup>2.</sup> This value is rated according to Rthj-c

<sup>3.</sup> Starting Tj = 25 °C,  $I_D$  = 80 A,  $V_{DD}$  = 32 V

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### 2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	40			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max rating, $V_{DS}$ = Max rating, $T_c$ =125°C			10 100	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>DS</sub> = ± 20V			±200	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2		4	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 80A		1.40	1.70	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	$V_{DS} = 10V, I_{D} = 100A$		200		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> =0		7400 1800 50		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ = 20V, $I_{D}$ = 160A, $V_{GS}$ = 10V (see Figure 14)		110 30 25	150	nC nC nC

<sup>1.</sup> Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time Rise time	$V_{DD}$ = 20V, $I_D$ = 80A $R_G$ = 4.7 $\Omega$ $V_{GS}$ = 10V, (see Figure 13)		25 180		ns ns
t <sub>d(off)</sub>	Turn-off delay time Fall time	$V_{DD}$ = 20V, $I_D$ = 80A $R_G$ = 4.7 $\Omega$ $V_{GS}$ = 10V, (see Figure 13)		110 45		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current Source-drain current (pulsed)				180 720	A A
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	$I_{SD} = 180 \text{ A}, V_{GS} = 0$			1.5	٧
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}$ = 160 A,di/dt = 100A/ $\mu$ s $V_{DD}$ = 32V, $T_j$ = 150°C (see Figure 15)		70 225 3.2		ns nC A

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5%

Electrical characteristics STH270N4F3-6

#### 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

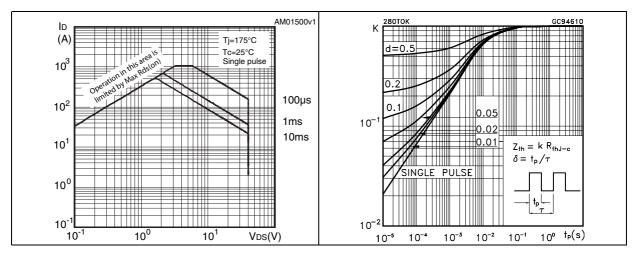


Figure 4. Output characteristics

Figure 5. Transfer characteristics

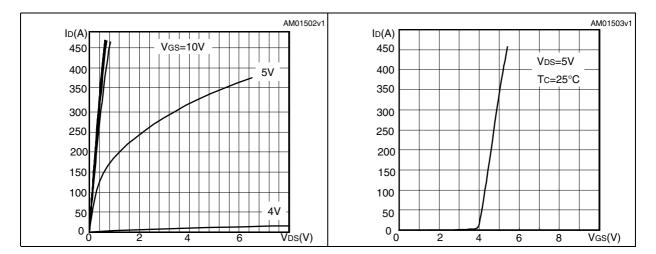
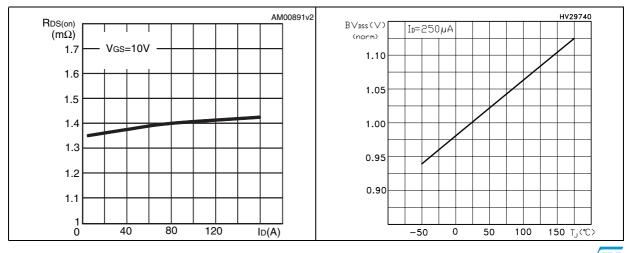


Figure 6. Static drain-source on resistance

Figure 7. Normalized B<sub>VDSS</sub> vs temperature



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Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

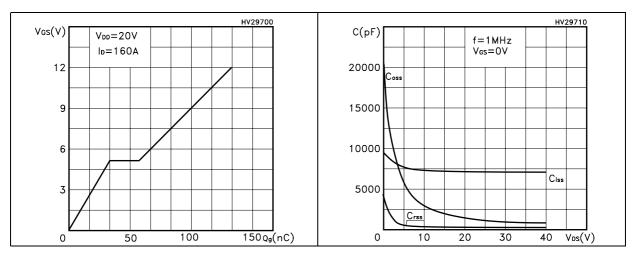


Figure 10. Normalized gate threshold voltage Figure 11. Normalized on resistance vs vs temperature temperature

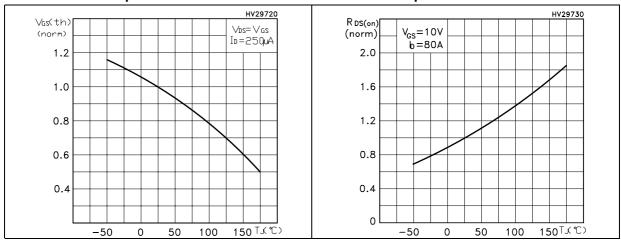
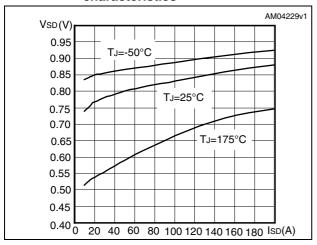


Figure 12. Source-drain diode forward characteristics



Test circuits STH270N4F3-6

### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

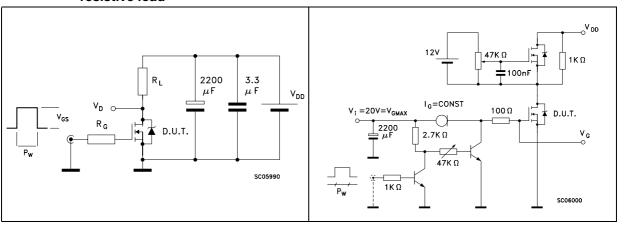


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

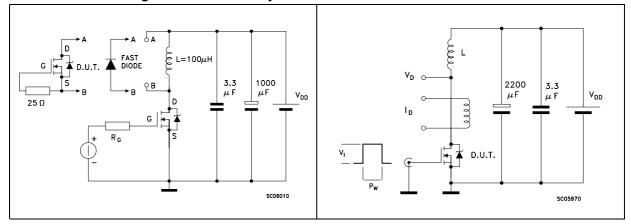
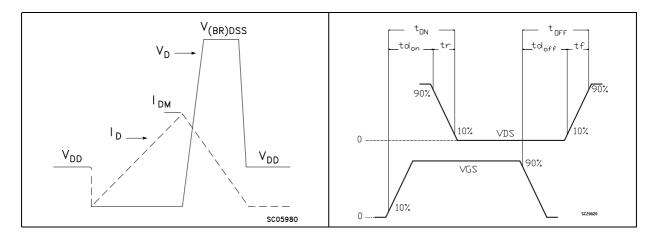


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



### 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. H<sup>2</sup>PAK 6 leads mechanical data

Dim	Dim.		
DIM.	Min.	Max.	
Α	4.30		4.80
A1	0.03		0.20
С	1.17		1.37
е	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
Е	0.45		0.60
F	0.50		0.70
Н	10.00		10.40
H1	7.80	- 	8.20
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	7.45		7.85
L4	1.5	1	1.75
М	1.90	1	2.50
R	0.20	1	0.60
V	0°		8°

Figure 19. H<sup>2</sup>PAK 6 leads drawing

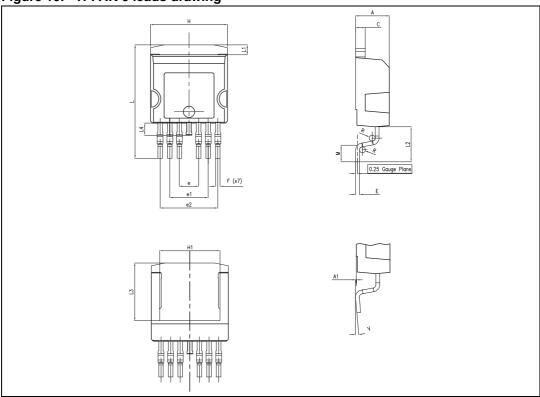
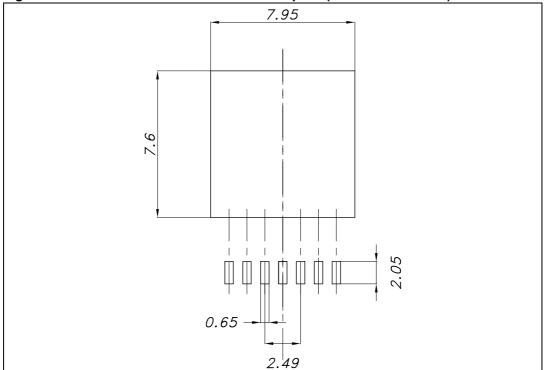


Figure 20. H<sup>2</sup>PAK 6 leads recommended footprint (dimensions in mm)



### 5 Packaging mechanical data

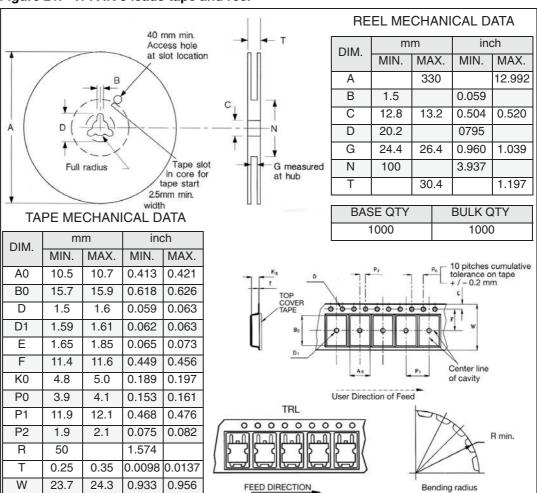


Figure 21. H<sup>2</sup>PAK 6 leads tape and reel

Revision history STH270N4F3-6

# 6 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Jan-2010	1	Initial release

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