2 dB LSB, 4-Bit, Silicon Digital Attenuator, 10 MHz to 60 GHz

Data Sheet **ADRF5740**

FEATURES

- Ultrawideband frequency range: 10 MHz to 60 GHz
- Attenuation range: 2 dB steps to 22 dB
- Low insertion loss
  - 1.4 dB up to 20 GHz
  - 2.2 dB up to 44 GHz
  - 3.3 dB up to 55 GHz
- Attenuation accuracy
  - ±(0.1 + 1.0% of state) up to 20 GHz
  - ±(0.2 + 3.0% of state) up to 44 GHz
  - ±(0.2 + 7.0% of state) up to 55 GHz
- Typical step error
  - ±0.30 dB up to 20 GHz
  - ±0.50 dB up to 44 GHz
  - ±0.60 dB up to 55 GHz
- High input linearity
  - P0.1dB: 25.5 dBm typical
  - IP3: 45 dBm typical
- High RF input power handling: 24 dBm average, 24 dBm peak
- Tight distribution in relative phase
- No low frequency spurious signals
- Parallel mode control, CMOS and LVTTL compatible
- RF amplitude settling time (0.1 dB of final RF output): 175 ns
- 16-terminal, 2.5 mm × 2.5 mm, RoHS compliant LGA package

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G millimeter wave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

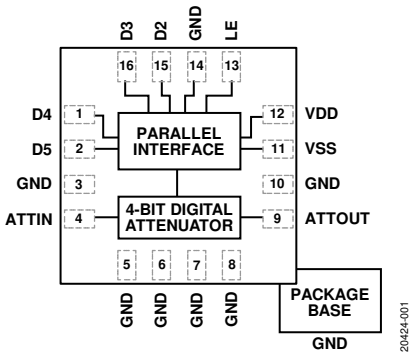

Figure 1.

GENERAL DESCRIPTION

The ADRF5740 is a silicon, 4-bit digital attenuator with 22 dB attenuation control range in 2 dB steps.

The ADRF5740 operates from 10 MHz to 60 GHz with less than 3.3 dB of insertion loss and with ±(0.2 + 7.0% of attenuation state) of attenuation accuracy at 55 GHz. The ATTIN port of the ADRF5740 has an RF input power handling capability of 24 dBm average and 24 dBm peak for all states.

The ADRF5740 requires a dual supply voltage of +3.3 V and −3.3 V. The ADRF5740 features parallel mode control, and CMOS- and low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5740 RF ports are designed to match a characteristic impedance of 50 Ω. The ADRF5740 comes in a 16-terminal, 2.5 mm × 2.5 mm, RoHS compliant, land grid array (LGA) package and operates from −40°C to +105°C.

Rev. 0 Document Feedback

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REVISION HISTORY

6/2020—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, digital voltages = 0 V or VDD, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		10		60,000	MHz
INSERTION LOSS	10 MHz to 20 GHz		1.4		dB
	20 GHz to 44 GHz		2.2		dB
	44 GHz to 55 GHz		3.3		dB
	55 GHz to 60 GHz		4.4		dB
RETURN LOSS	ATTIN and ATTOUT, all attenuation states				
	10 MHz to 20 GHz		14		dB
	20 GHz to 44 GHz		13		dB
	44 GHz to 55 GHz		12		dB
	55 GHz to 60 GHz		10		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		22		dB
Step Size	Between any successive attenuation states		2		dB
Accuracy	Referenced to insertion loss				
	10 MHz to 20 GHz		±(0.1 + 1.0% of state)		dB
	20 GHz to 44 GHz		±(0.2 + 3.0% of state)		dB
	44 GHz to 55 GHz		±(0.2 + 7.0% of state)		dB
	55 GHz to 60 GHz		±(0.3 + 7.0% of state)		dB
Step Error	Between any successive state				
	10 MHz to 20 GHz		±0.30		dB
	20 GHz to 44 GHz		±0.50		dB
	44 GHz to 55 GHz		±0.60		dB
	55 GHz to 60 GHz		±1.2		dB
RELATIVE PHASE	Referenced to insertion loss				
	10 MHz to 20 GHz		22		Degrees
	20 GHz to 44 GHz		55		Degrees
	44 GHz to 55 GHz		65		Degrees
	55 GHz to 60 GHz		70		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at input power = 10 dBm				
Rise and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output		50		ns
On and Off Time (t_{ON} and t_{OFF})	50% triggered control to 90% of RF output		100		ns
RF Amplitude Settling Time					
0.1 dB	50% triggered control to 0.1 dB of final RF output		175		ns
0.05 dB	50% triggered control to 0.05 dB of final RF output		225		ns
Overshoot			2		dB
Undershoot			0.75		dB
RF Phase Settling Time	f = 40 GHz				
5°	50% triggered control to 5° of final RF output		105		ns
1°	50% triggered control to 1° of final RF output		120		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT LINEARITY[1]	100 MHz to 50 GHz				
0.1 dB Power Compression (P0.1dB)			25.5		dBm
1 dB Power Compression (P1dB)			26.5		dBm
Third-Order Intercept (IP3)	Two-tone input power = 12 dBm per tone, Δf = 1 MHz, all attenuation states		45		dBm
DIGITAL CONTROL INPUTS	LE, D2, D3, D4, D5 pins				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low (I_{INL})			−10		µA
High (I_{INH})	LE, D2, D3, D4, D5 pins		<1		µA
SUPPLY CURRENT					
Positive Supply Current (I_{DD})	VDD pin				
Bias Low	LE, D2, D3, D4, D5 = 0 V		52		µA
Bias High	LE, D2, D3, D4, D5 = 3.3 V		2		µA
Negative Supply Current (I_{SS})	VSS pin		−110		µA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
VDD		3.15		3.45	V
VSS		−3.45		−3.15	V
Digital Control Voltage		0		VDD	V
RF Power[2]	f = 100 MHz to 50 GHz, T_{CASE} = 85°C,[3] all attenuation states				
Input at ATTIN	Steady state, average			24	dBm
	Steady state, peak			24	dBm
	Hot switching, average			24	dBm
	Hot switching, peak			24	dBm
Input at ATTOUT	Steady state, average			16	dBm
	Steady state, peak			16	dBm
	Hot switching, average			16	dBm
	Hot switching, peak			16	dBm
T_{CASE}		−40		+105	°C

[1] Input linearity performance degrades over frequency (see Figure 21 and Figure 22).
[2] For power derating over frequency, see Figure 2 and Figure 3. Power derating is applicable for all ATTIN and ATTOUT power specifications.
[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

TIMING SPECIFICATIONS

See Figure 24 for the timing diagram.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{LEW}	Minimum LE pulse width		10		ns
t_{PH}	Hold time		10		ns
t_{PS}	Setup time		2		ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input Voltage	−0.3 V to VDD + 0.3 V
RF Power[1] (f = 100 MHz to 50 GHz, T_{CASE} = 85°C[2])	
Input at ATTIN	
Steady State, Average	25 dBm
Steady State, Peak	25 dBm
Hot Switching, Average	25 dBm
Hot Switching, Peak	25 dBm
Input at ATTOUT	
Steady State, Average	17 dBm
Steady State, Peak	17 dBm
Hot Switching, Average	17 dBm
Hot Switching, Peak	17 dBm
RF Power Under Unbiased Condition[1] (VDD, VSS = 0 V)	
Input at ATTIN	18 dBm
Input at ATTOUT	10 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C
Continuous Power Dissipation (P_{DISS})	0.25 W

[1] For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.
[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ESDA/JEDEC JS-002.

ESD Ratings for ADRF5740

Table 4. ADRF5740, 16-Terminal LGA

ESD Model	Withstand Threshold (V)
HBM	
ATTIN and ATTOUT Pins	±250
Supply and Control Pins	±2000
FICDM	±1250

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-16-6	200	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pad to the PCB. The ground pad is held constant at 85°C operating temperature.

POWER DERATING CURVES

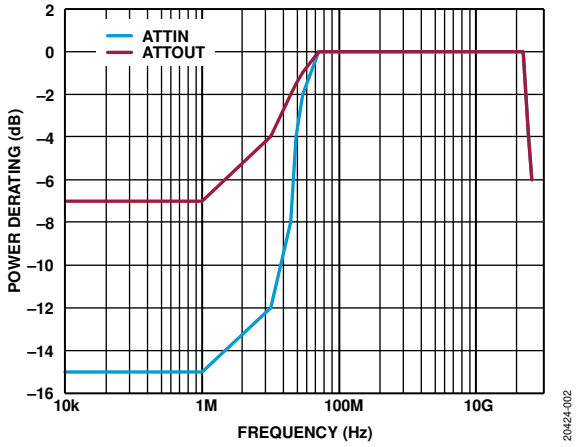

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

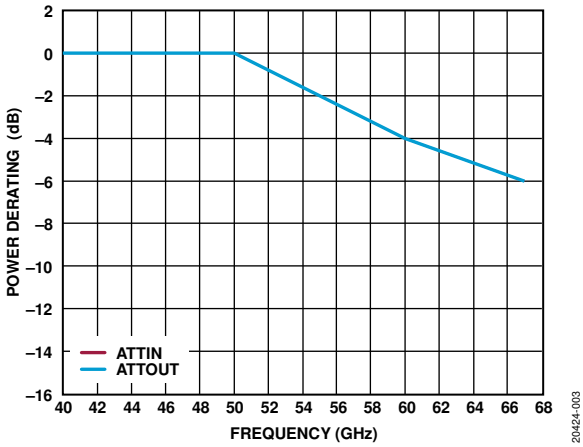

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

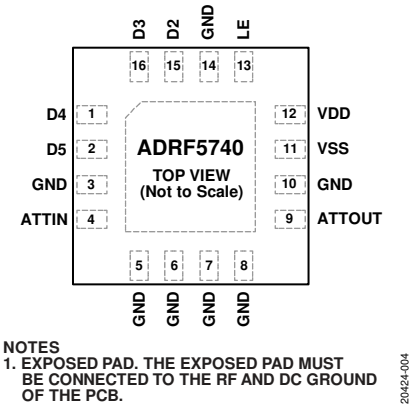

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D4	Parallel Control Input for 8 dB Attenuator Bit. See the Theory of Operation section for more information.
2	D5	Parallel Control Input for 8 dB Attenuator Bit. See the Theory of Operation section for more information.
3, 5 to 8, 10, 14	GND	Ground. The GND pins must be connected to the RF and dc ground of the PCB.
4	ATTIN	Attenuator Input. The ATTIN pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
9	ATTOUT	Attenuator Output. The ATTOUT pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
11	VSS	Negative Supply Input.
12	VDD	Positive Supply Input.
13	LE	Latch Enable Input. See the Theory of Operation section for more information.
15	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information.
16	D3	Parallel Control Input for 4 dB Attenuator Bit. See the Theory of Operation section for more information.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB.

INTERFACE SCHEMATICS

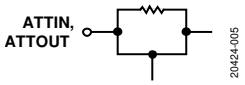

Figure 5. ATTIN and ATTOUT Interface

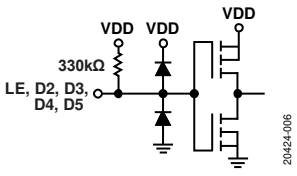

Figure 6. Digital Input Interface (LE, D2, D3, D4, D5)

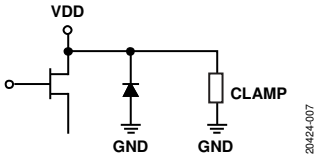

Figure 7. VDD Pin Interface Schematic

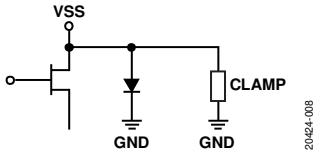

Figure 8. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

VDD = 3.3 V, VSS = −3.3 V, digital voltages = 0 V or VDD, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. Measured on the ADRF5740-EVALZ-185. See the Applications Information section for details on the evaluation board.

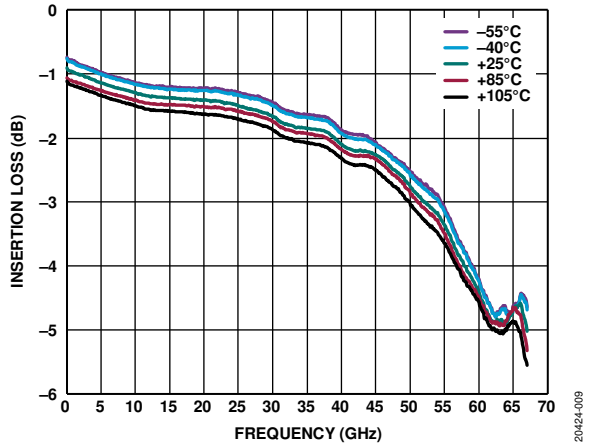

Figure 9. Insertion Loss vs. Frequency over Temperature

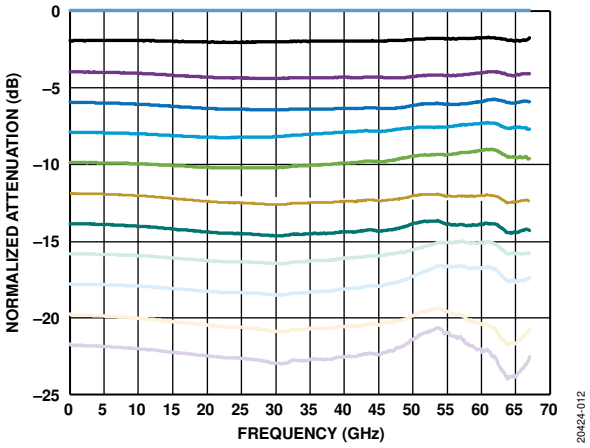

Figure 12. Normalized Attenuation vs. Frequency for All States at Room Temperature

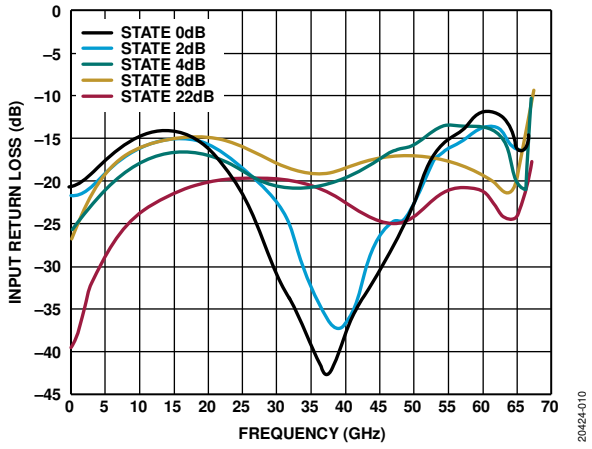

Figure 10. Input Return Loss vs. Frequency (Major States Only)

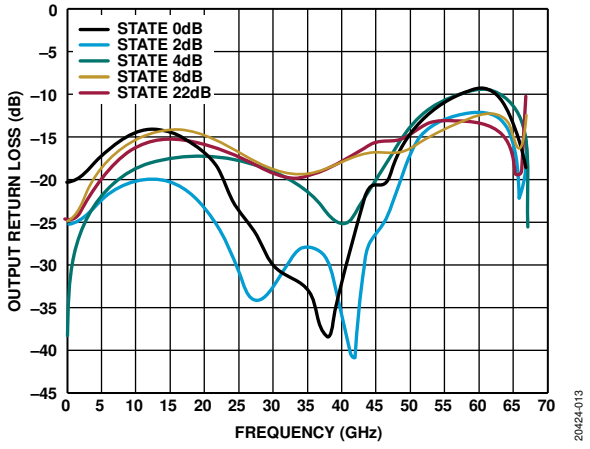

Figure 13. Output Return Loss vs. Frequency (Major States Only)

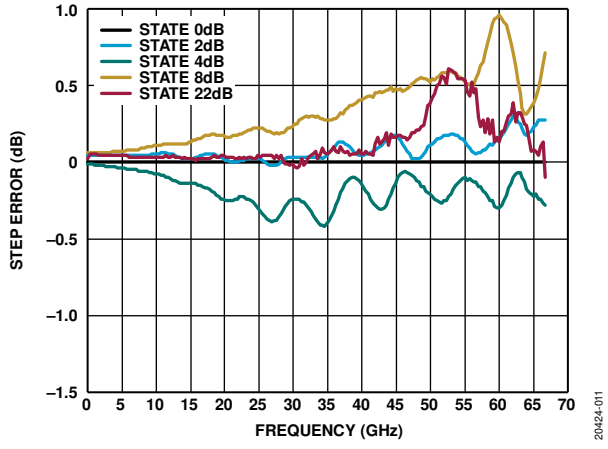

Figure 11. Step Error vs. Frequency (Major States Only)

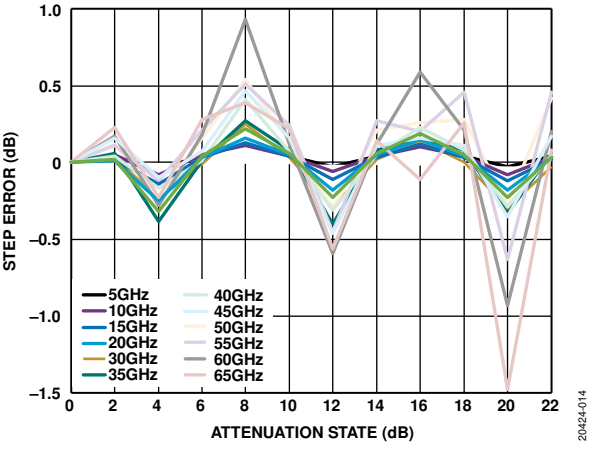

Figure 14. Step Error vs. Attenuation State over Frequency

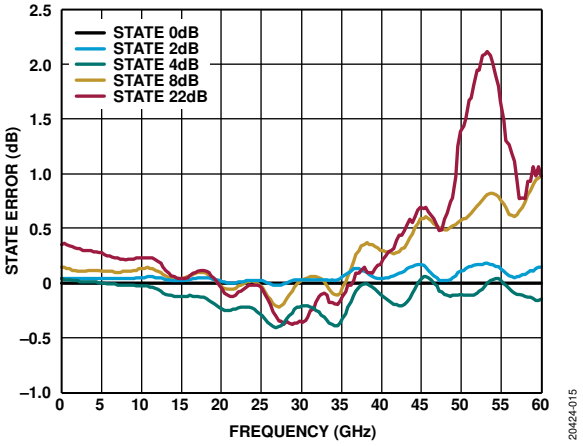

Figure 15. State Error vs. Frequency (Major States Only)

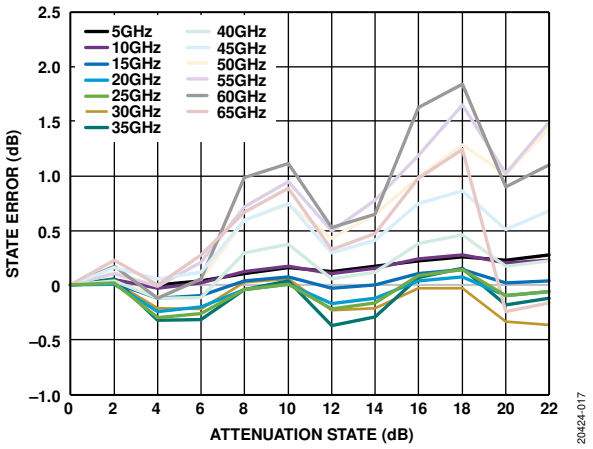

Figure 17. State Error vs. Attenuation State over Frequency

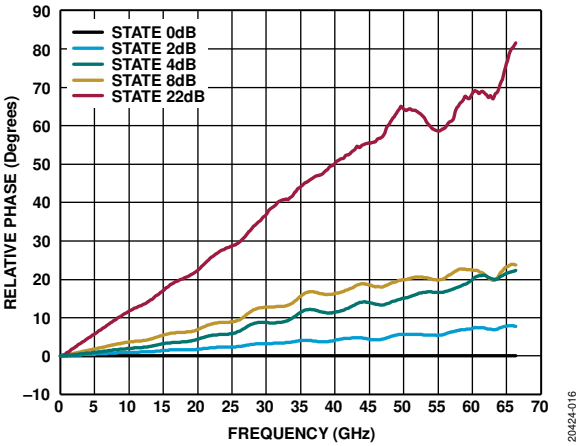

Figure 16. Relative Phase vs. Frequency (Major States Only)

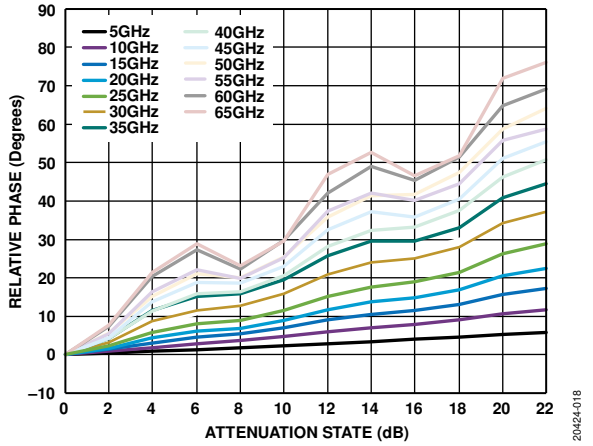

Figure 18. Relative Phase vs. Attenuation State over Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

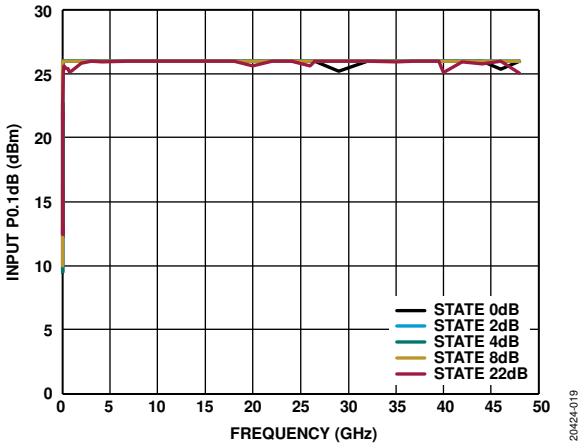

Figure 19. Input P0.1dB vs. Frequency (Major States Only)

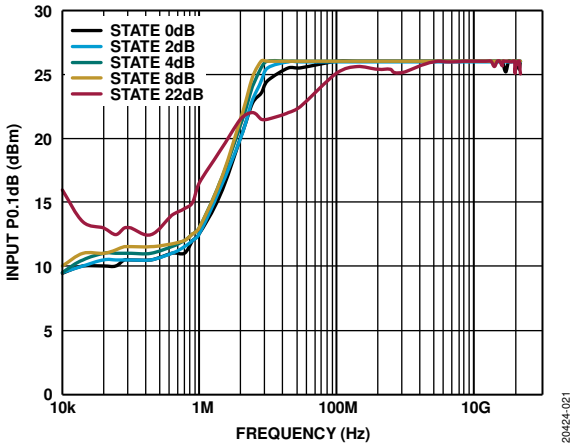

Figure 21. Input P0.1dB vs. Frequency (Major States Only), Low Frequency Detail

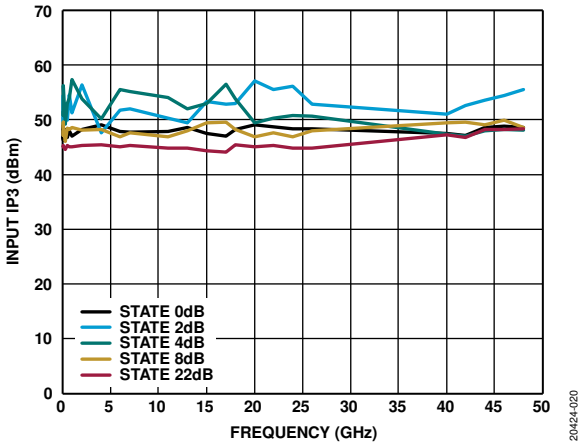

Figure 20. Input IP3 vs. Frequency (Major States Only)

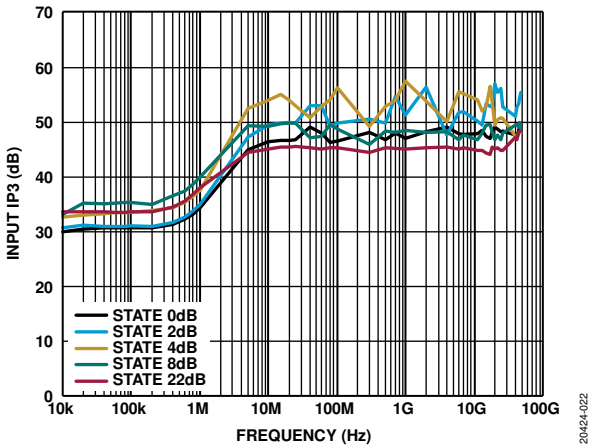

Figure 22. Input IP3 vs. Frequency (Major States Only), Low Frequency Detail

THEORY OF OPERATION

The ADRF5740 incorporates a 4-bit fixed attenuator array that offers an attenuation range of 22 dB in 2 dB steps. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5740 has four digital control inputs, D2 (LSB) to D5, to select the desired attenuation state in parallel mode, as shown in Figure 23. Internally, there are two 8 dB stages, and these can be controlled by the D4 and D5 pins.

POWER SUPPLY

The ADRF5740 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Power up the digital control inputs. The relative order of the digital control inputs is not important. However, powering the digital control inputs before the VDD supply may inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5740 has internal pull-up resistors (see Figure 6). The internal pull-up resistors set the attenuator to the maximum attenuation state (22 dB) when the VDD and VSS voltages are applied.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are dc-coupled to 0 V. DC blocking is not required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching components are not required.

The ADRF5740 supports bidirectional operation at a lower power level. The power handling of the ATTIN and ATTOUT ports are different. Therefore, the bidirectional power handling is defined by the ATTOUT port. Refer to the RF input power specifications in Table 1.

Table 7. Recommended Truth Table

Digital Control Input[1]				
D5[2]	D4[2]	D3	D2	Attenuation State (dB)
Low	Low	Low	Low	0 (reference)
Low	Low	Low	High	2
Low	Low	High	Low	4
Low	Low	High	High	6
Low	High	Low	Low	8
Low	High	Low	High	10
Low	High	High	Low	12
Low	High	High	High	14
High	High	Low	Low	16
High	High	Low	High	18
High	High	High	Low	20
High	High	High	High	22

[1] Any combination of the control voltage input states shown in Table 7 provides an attenuation equal to the sum of the bits selected.
[2] D4 and D5 both correspond to the 8 dB state. D4 has slightly higher accuracy over states at higher frequencies.

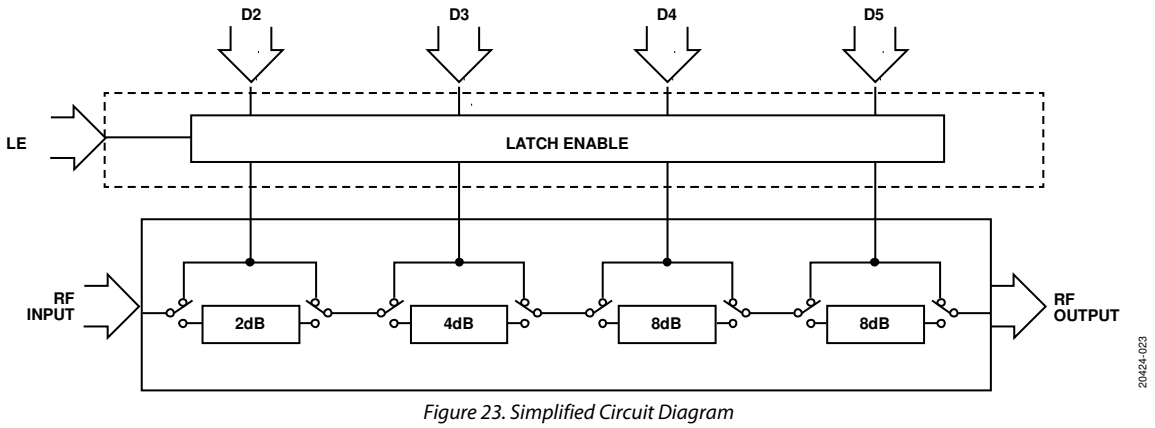

Figure 23. Simplified Circuit Diagram

PARALLEL MODE INTERFACE

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pin high. To change the attenuation state, use the control voltage inputs (D2 to D5) directly. Direct parallel mode is for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, keep the LE pin low when changing the control voltage inputs (D2 to D5) to set the attenuation state. The LE pin is level triggered. When the desired attenuation state is set, toggle LE high to transfer the data to the bypass switches of the attenuator array. Then, toggle LE low to secure the change into the device until the next required attenuation change.

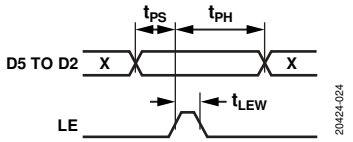

Figure 24. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS

All measurements in this data sheet are measured on the ADRF5740-EVALZ-185 evaluation board. The design of the ADRF5740-EVALZ-185 and the ADRF5740-EVALZ-292 serves as a layout recommendation for the ADRF5740 application.

See the ADRF5740-EVALZ-185 and the ADRF5740-EVALZ-292 user guide for more information on using the evaluation boards.

BOARD LAYOUT

The ADRF5740-EVALZ-185 and the ADRF5740-EVALZ-292 are 4-layer evaluation boards. The outer copper (Cu) layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. Figure 25 shows the ADRF5740-EVALZ-185 and the ADRF5740-EVALZ-292 stack up.

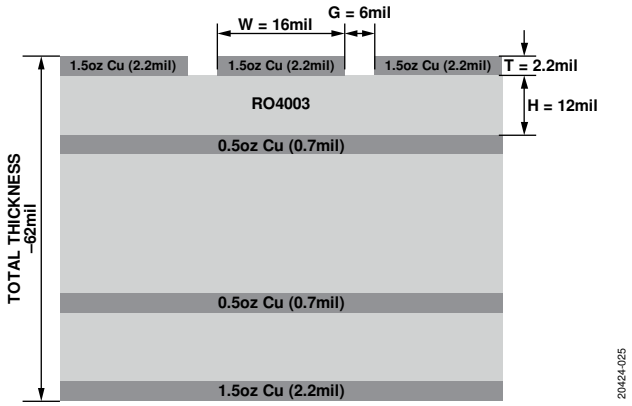

Figure 25. ADRF5740-EVALZ-185 and ADRF5740-EVALZ-292 Stack Up

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 12 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 1.85 mm RF launchers to be connected at the board edges.

RF AND DIGITAL CONTROLS

The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a trace width of 16 mil and ground clearance of 6 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many through vias as possible are arranged around transmission lines and under the exposed pad of the package.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines to the 1.85 mm RF launchers. On the VDD and VSS supply traces, a 100 pF bypass capacitor filters high frequency noise.

Figure 26 shows the simplified application circuit for the ADRF5740.

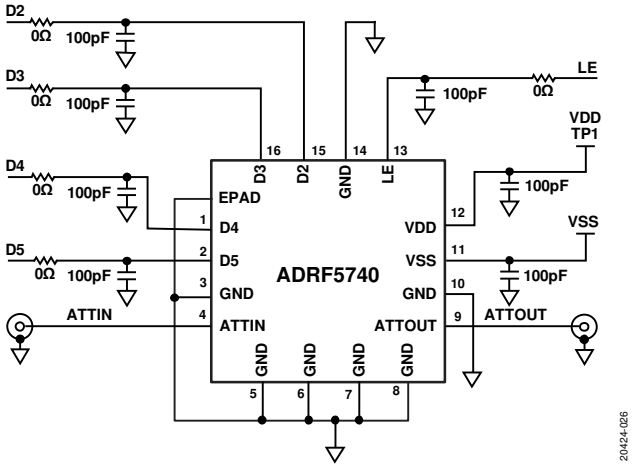

Figure 26. Simplified Application Circuit

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

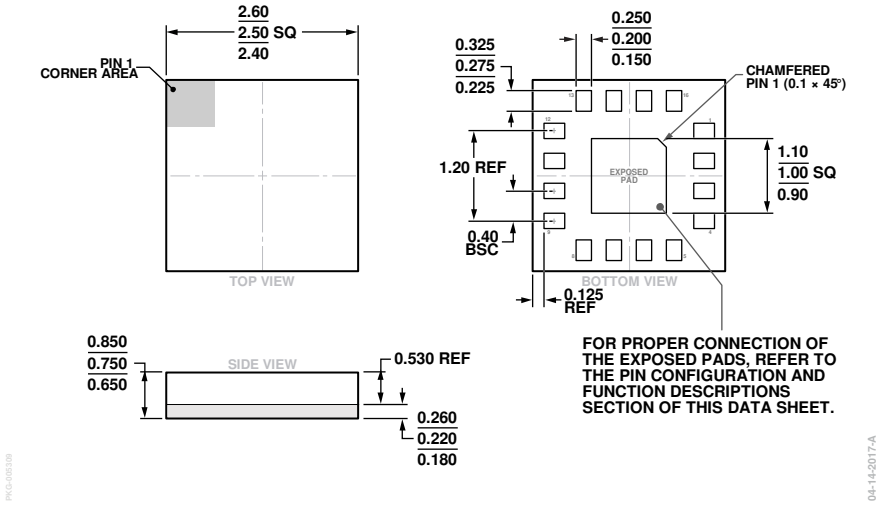

Figure 27. 16-Terminal Land Grid Array [LGA]
2.5 mm × 2.5 mm Body and 0.75 mm Package Height
(CC-16-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADRF5740BCCZN	−40°C to +105°C	16-Terminal Land Grid Array [LGA]	CC-16-6	FF
ADRF5740BCCZN-R7	−40°C to +105°C	16-Terminal Land Grid Array [LGA]	CC-16-6	FF
ADRF5740-EVALZ-185		Evaluation Board with 1.85 mm Connectors		
ADRF5740-EVALZ-292		Evaluation Board with 2.92 mm Connectors		

[1] Z = RoHS Compliant Part