

## N-channel 650 V, 0.067 $\Omega$ typ., 35 A MDmesh™ V Power MOSFET in D<sup>2</sup>PAK, TO-220FP and TO-220 packages

Datasheet – production data

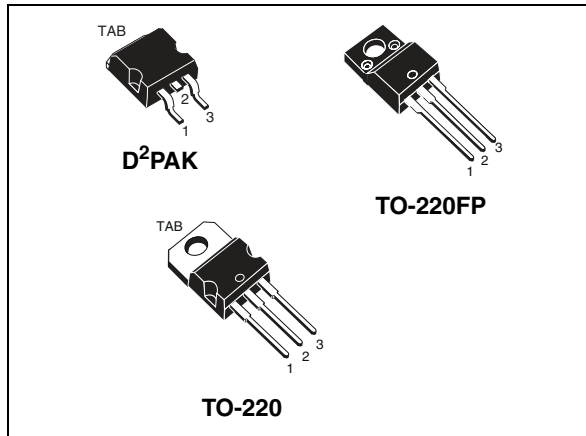
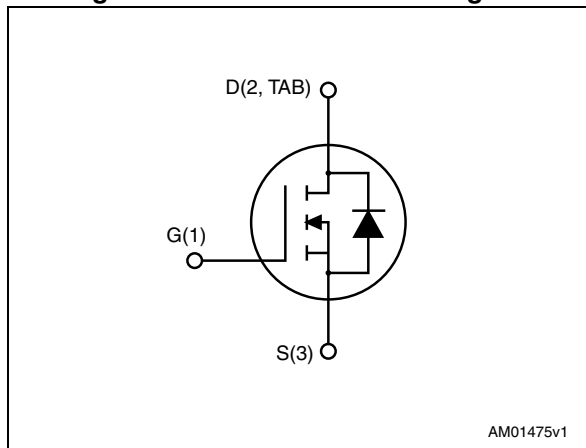


Figure 1. Internal schematic diagram



### Features

Order codes	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STB45N65M5	710 V	0.078 $\Omega$	35 A
STF45N65M5			
STP45N65M5			

- Worldwide best R<sub>DS(on)</sub> \* area
- Higher V<sub>DSS</sub> rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

### Applications

- Switching applications

### Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB45N65M5	45N65M5	D <sup>2</sup> PAK	Tape and reel
STF45N65M5		TO-220FP	Tube
STP45N65M5		TO-220	

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK TO-220	TO-220FP	
V <sub>GS</sub>	Gate-source voltage	± 25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	35	35 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	22	22 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	140	140 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	210	40	W
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	15		V/ns
dv/dt <sup>(3)</sup>	MOSFET dv/dt ruggedness	50		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)		2500	V
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature	150		°C

- Limited by maximum junction temperature.
- $I_{SD} \leq 35$  A,  $di/dt \leq 400$  A/ $\mu$ s,  $V_{DS(Peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400$  V
- $V_{DS} \leq 480$  V

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		D <sup>2</sup> PAK	TO-220FP	TO-220	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.60	3.13	0.60	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	30			°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		62.5		°C/W

- When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	9	A
E <sub>AS</sub>	Single pulse avalanche energy (starting t <sub>j</sub> =25°C, I <sub>d</sub> = I <sub>AR</sub> ; V <sub>dd</sub> =50)	810	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$		0.067	0.078	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	3470	-	pF
$C_{oss}$	Output capacitance			82		
$C_{rss}$	Reverse transfer capacitance			7		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0$	-	280	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			79		
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 17.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 18</a> )	-	82	-	nC
$Q_{gs}$	Gate-source charge			18.5		
$Q_{gd}$	Gate-drain charge			35		

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_d$ (v)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 23$ A,		79.5		ns
$t_r$ (v)	Voltage rise time	$R_G = 4.7$ $\Omega$ , $V_{GS} = 10$ V		11		ns
$t_f$ (i)	Current fall time	(see <a href="#">Figure 19</a> and	-	9.3	-	ns
$t_c$ (off)	Crossing time	<a href="#">Figure 22</a> )		16		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				35	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		140	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 35$ A, $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 35$ A, $di/dt = 100$ A/ $\mu$ s		392		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V (see <a href="#">Figure 19</a> )	-	7.4		$\mu$ C
$I_{RRM}$	Reverse recovery current			38		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 35$ A, $di/dt = 100$ A/ $\mu$ s		468		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V, $T_j = 150$ °C	-	9.7		$\mu$ C
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 19</a> )		42		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK and TO-220

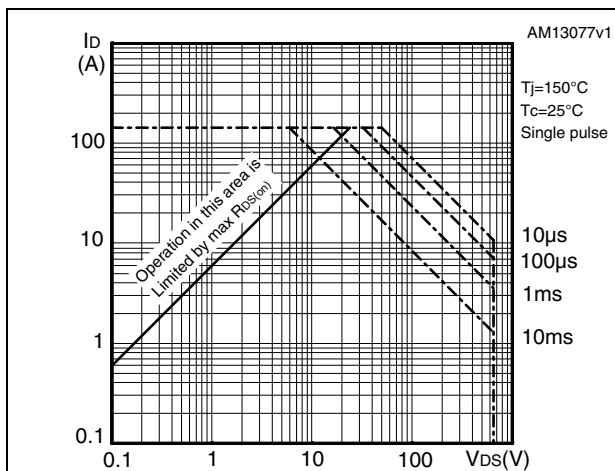


Figure 3. Thermal impedance for D<sup>2</sup>PAK and TO-220

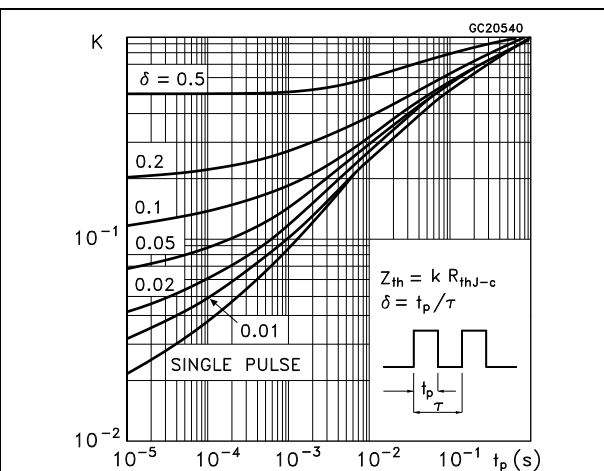


Figure 4. Safe operating area TO220FP

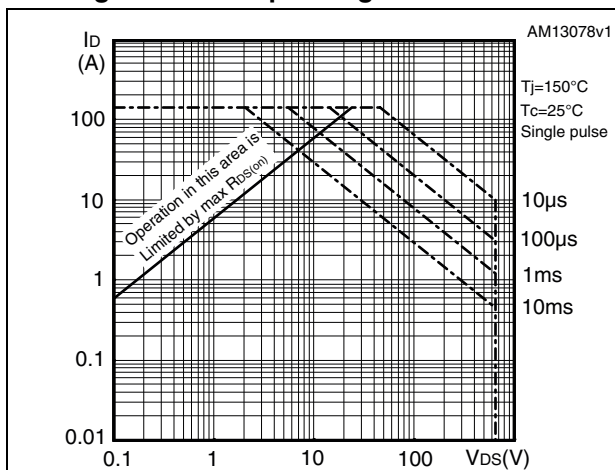


Figure 5. Thermal impedance for TO-220FP

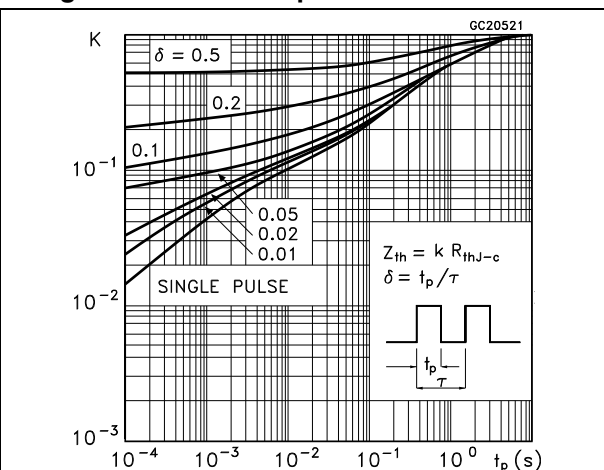


Figure 6. Output characteristics

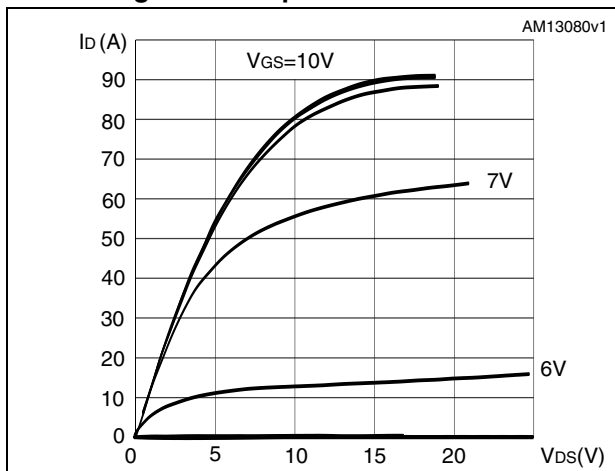


Figure 7. Transfer characteristics

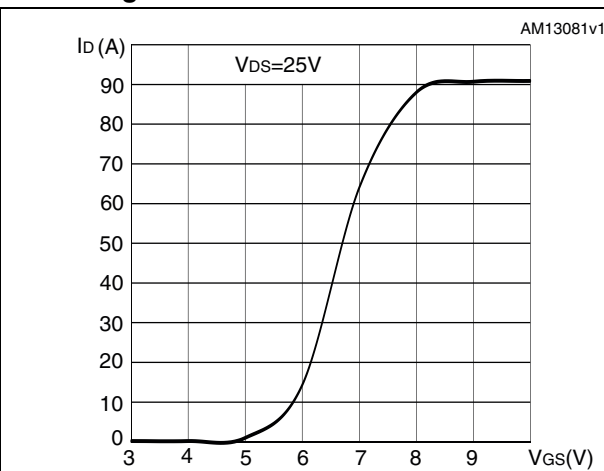


Figure 8. Gate charge vs gate-source voltage

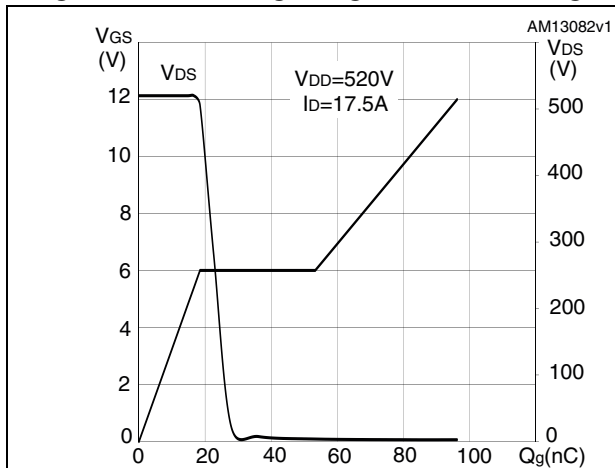


Figure 9. Static drain-source on-resistance

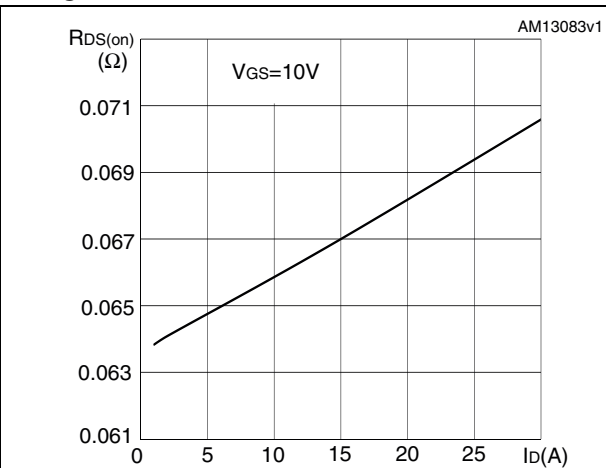


Figure 10. Capacitance variations

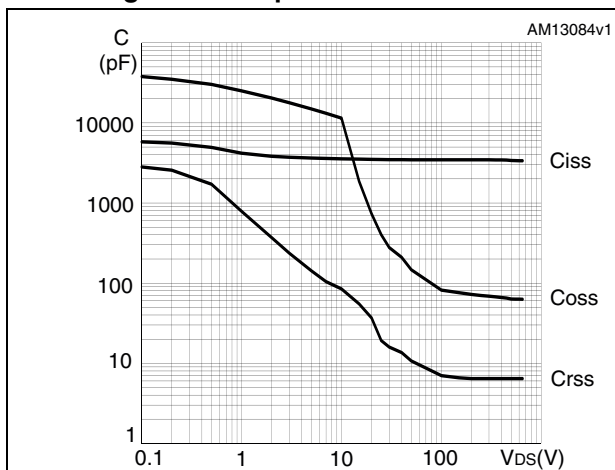


Figure 11. Output capacitance stored energy

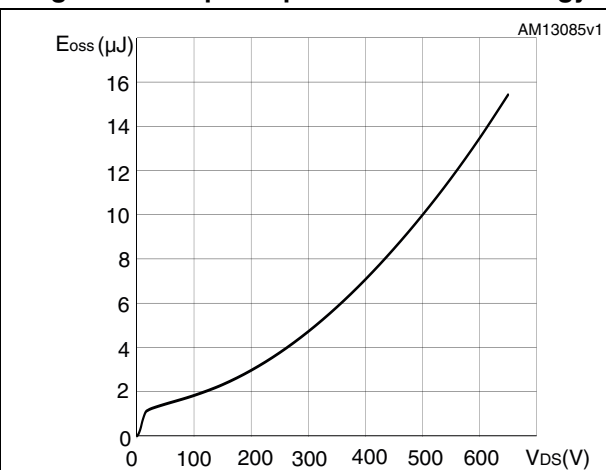


Figure 12. Normalized gate threshold voltage vs. temperature

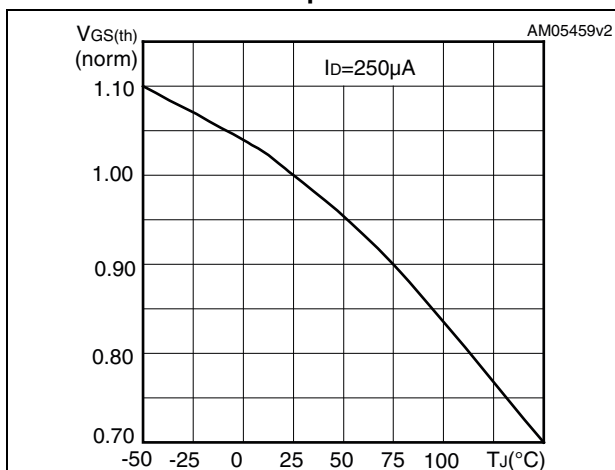


Figure 13. Normalized on resistance vs. temperature

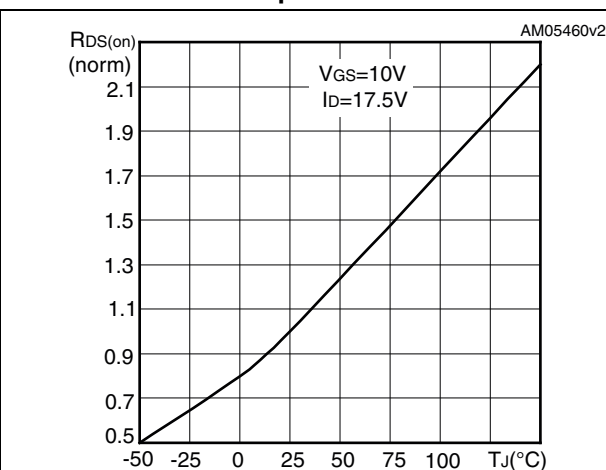


Figure 14. Drain-source diode forward characteristics

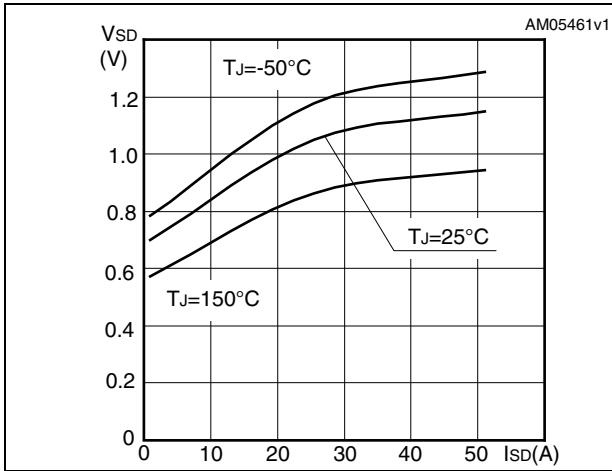


Figure 15. Normalized  $V_{DS}$  vs. temperature

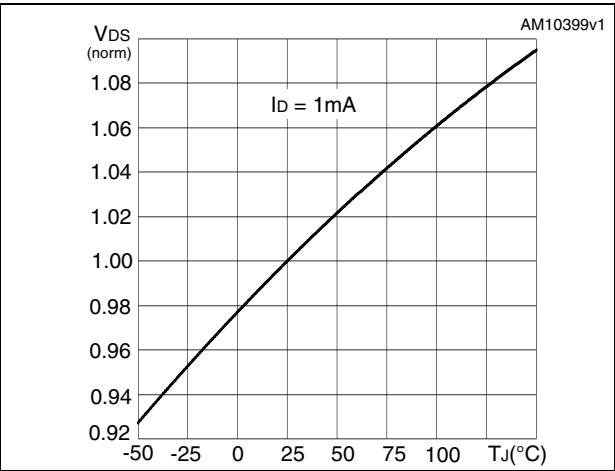
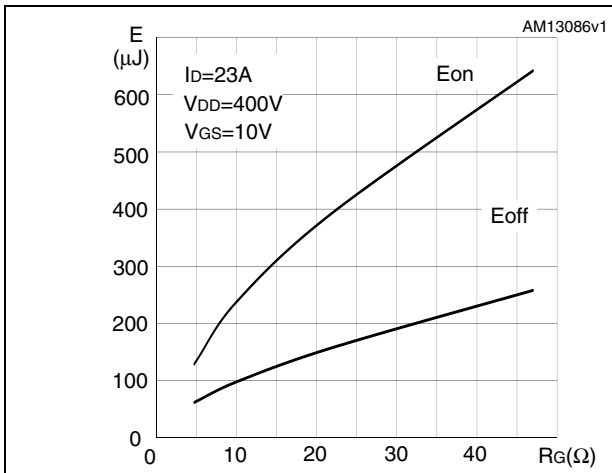


Figure 16. Switching losses vs. gate resistance (1)



1. Eon including reverse recovery of a SiC diode



### 3 Test circuits

Figure 17. Switching times test circuit for resistive load

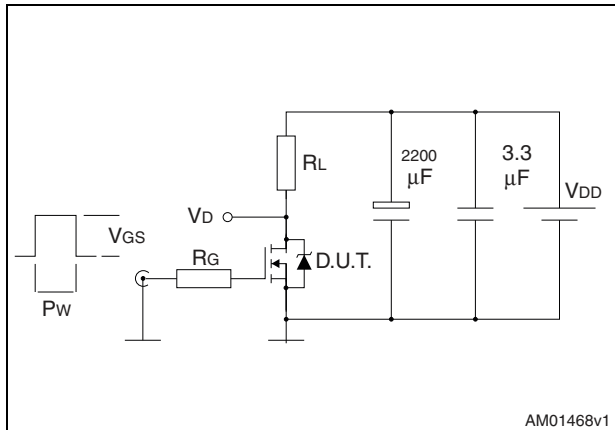


Figure 18. Gate charge test circuit

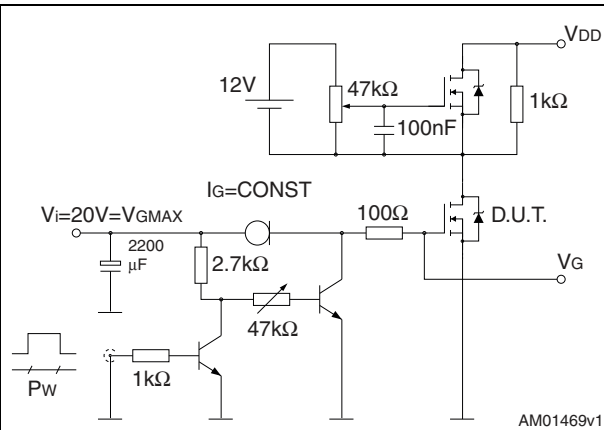


Figure 19. Test circuit for inductive load switching and diode recovery times

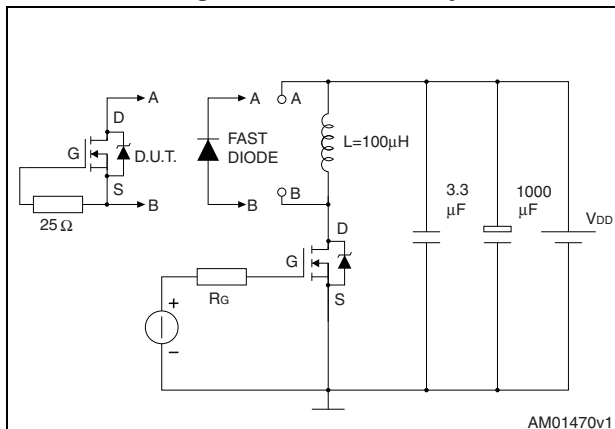


Figure 20. Unclamped inductive load test circuit

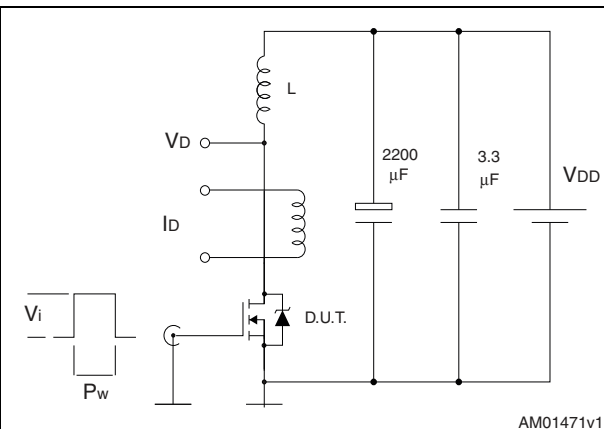


Figure 21. Unclamped inductive waveform

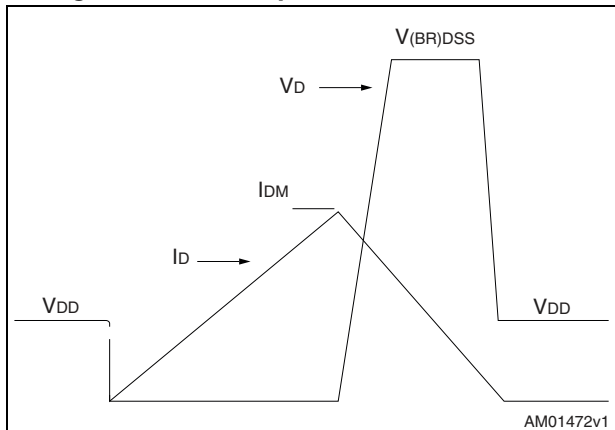
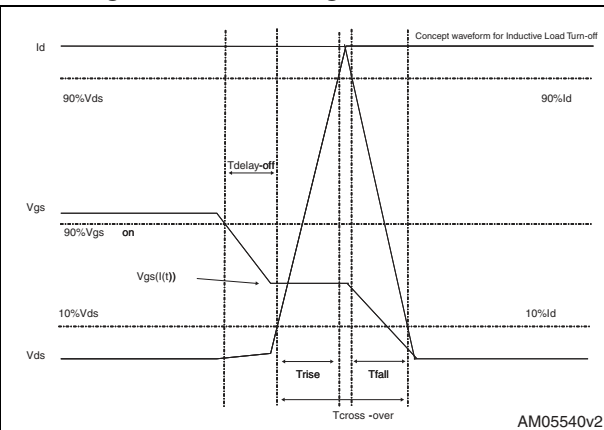


Figure 22. Switching time waveform



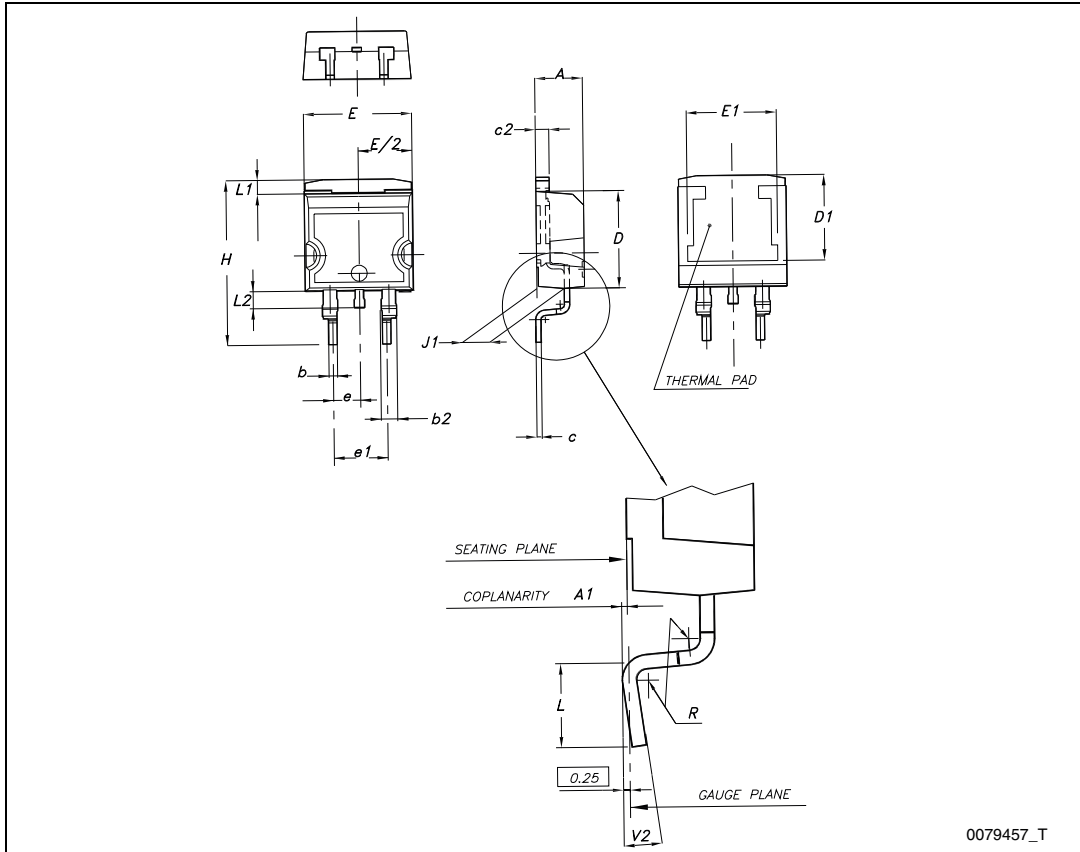
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

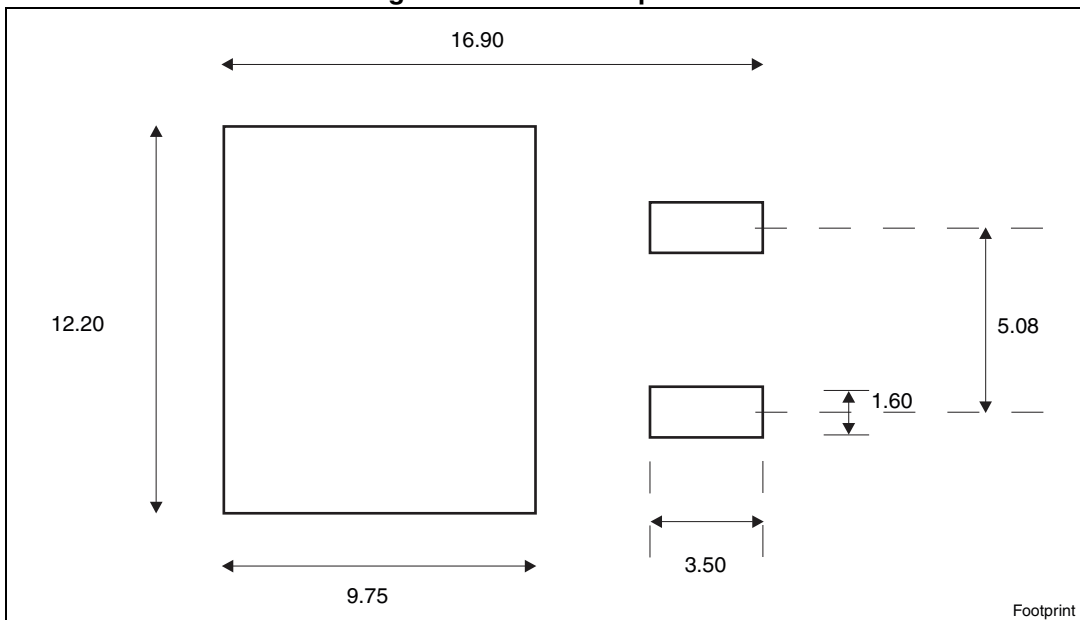
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D<sup>2</sup>PAK (TO-263) drawing



0079457\_T

Figure 24. D<sup>2</sup>PAK footprint<sup>(a)</sup>

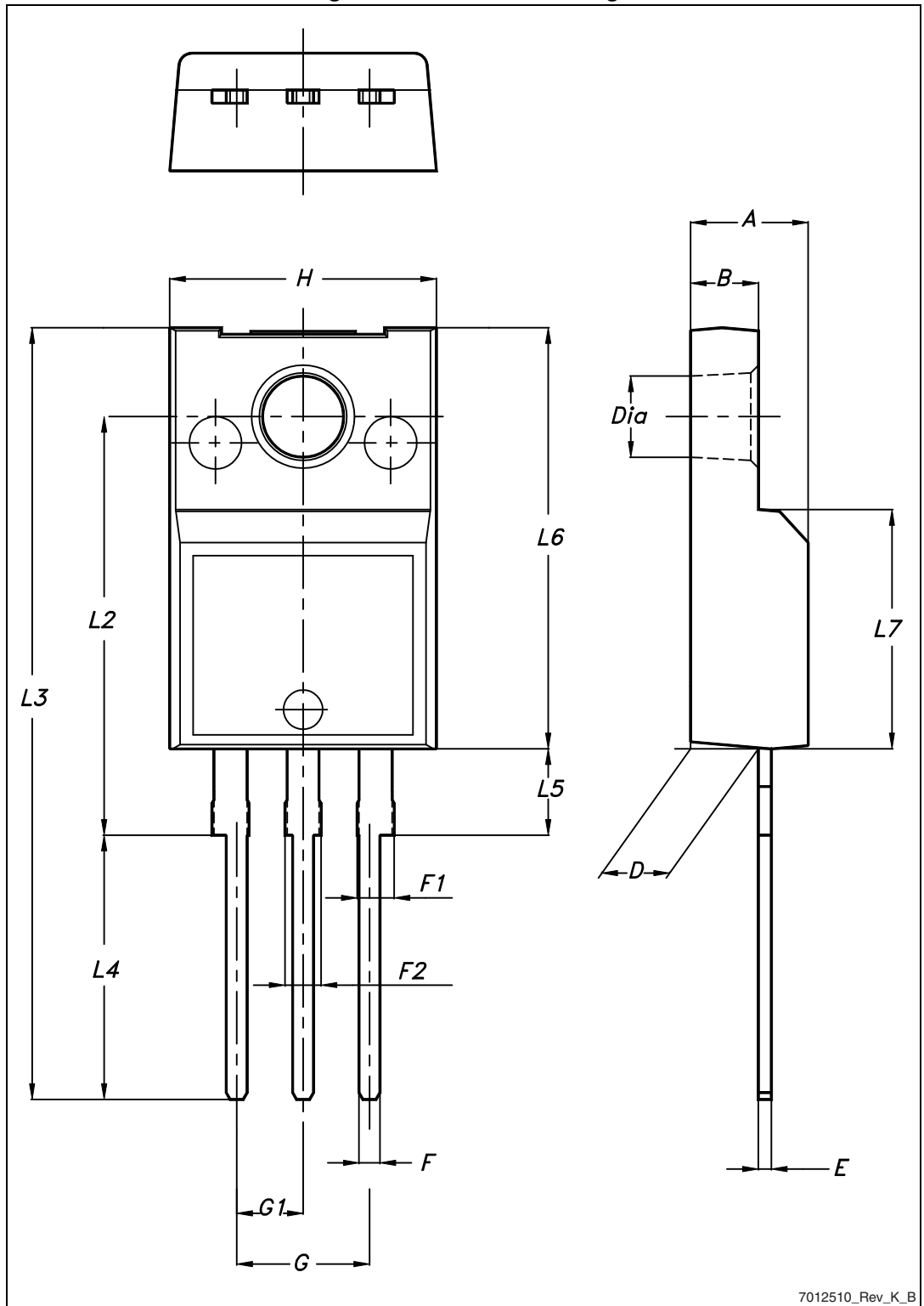


a. All dimensions are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing

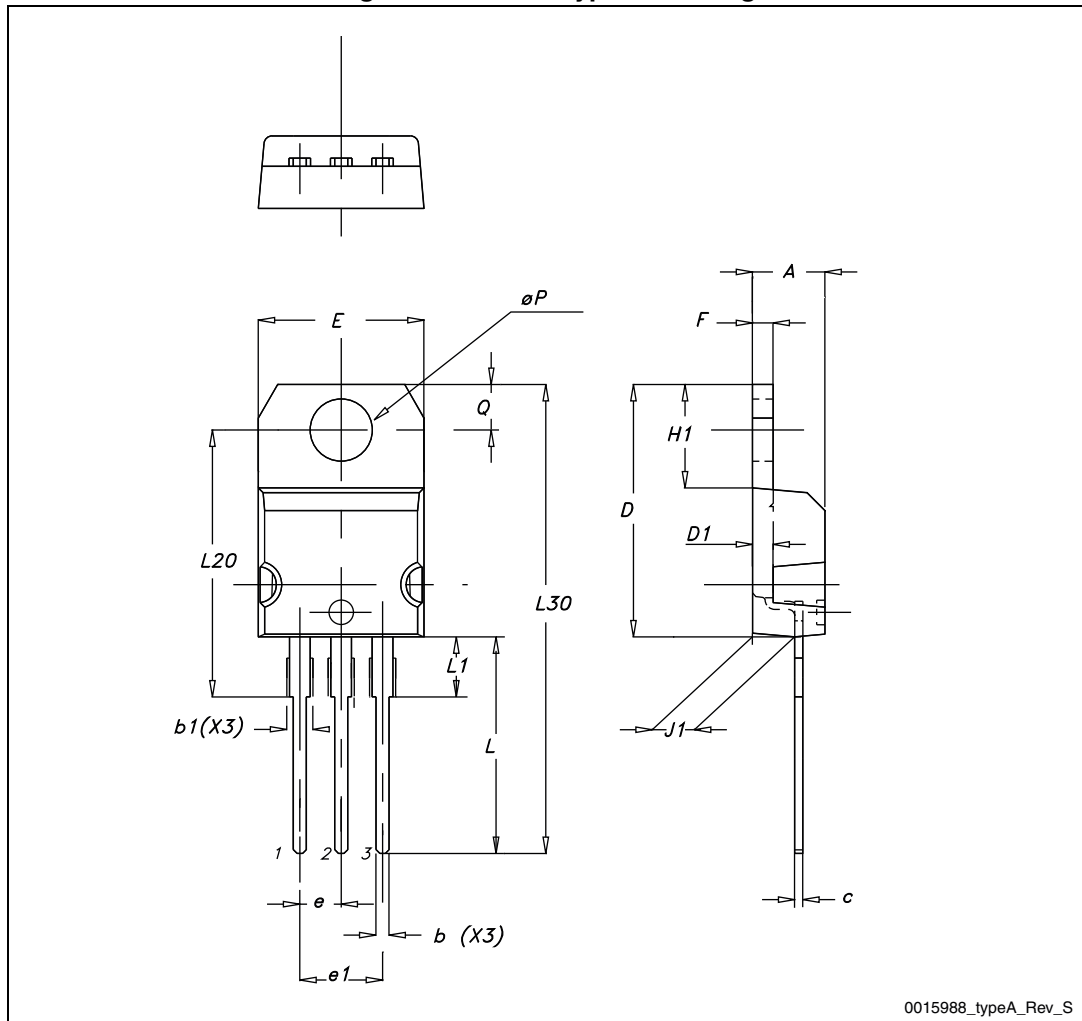


7012510\_Rev\_K\_B

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing



0015988\_typeA\_Rev\_S



## 5 Packaging mechanical data

Table 12. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 27. Tape for D<sup>2</sup>PAK (TO-263)

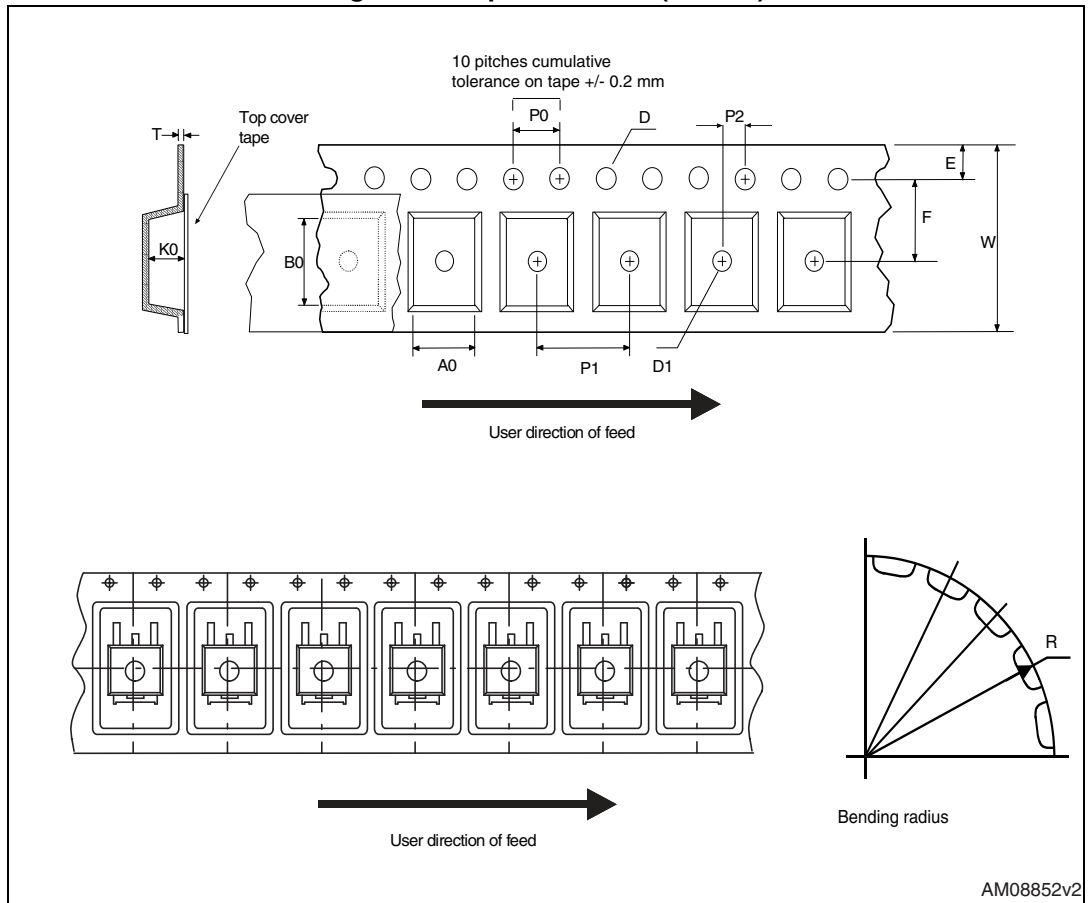
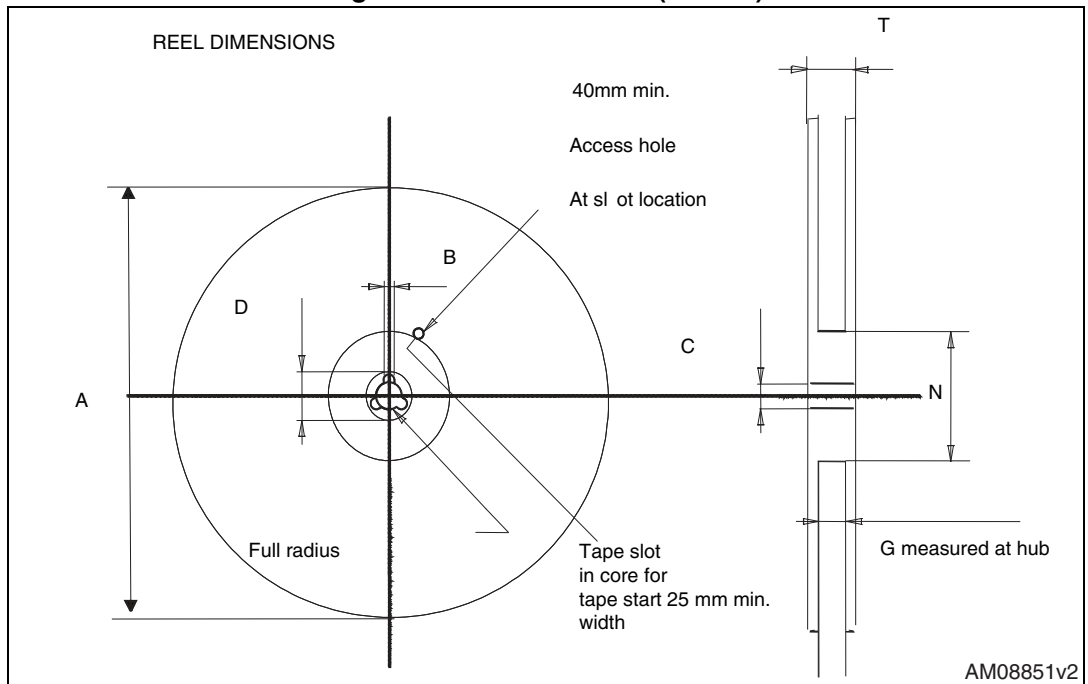


Figure 28. Reel for D<sup>2</sup>PAK (TO-263)



## 6 Revision history

Table 13. Document revision history

Date	Revision	Changes
22-Feb-2012	1	First release.
28-Aug-2012	2	Document status promoted from preliminary data to production data. Inserted <a href="#">Section 2.1: Electrical characteristics (curves)</a> .
05-Dec-2012	3	The part number STW45N65M5 has been moved to a separate datasheet.
05-Mar-2013	4	– Added dv/dt value on <a href="#">Table 2: Absolute maximum ratings</a> – Minor text changes

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