QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS Bus Interface 18-Bit Universal Register in QVSOP™

FEATURES/BENEFITS

- Function compatible to the 74F823, 74FCT823 and 74FCT823T
- CMOS power levels: <15mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 48-pin 0.4mm pitch QVSOP (Q1)
- A speed grades with 10.0ns
- I_{OL} = 48mA Ind.

DESCRIPTION

The QS74FCT2X823T is an 18-bit high-speed CMOS TTL-compatible buffered register with three-state outputs that is ideal for driving high capacitance loads such as memory and address buses. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

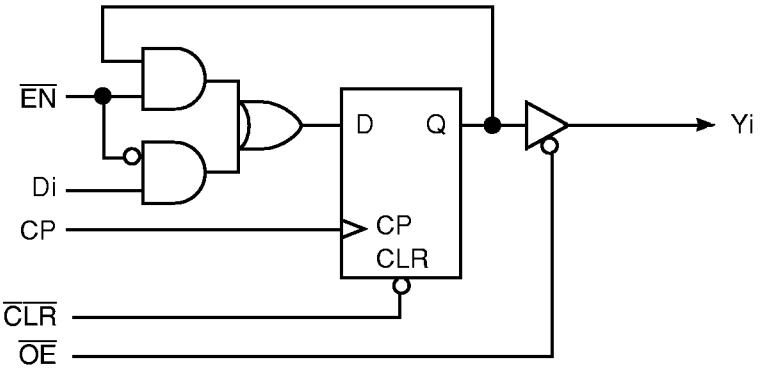

Figure 2. Pin Configurations

(All Pins Top View)

QVSOP

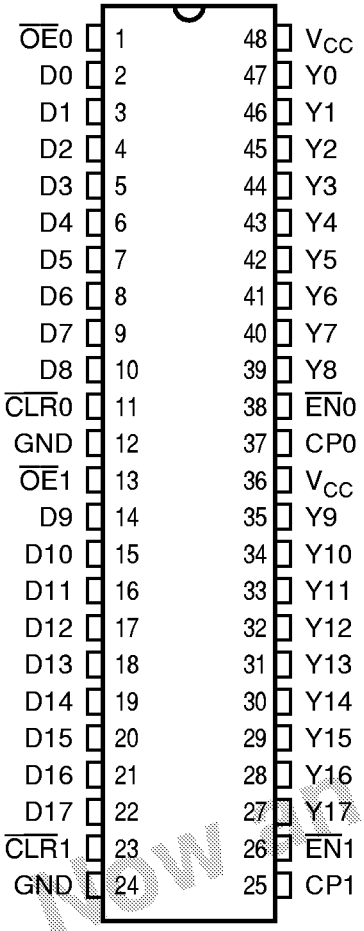

Table 1. Pin Description

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
CPi	I	Clock Pulse
$\overline{OE}$	I	Output Enable
$\overline{ENi}$	I	Clock Enable
$\overline{CLRi}$	I	Asynchronous Reset

Table 2. Function Table

Inputs					Int.	O/P	
$\overline{OEi}$	$\overline{CLRi}$	$\overline{ENi}$	Di	CPi	Qi	Yi	Function
H	X	L	L	↑	L	Hi-Z	High Z
H	X	L	H	↑	H	Hi-Z	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 4. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	Max	Unit
1-11, 13-23, 25-35, 37-47	8	pF

Note: Capacitance is characterized but not production tested.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., Freq = 0 0V ≤ V_{IN} ≤ 0.2V or V_{CC}-0.2V ≤ V_{IN} ≤ V_{CC}	—	3.0	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH[2]	V_{CC} = Max., V_{IN} = 3.4V, Freq = 0	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz[3,4]	V_{CC} = Max., Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{CC}	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 6. DC Electrical Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current(2,3)	V_{CC} = Max., V_{OUT} = GND	–60	—	—	mA
V_{IC}	Input Clamp Voltage(3)	V_{CC} = Min., I_{IN} = –18 mA	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –24 mA (COM)	2.4	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12 mA (COM)	—	—	0.50	

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

Table 7. Switching Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±5%,
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	2X823A		2X2823C		Unit
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Clock to Y Delay $\overline{OE}$ = LOW		10		6.0	ns
t_{PHL} t_{PLH}	Clock to Y Delay[2,3] $\overline{OE}$ = LOW		20		12.5	ns
t_S	Data to CP Setup Time	4.0		3.0		ns
t_H	Data to CP Hold Time	2.0		1.5		ns
t_{ENS}	$\overline{EN}$ to CP Setup Time	4.0		3.0		ns
t_{ENH}	$\overline{EN}$ to CP Hold Time	2.0		0.0		ns
t_{CLR}	$\overline{CLR}$ to Y Delay		11		8.0	ns
t_{REC}	$\overline{CLR}$ to CP Setup Time	6.0		6.0		ns
t_{PWH} t_{PWL}	Clock Pulse Width[2] HIGH or LOW	7.0		6.0		ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi		12		7.0	ns
t_{PZH} t_{PZL}	Output Enable Time[2,3] $\overline{OE}$ to Yi		23		12.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2,4] $\overline{OE}$ to Yi		7.0		6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2] $\overline{OE}$ to Yi		9.0		6.5	ns

Notes:
1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. C_{LOAD} = 300pF
4. C_{LOAD} = 5pF