

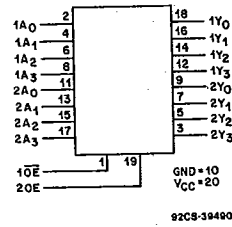
HARRIS SEMICONDUCTOR

CD54AC241/3A
CD54ACT241/3A

T-52-07

The RCA CD54AC241/3A and CD54ACT241/3A are 3-state octal buffer/line drivers that utilize the new RCA ADVANCED CMOS LOGIC technology. These devices have one active-LOW ($\overline{1OE}$) and one active-HIGH (2OE) output enable.

The CD54AC241/3A and CD54ACT241/3A are supplied in 20-lead dual-in-line ceramic packages (F suffix).



Package Specifications

See Section 11, Fig. 13

FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			+25		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} $V_O = V_{CC}$ or GND	5.5	—	±0.5•	—	±10•	μA
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	—	8•	—	160•	μA

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The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
nA0 - A3	0.5
$\overline{1OE}$	0.83
2OE	1.67

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT241	3,5,7,9,12 14,16,18	1,2,4,6,8,10,11,13, 15,17	19,20	3,5,7,9,12, 14,16,18	1,10	2,4,6,8,11,13,15 17,19,20
Dynamic	OPEN	GROUND	$1/2 V_{CC}$ (3V)	V_{CC} (6V)	OSCILLATOR	
CD54AC/ACT241	1,10	3,5,7,9,12,14, 16,18	19,20	2,4,6,8,11, 13,15,17	50 kHz	25 kHz

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC241/3A
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SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays Data to Outputs	t_{PLH}	1.5	—	120	ns
	t_{PHL}	3.3*	3.8	16.8	
Output Enable and Disable Times	t_{PLZ}	1.5	—	167	ns
	t_{PZL}	3.3	3.8	23.4	
	t_{PZH}	5	2.4	13.4*	
	t_{PHZ}	5	2.4	13.4*	
Power Dissipation Capacitance	$C_{PD}\S$	—	95 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C		V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C		V
Input Capacitance	C_i	—	—	10	pF
3-State Output Capacitance	C_o	—	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays Data to Outputs	t_{PLH}	5†	1.8	10.6*	ns
	t_{PHL}	5†	1.8	10.6*	
Output Enable and Disable Times	t_{PLZ}	5	2.5	14.4*	ns
	t_{PZL}	5	2.5	14.4*	
	t_{PZH}	5	2.5	14.4*	
	t_{PHZ}	5	2.5	14.4*	
Power Dissipation Capacitance	$C_{PD}\S$	—	115 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C		V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C		V
Input Capacitance	C_i	—	—	10	pF
3-State Output Capacitance	C_o	—	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption per package.

For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

(Limits with black dots (*) are tested 100%.)