Am2925A

Clock Generator and Microcycle Length Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Crystal controlled oscillator**
  - Stable operation from 1-50 MHz
- **TTL controlled oscillator**
  - Stable operation from 1-60 MHz
- **Four microcode controlled clock outputs**
  Allows clock cycle length control for 15–30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length.
- **System controls for $\overline{\text{Run}}/\overline{\text{Halt}}$ and Single Step**
  Switch debounced inputs provide flexible halt controls
- **Slim 0.3" 24-pin package**
  LSI complexity in minimum board area

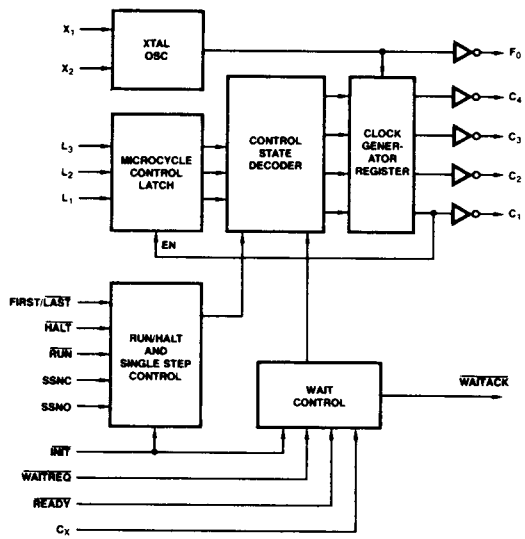
GENERAL DESCRIPTION

The Am2925A is a single-chip general purpose clock generator/driver. It is crystal controlled, and has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meet a variety of system speed requirements. The Am2925A generates four different simultaneous clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. One-of-eight cycle lengths may be generated under microprogram control using the Cycle Length inputs L_1, L_2, and L_3.

The Am2925A oscillator runs at frequencies up to 50 MHz crystal input or 60 MHz TTL input. A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs C_1, C_2, C_3 and C_4.

System control functions include Run, Halt, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/$\overline{\text{LAST}}$ input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. $\overline{\text{WAITACK}}$ indicates that the Am2925A is in a wait state.

BLOCK DIAGRAM



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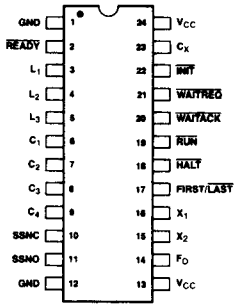
CONNECTION DIAGRAMS
Top View



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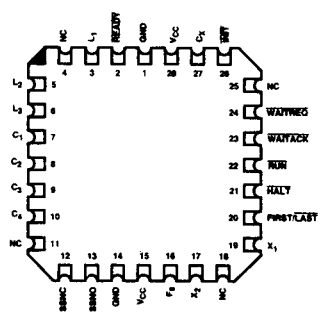

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Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM2925 A D C —

E. OPTIONAL PROCESSING
Blank = Standard Processing

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
D = 24-Pin SLIM Ceramic DIP (CD3024)
L = 28-Pin Ceramic Leadless Chip Carrier (CLT028)
X = Dice

B. SPEED OPTION
A = 60 MHz

A. DEVICE NUMBER/DESCRIPTION
Am2925A
Clock Generator and Microcycle Length Controller

Valid Combinations	
AM2925A	DC, LC, XC

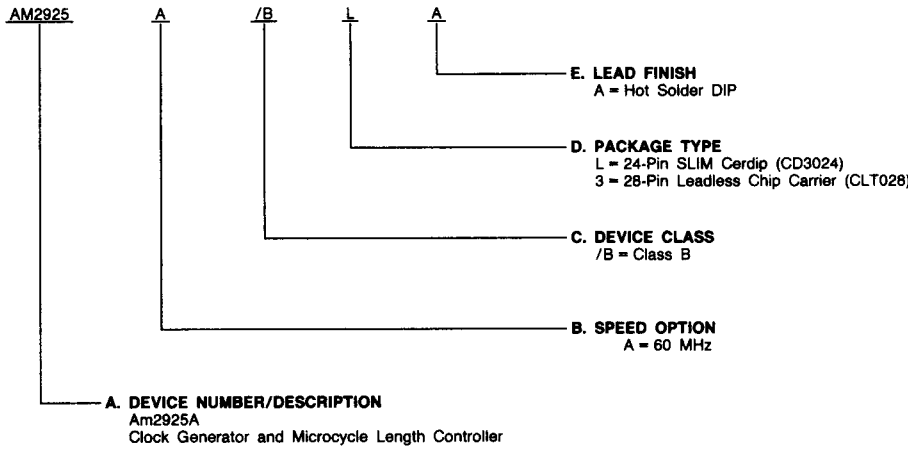
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

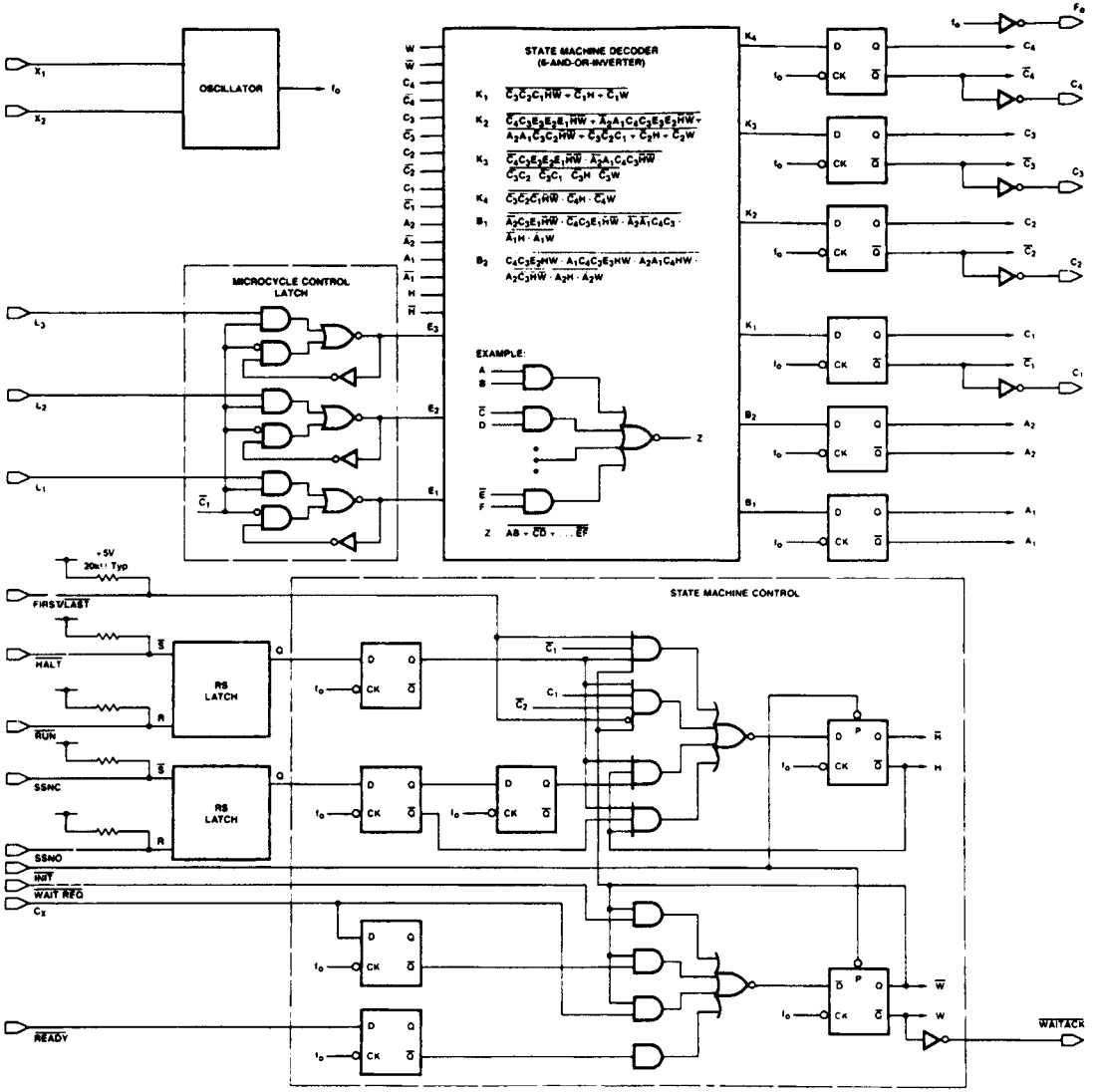


Valid Combinations	
AM2925A	/BLA, /B3A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Am2925A LOGIC DIAGRAM



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PIN DESCRIPTION

$C_1 - C_4$ System Clock Outputs (Outputs)
These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls, L_1, L_2, and L_3.

$L_1 - L_3$ Clock Cycle Length Control Inputs (Inputs)
These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.

F_0 Buffered Oscillator Output (Output)
F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{WAITACK}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.

$\overline{HALT}$, $\overline{RUN}$ Debounce Inputs (Inputs)
These inputs determine whether the output clocks run or not. A LOW input on $\overline{HALT}$ ($\overline{RUN}$ = HIGH) will stop all clock outputs.

FIRST/$\overline{LAST}$ $\overline{HALT}$ Time Control Input (Input)
A HIGH input in conjunction with a $\overline{HALT}$ command a will cause halt to occur when C_4 = LOW and $C_1 = C_2 = C_3$ = HIGH (see Clock Waveforms). A LOW input causes a $\overline{HALT}$ to occur when $C_1 = C_2 = C_3$ = LOW and C_4 = HIGH.

SSNO, SSNC Single-Step Control Inputs (Inputs)
These debounced inputs allow system clock cycle single stepping while $\overline{HALT}$ is activated LOW.

$\overline{WAITREQ}$ $\overline{WAIT\ REQUEST}$ (Input)
When LOW this input will cause the outputs to halt during the next oscillator cycle after the C_X input goes LOW.

C_X Wait Cycle Control Input (Input)
The clock outputs respond to a wait request one oscillator clock cycle after C_X goes LOW. C_X is normally tied to any one of C_1, C_2, C_3 or C_4.

$\overline{WAITACK}$ $\overline{WAIT\ ACKNOWLEDGE}$ (Output)
When LOW, this output indicates that all clock outputs are in the "WAIT" state.

$\overline{READY}$ $\overline{READY}$ (Input)
The $\overline{READY}$ active LOW input is used to continue normal clock output patterns after a wait stage.

$\overline{INIT}$ $\overline{INITIALIZE}$ (Input)
This input is intended for use during power-up initialization of the system. When LOW all clock outputs free run regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.

X_1, X_2 External Crystal Connections (Input/Output)
X_1 can also be driven by a TTL frequency source.

FUNCTIONAL DESCRIPTION

The Am2925A is a dynamically programmable general-purpose clock generator/driver. It can be logically separated into three parts. There is an oscillator, a state machine decoder and a state machine control section.

The oscillator is a linear inverting amplifier which may be configured with a minimum of external parts as a 1st harmonic* crystal oscillator, 3rd harmonic* crystal oscillator, L-C oscillator or used to buffer an external clock. The buffered, inverted output of this oscillator is available as F_0.

The state machine takes microcode information from the Microcycle Length "L" inputs L_1, L_2 and L_3 and counts the fundamental frequency of the internal oscillator, F_0, to create the clock outputs, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle, and C_4 is always LOW on the first. C_3 has an approximately 50% duty cycle, and C_2 is HIGH for all but the last two periods.

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into a set of combinatorial logic to generate the next state. On each falling edge of the internal clock, the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle ($C_1 = C_2 = C_3$ = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the Am2925A comprised of Run, Halt, Wait and Single Step.

System Timing

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The Am2925A allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

This section will cover several aspects of the Am2925A. The first topic to be covered is the oscillator section which is responsible for providing the basis of all system timing. Second will be how to operate the Am2925A; last will be an example of an Am2925A in a 16-bit microprogrammed machine.

*It is understood that the terms "fundamental mode" and "3rd overtone" are generally regarded as more technically correct, but "1st harmonic" and "3rd harmonic" are used here because of their more generally accepted usage.

Oscillator

The Am2925A contains an inverting, linear amplifier which is intended to form the basis of a crystal oscillator. In designing this oscillator it is necessary to consider several factors related to the application.

The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the Am2925A is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystals are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO). For extreme temperature stability, an oven must be used or some other form of temperature compensation applied.

Absolute frequency accuracy must also be considered. The resonant frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32 pF), or to specify the load when ordering a special crystal. It should then be possible to determine from the crystal characteristics the load tolerance to maintain a given accuracy. If the "set-on" error due to load tolerance is unacceptable, a trimmer capacitor should be incorporated for fine adjustment.

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained crystal oscillators operate at their fundamental frequency. However, crystals are not generally available with fundamental frequencies above 20-25 MHz. At higher frequencies, an overtone oscillator must be used. In this case, the crystal is designed to oscillate efficiently at one of its odd harmonic frequencies and additional components are included in the oscillator circuit to prevent it oscillating at lower harmonics.

Where a high degree of accuracy or stability is not required, the amplifier may be configured as an L-C oscillator. It may also be driven from an external clock source if operation is required in synchronous with that source.

1st Harmonic (Fundamental) Oscillator

The circuit of a typical 1st harmonic oscillator is shown in Figure 1. The crystal load is comprised of the two 68 pF capacitors in series. This 34 pF approximates the standard 32 pF crystal load. If a closer match is required then one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer. The nominal value of the combination should be 60 pF to provide proper crystal loading.

A typical crystal specification for use in this circuit is:

Frequency Range: 5–20 MHz
Resonance: Parallel Mode
Load: 32 pF
Stability: .01% or to match systems requirements
Case: H-17 — for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change over temperature.

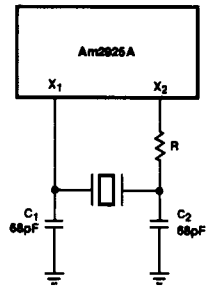

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Figure 1. Connections for 5–20 MHz

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.

Note: At fundamental frequencies below 5 MHz it is possible for the oscillator to operate at the 3rd harmonic. To prevent this a resistor should be added in series with the X_2 pin as shown in the circuit diagram.

The resistor value should match the impedance of C_2:

$$R = X_{C_2} = \frac{1}{2\pi f C_2}$$

3rd Harmonic Oscillator

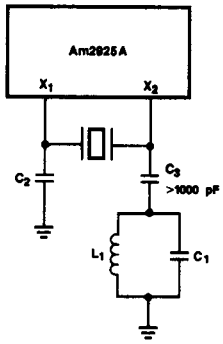
At frequencies greater than 20 MHz, the crystal can be operated at its 3rd harmonic. A typical circuit is shown in Figure 2. Two additional components are included; an inductor, L_1, and a capacitor, C_3. The purpose of the capacitor is to block the d.c. path through the inductor and thereby maintain the correct amplifier bias. C_3 should be large ($\geq$ 1000 pF).

The inductor forms a parallel tuned circuit with C_1. This circuit has its resonance set between the 1st and 3rd harmonics of the crystal and is used to prevent the oscillator operating at the 1st harmonic. In the 1st harmonic oscillator (Figure 1), the crystal appears as an inductor and forms a π-network with the two capacitors, thus providing the necessary phase shift for oscillation. In the 3rd harmonic oscillator, L_1 and C_1 are chosen such that at the 3rd harmonic the impedance of circuit is equivalent to that of the capacitor C_2 in the 1st harmonic oscillator (Figure 3b). Thus, the same π-network is formed (Figure 3c) and oscillation is possible. At the 1st harmonic the tuned circuit appears as an inductor (Figure 3a), the π-network is not formed and oscillation is not possible.

The following specification is typical for a crystal to be used in a 3rd harmonic oscillator.

Frequency Range: Above 20 MHz
Resonance: Parallel Mode
Load: 32 pF
Stability: .01% or to match systems requirements
Case: H-17 — for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change over temperature.

Again it is good practice to ground the crystal case and keep connections short.



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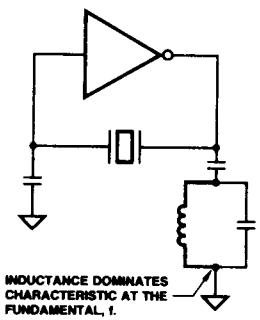
C_1	C_2	L	f_0 (Max.)
68	82	$\frac{1150}{F_0{}^2}$	20-27
33	45	$\frac{2079}{F_0{}^2}$	27-48
18	25	$\frac{3800}{F_0{}^2}$	48-54

Units:
C_1, C_2 = pF; L = μH; f_0 = MHz

Figure 2. Connections for Frequencies above 20 MHz



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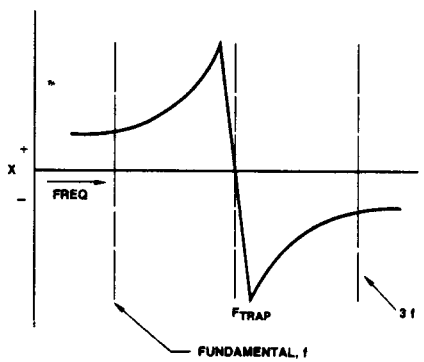
a) Fundamental Equivalent



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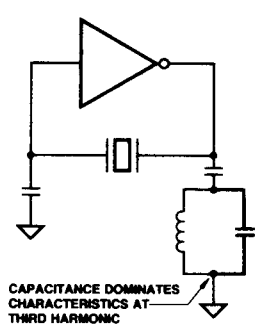
b) Trap Impedance



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c) 3rd Harmonic Equivalent

Figure 3. Forcing Third Harmonic Oscillation

Design Procedure

(1) Assume C_1 = 82 pF and C_2 = 68 pF (this gives a sensible inductor value). L_1 is calculated according to the formula:

$$L_1 = \frac{1151}{f_o^2}$$

f_o = Operating frefquency in MHz
L_1 in μH

This sets the resonant frequency of the L-C combination at 0.52 f_o.

(2) Select the closest standard value inductor for L_1. Using this value calculate C_1 such that the resulting crystal load at the 3rd harmonic is 32 pF.

$$C_1 = 60 + \frac{25330}{L_1 \cdot f_o^2} \qquad C_1 \text{ in pF.}$$

Choose the closest standard capacitor value to this.

Using standard values both the resonant frequency of the L-C circuit (f_r) and the crystal load are non-optimal. This will cause a slight error in the oscillating frequency. If this is not permissible, C_1 may be a fixed capacitor in parallel with a trimmer such that the range of adjustment includes the calculated value for C_1. This is then set to give the desired frequency. In either case the approximate inductor value will cause the resonant frequency to the L-C circuit to change. This frequency, f_r, may be computed and should remain approximately midway between the 1st and 3rd harmonic.

$$f_r = \frac{159}{\sqrt{L_1 C_1}}$$

f_r in MHZ
L_1 in μH
C_1 in pF

L-C Oscillator

The Am2925A can be operated as an L-C tuned oscillator (Figure 4) and will perform as a stable oscillator within the restrictions of the chosen frequency determining components (i.e., inductor and capacitors). The circuit chosen is a classical π-network with DC loop isolation. The Am2925A oscillator is a DC biased linear amplifier. This DC bias is necessary and therefore C_3 is included to block the DC path through the inductor. If a variable slug tuned inductor is used, a moderate range of frequency adjustment tuneability (approximately 2:1) can be achieved. The range can be enhanced by switching the two resonant capacitors (C_1, C_2) to larger or smaller values. The specific frequency of operation can be determined by the formula:

$$f = \frac{1}{2\pi\sqrt{LC}}$$ (where C is C_1 and C_2 in series).

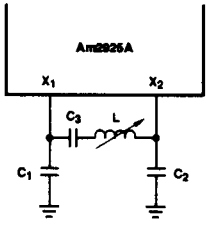

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Figure 4. L-C Tuned Oscillator

External Clock Drive

The Am2925A can be driven by an external TTL clock signal. This is accomplished by directly coupling the TTL clock signal into X_1, the oscillator input. The X_2 pin is an output and should be left unloaded in this configuration.

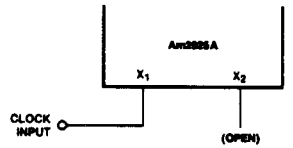

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Figure 5. External Clock Drive

Am2925A Control Inputs

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which are intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch. The Microcycle Latch performs the function of a pipeline register for the microcycle length microcode bits. Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 6). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{\text{LAST}}$ input is used to determine at what point of the microcycle the Am2925A will halt when $\overline{\text{HALT}}$ or a SINGLE STEP is initiated. In most applications the user wires this input HIGH or LOW depending on his design.

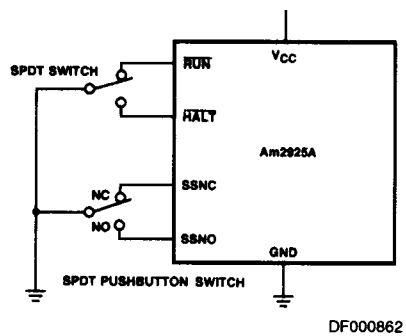

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Figure 6. Switch Connection for $\overline{\text{RUN}}$/$\overline{\text{HALT}}$ and Single Step

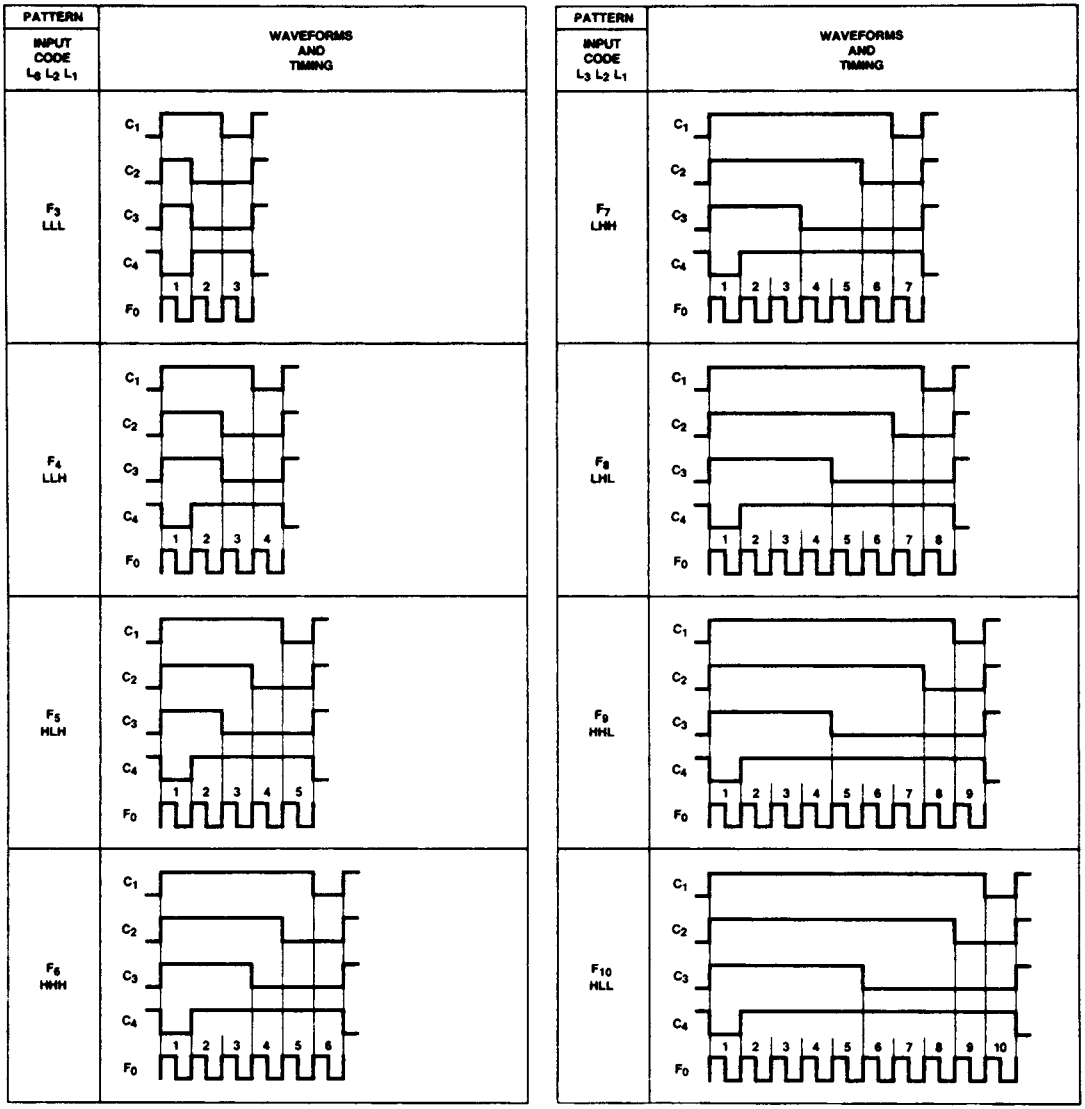

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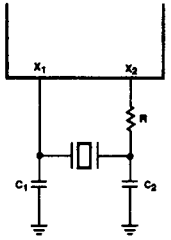
Figure 7. Am2925A Clock Waveforms



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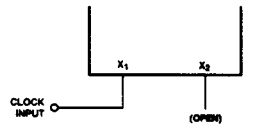
$$R = X_{C_2} = \frac{1}{Tf_{C_2}} \text{ for } 1-6 \text{ MHz}$$

$R = 0$ for 6 – 20 MHz

a) Fundamental Oscillator



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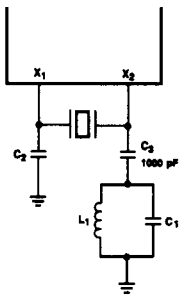
b) External Clock Drive

C_1	C_2	L	f_0 (Max.)
68	82	$\frac{1150}{F_0{}^2}$	20-27
33	45	$\frac{2079}{F_0{}^2}$	27-48
18	25	$\frac{3800}{F_0{}^2}$	48-54

Units:
C_1, C_2 = pF; L = μH; f_0 = MHz



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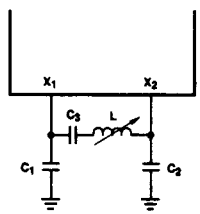
($f_0 \geq 20$ MHz)

c) 3rd Harmonic Oscillator



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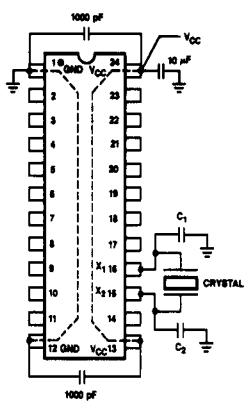
$$f_0 = \frac{1}{2\pi\sqrt{2LC}}$$

$C_1 = C_2 = C$

$X_{C_3} < X_L$

d) L-C Oscillator



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e) Typical External Connections

Design Considerations

1. Oscillator external connections should be less than 1" long — wirewrap is not recommended.
2. V_{CC} and GND connections should be less than ½" long to power plane.
3. Supply decoupling includes both high frequency and bulk storage elements.
4. The same considerations apply for 3rd overtone configurations.

Figure 8. Am2925A Oscillator Applications

(External Component Calculations Summary)

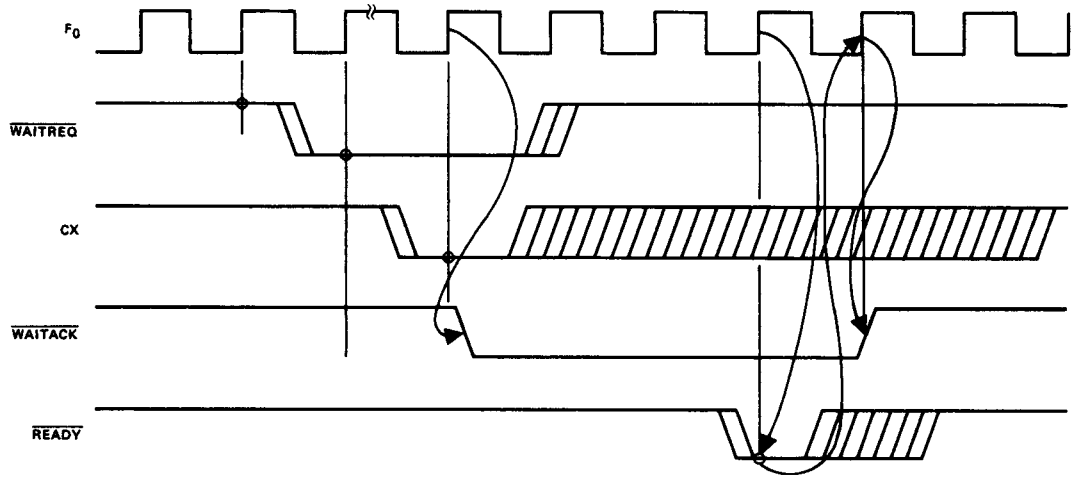


Figure 9. Am2925A WAIT/READY Timing

When HALT is held LOW (RUN = HIGH), the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/LAST input. When RUN goes LOW (HALT = HIGH), the state machine will resume the run mode.

The WAITREQ, C_X, READY and WAITACK signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the data bus for several microseconds in which case the peripheral pulls the WAITREQ line LOW. The C_X input lets the designer specify when the WAITREQ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to respond in order to request a wait cycle (see Figure 9). The READY line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The WAITACK line goes LOW on the next oscillator cycle after the C_X input goes LOW and remains LOW until the second oscillator cycle after READY goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been LOW for one clock edge, the state machine will change to the run mode. The microcycle will end on the first or last state of the microcycle depending on the state of the FIRST/LAST.

AC Timing Signal References

Set-up and hold times in registers and latches are measured relative to the clock signals that drive them. In the Am2925A, the crystal oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference for set-up, hold and clock to output times. However for the Microcontrol Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcontrol Latch because in a typical application this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.

Clock Outputs

There are four clock outputs provided for the user which have different duty cycles. The user must make a decision as to which one best fits his purposes. For example, in a three-address architecture, with the Am2903A (Figure 10), the C_3 clock (approximately 50% duty cycle) could be used to drive the clock input while C_2 (always LOW last two oscillator cycles) drives Instruction Enable. This guarantees, for microcycle lengths greater than four, that the internal RAM data latches of the Am2903A are closed and the destination address is multiplexed onto the B address bus before the RAM begins the Write cycle (Figure 11).

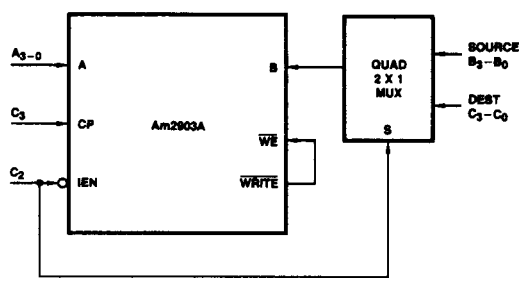


Figure 10. Am2903A Three-Address Architecture

APPLICATIONS

16-Bit Machine with Am2925A

The block diagram in Figure 12 shows a 16-bit microprogrammed machine which uses an Am2925A to generate system timing. The design decisions include oscillator frequency and clock pattern selections.

Selecting the Crystal

In order to pick the oscillator frequency, a detailed timing analysis of the machine must be done in order to determine the execution length of every operation to be performed. For each operation there will be several delay paths, which usually include the ALU and the microprogram control.

Table 1 is an example of two of these paths. PATH 1 is a path through the Am2910A (Figure 12) for a microprogram Conditional Jump Subroutine. PATH 2 is a data flow path through the Am2903A for an Add instruction. Therefore, if the operation were an Add with a Conditional Jump Subroutine the maximum delay would be 170 ns. If there were a Program Control Unit also, then delays through it would have to be considered.

After the execution times all of the instruction types have been calculated, the oscillator frequency can be selected. It is desirable to minimize the difference between the most commonly used instructions and multiples of the oscillator period. In this way the most efficient use can be made of the variable microcycle scheme.

For example, in the hypothetical machine in Figure 12 there are four instruction types (most machines will have more). Table 2 is a table which lists each instruction type, corresponding execution time, and anticipated percentage of the typical instruction stream for each instruction. Several possible frequencies are shown which contain the next highest multiple of the corresponding oscillator period for each instruction. 50 MHz is the best choice because it comes closest to matching instructions A and C which compose 90% of the typical instruction stream.

Fixed Bandwidth Buses

For those designs that require a data bus with fixed bandwidth and fixed time slots for each memory access, the designer should consider using cycle lengths which are a multiple of the shortest cycle length, i.e., cycle lengths 3, 6 and 9 or cycle lengths 4 and 8.

The design could further require that the bus be accessed only during the shortest cycle length. Therefore, by using multiple cycle lengths it can be predicted when the CPU will access the bus and for how long, thereby maintaining the fixed bandwidth.

Performance Comparison

Estimated performance can be calculated directly from Table 2. For a fixed microcycle machine the longest instruction execution time would have to be used for all instructions, yielding an average instruction time of 200 ns. With a variable microcycle machine the average instruction time is the sum of the products for each instruction, of the percentage of the instruction stream and the next highest multiple. The average instruction for the example machine with a 50 MHz crystal is:

$(0.6 \times 140 + .08 \times 180 + .3 + 200 + .02 \times 200) = 162.8$ ns

This represents a 19% increase in system performance without requiring any other system speed-ups and without requiring faster devices.

TABLE 1. DELAY PATH TOTALS FOR AN ADD AND A CONDITION JUMP SUBROUTINE

Device No.	Device Path	Path 1	Path 2
Am27S27	CP – Q	27	27
Am2904	INST – CT	58	–
Am2903A	I/AB – GP	–	50
Am2910A	CC – Y	30	–
Am2902A	GP – CN + Z	–	7
Am27S27	TS	55	–
Am2903A	CN – Z	–	35
Am2904	TSZ	–	17
Total	ns	170	136

TABLE 2. INSTRUCTION TIME ANALYSIS

Instruction Type	A	B	C	D	Units
Execution Time	140	180	184	200	ns
Percentage of Instruction Stream	60%	8%	30%	2%	%
Closest Multiple Oscillator Period					
20 MHz P = 50	150 (3P)	200 (4P)	200 (4P)	200 (4P)	ns
25 MHz P = 40	160 (4P)	200 (5P)	200 (5P)	200 (5P)	ns
30 MHz P = 33	167 (5P)	200 (6P)	200 (6P)	200 (6P)	ns
33 MHz P = 30	150 (5P)	180 (6P)	210 (7P)	210 (7P)	ns
40 MHz P = 25	150 (6P)	200 (8P)	200 (8P)	200 (8P)	ns
50 MHz P = 20	140 (7P)	180 (9P)	200 (10P)	200 (10P)	ns

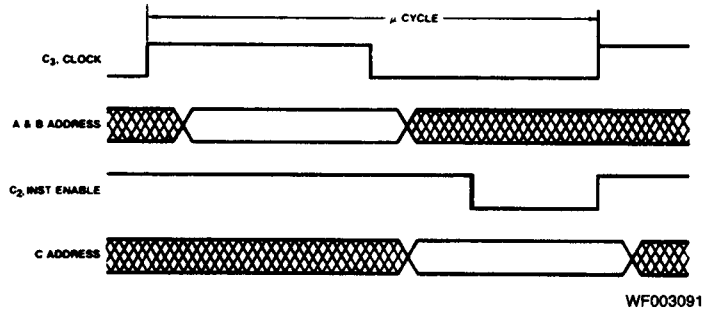


Figure 11. Am2903A Three-Address Operation

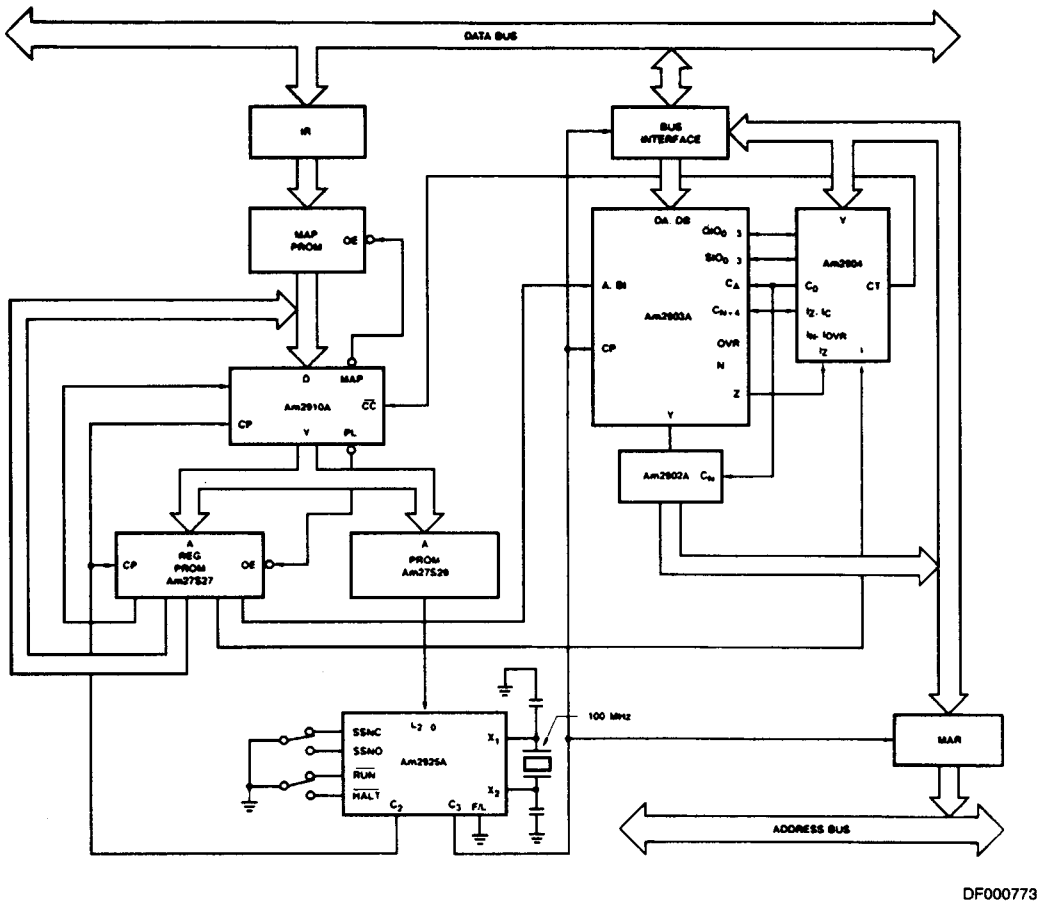


Figure 12. 16-Bit Microprogrammed Machine

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs For
High Output State ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Output Current, Into Outputs ..... 30 mA
DC Input Current ..... −30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Note 1)				Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.0 mA		2.5		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		$\overline{WAITACK}$ C_I	I_{OL} = 4.0 mA		0.4	Volts
					I_{OL} = 8.0 mA		0.45	
					I_{OL} = 12 mA		0.5	
				F_0	I_{OL} = 16 mA		0.5	Volts
V_{IH}	Input HIGH Level (Note 2)	Guaranteed input logical HIGH voltage for all inputs				2.0		Volts
V_{IL}	Input LOW Level (Note 2)	Guaranteed input logical LOW voltage for all inputs			MIL		0.7	Volts
					COM'L		0.8	
V_I	Input Clamp Voltage (Note 2)	V_{CC} = Min., I_{IN} = −18 mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = 0.4 V		$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			−0.4	mA
				$\overline{WAITREQ}$, X_1 (See Figure 13)			−0.8	mA
				SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			−1.0	mA
				C_X			−1.2	mA
				FIRST/$\overline{LAST}$			−1.5	mA
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = 2.7 V		$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			20	μA
				$\overline{WAITREQ}$			50	μA
				SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			−500	μA
				C_X			70	μA
				FIRST/$\overline{LAST}$			−750	μA
				X_1 (See Figure 13)			500	μA
I_I	Input HIGH Current	V_{CC} = Max.	V_{IN} = 5.5 V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			100	μA
			V_{IN} = V_{CC}	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			100	μA
			V_{IN} = 5.5 V	$\overline{WAITREQ}$, C_X			1.0	mA
			V_{IN} = V_{CC}	FIRST/$\overline{LAST}$			1.0	mA
			V_{IN} = 4.0 V	X_1 (See Figure 13)			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = Max.				−30	−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = Max.					120	mA

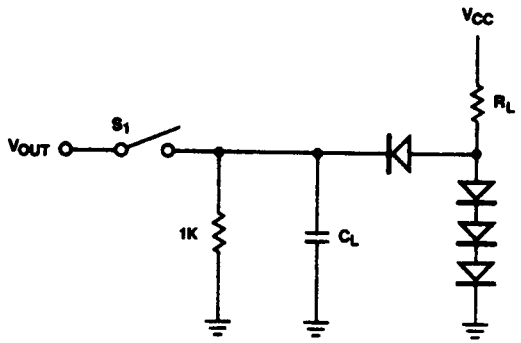
Notes: 1. For conditions shown as Min. or Max. use the appropriate value specified under Operating Ranges for the applicable device type.
2. Does not apply to X_1 and X_2.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} varies with temperature and oscillation frequency as shown in Figure 14. The parameters specified (worst case) apply to f_0 = 0, +25°C, C_1 = C_2 = C_3 = LOW, C_4 = HIGH, X_1 = 2.4 V, X_2 = OPEN and F_0 = LOW. The variations shown in Figure 14 apply to typical values.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

SWITCHING TEST CIRCUITS

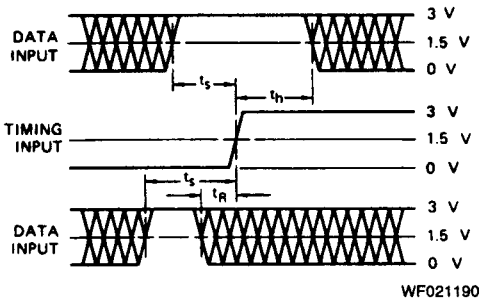


TC003490

Normal Outputs

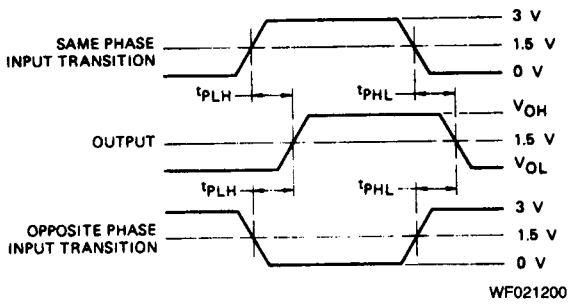
Notes: 1. $C_L = 50$ pF includes scope probe, wiring, and stray capacitances without device in test fixture.
2. S_1 is open during function test and all AC tests, except output enable tests.
3. $C_L = 15$ pF for t_{pd} for X_1 to F_0 tests.
4. Programmable loads are used for automatic testing.

SWITCHING TEST WAVEFORMS

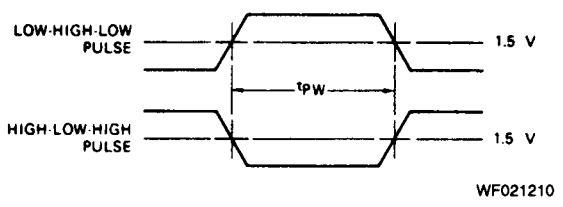


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched are is don't care condition.

Setup, Hold, and Release Times



Propagation Delay



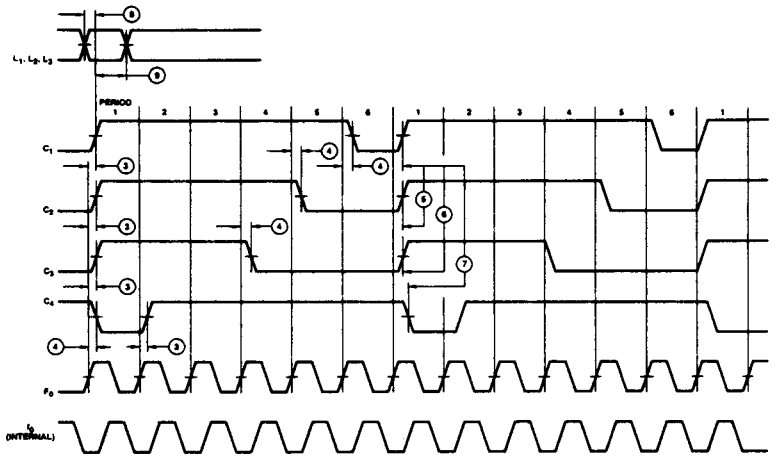
Pulse Width

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

No.	Parameter Symbol	Parameter Description		Test Conditions	Am2925A Min.	Am2925A Max.	Units
1	t_{MAX1}	F_0 Frequency (TTL Input) (Notes 1, 7)	C	C_L = 15 pF R_L = 280 Ω	60		MHz
			M		55		
2	t_{MAX2}	F_0 Frequency (Crystal Input) (Notes 1, 7)	C		50		MHz
			M		45		
3	t_{OFFSET}	F_0(↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)	C M	C_L = 50 pF R_L = 2.0 kΩ		8.5	ns
4	t_{OFFSET}	F_0(↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↑)	C			12	ns
			M				
5	t_{SKEW}	C_1 (↓) to C_2 (↓)	C M			5	ns
6	t_{SKEW}	C_1 (↓) to C_3 (↓)	C M			5	ns
7	t_{SKEW}	C_1 (↓) to C_4 (↑) Opposite Transition	C M			11	ns
8	t_S	L_1, L_2, L_3 to C_1 (↓) (Note 8)	C		15		ns
			M				
9	t_H	L_1, L_2, L_3 to C_1 (↓) (Note 8)	C M		0		n s
10	t_S	C_X to F_0 (↓) (Notes 2, 8)	C M		15		ns
11	t_H	C_X to F_0 (↓) (Notes 2, 8)	C M		0		ns
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Notes 3, 8)	C M		15		ns
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Notes 3, 8)	C M		0		ns
14	t_S	$\overline{READY}$ to F_0 (↓) (Notes 3, 8)	C M		15		ns
15	t_H	$\overline{READY}$ to F_0 (↓) (Notes 3, 8)	C M		0		ns
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↑) to F_0 (↓) (Notes 3, 4, 8)	C M		15		ns
17	t_H	SSNC, SSNO to F_0 (↓) (Notes 3, 4, 8)	C M		15		ns
18	t_S	First/$\overline{LAST}$ to F_0 (↓) (Notes 5, 8)	C		20		ns
			M				
19	t_S	$\overline{INIT}$ (↑) to F_0 (↓) (Notes 3, 8)	C		20		ns
			M				
20	t_{PWL}	$\overline{INIT}$ LOW Pulse Width	C		12		ns
			M				
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$	C			17	ns
			M				
22	t_{PLH}	Propagation Delay (Notes 6, 9) X_1 to F_0	C	C_L = 15 pF R_L = 280 Ω		16	ns
			M				
23	t_{PHL}		C			13	ns
			M				

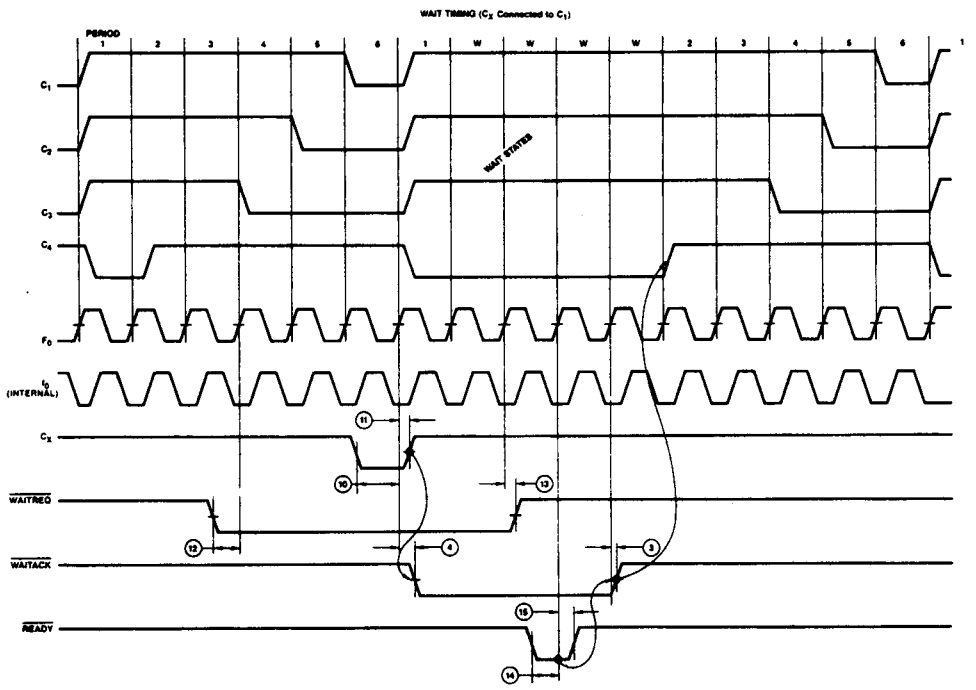
Notes:
1. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or HIGH. The C_X input load must be considered part of the 50 pF/2.0 kΩ clock output loading.
2. These set-up and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW.
3. These inputs are synchronized internally. Failure to meet t_S may cause a $1/F_0$ delay but will not cause incorrect operation.
4. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
5. FIRST/LAST normally wired HIGH or LOW.
6. Reference point of T offset has been moved forward which has increased T offsets.
7. f_{MAX} not tested.
8. Setup and Hold not tested.
9. Tested at 50 pF system load correlated to 15 pF.

SWITCHING WAVEFORMS



WF003070

Normal Cycle Without Wait States (Pattern F_6 Shown)



WF003061

Wait Timing (C_X Connected to C_1)

Am2925A General Test Notes

Automatic tester hardware and handler hardware add additional round trip A.C. delay to test measurements. Actual propagation delay testing may incorporate a correlation factor to negate the additional delay.

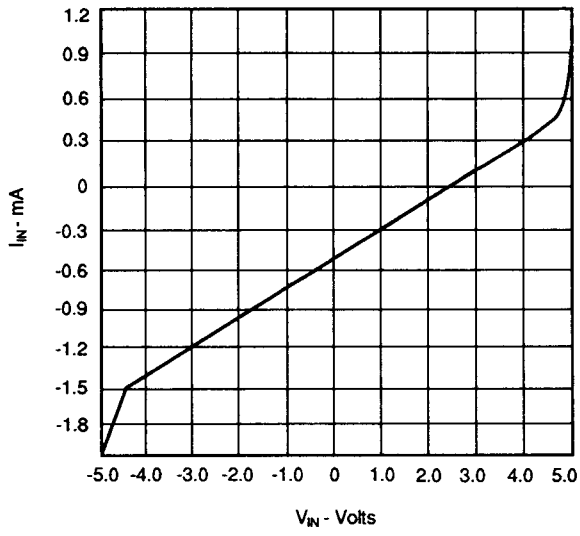
Function testing is done with input LOW less than V_{IL}, and input HIGH greater than V_{IH}. Single trip point at the approximate threshold voltage is used to determine output logic level.

Setup and Hold tests are not performed due to tester accuracy limitation. They are guaranteed by correlation.

T_{PLH} and T_{PHL}, X_1 to F_0, are tested with C_L = 50 pF and are extended limits, rather than 15 pF as specified in the Test Conditions column of the A.C. table. 50 pF is used because it is the minimum test system load. This parameter is guaranteed by correlation to worst-case A.C. parameter.

Programmable loads are used for automatic testing. A.C. loads specified in the datasheet are used for bench testing. Programmable loads, which simulate datasheets loads, are used during production testing.

TYPICAL PERFORMANCE CURVES



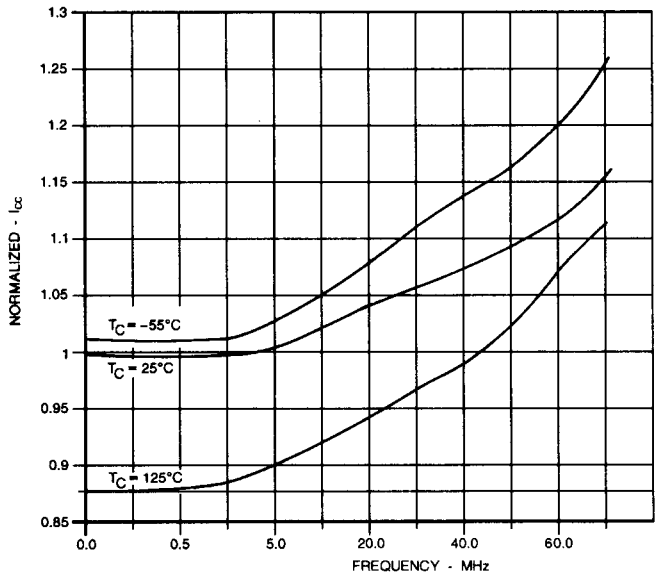
03367-001A

OP002780

X_1 is not a TTL input. It is a crystal connection to an inverting linear oscillator amplifier, and is specified primarily for test convenience.

Figure 13. Am2925A X_1 Input Characteristics (Typical, V_{CC} = 5.0 V)

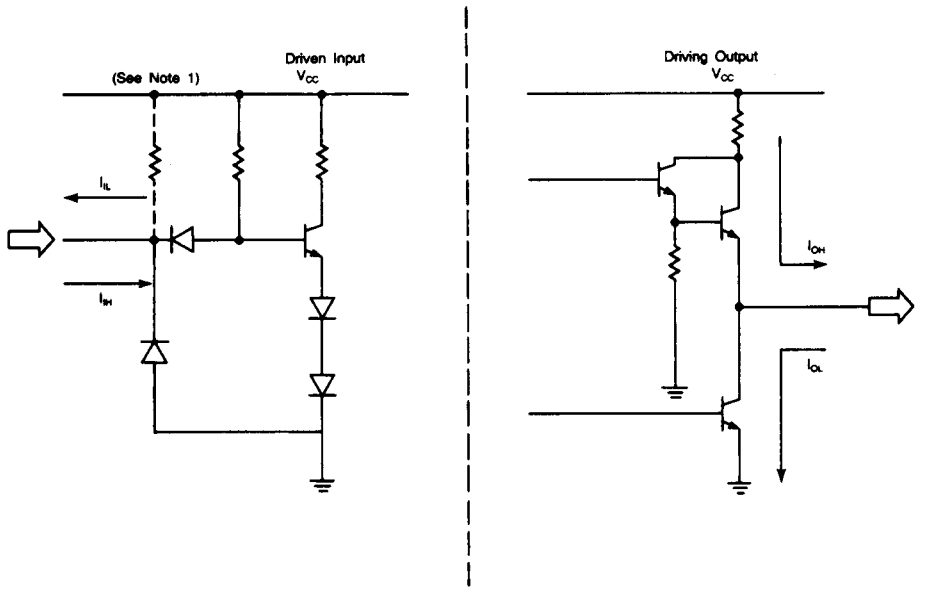
TYPICAL PERFORMANCE CURVES



OP002180

Figure 14. Am2925A I_{CC} Normalized vs Frequency (V_{CC} = 5.5 V)

INPUT/OUTPUT CURRENT DIAGRAM



IC000880

Notes: 1. This resistor exists for input pins 10, 11, 17, 18 and 19. This resistor does not exist in the input circuit structure of the other pins.