RF LDMOS Wideband Integrated Power Amplifiers

The A3I35D025WN wideband integrated circuit is designed for cellular base station applications requiring very wide instantaneous bandwidth capability. This circuit includes on-chip matching that makes it usable from 3200 to 4000 MHz. Its multi-stage structure is rated for 20 to 32 V operation and covers all typical cellular base station modulation formats.

3500 MHz

- Typical Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 72 mA, $I_{DQ2(A+B)}$ = 260 mA, P_{out} = 3.4 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
3400 MHz	28.5	16.5	–46.5
3500 MHz	28.8	17.0	–46.3
3600 MHz	28.9	17.3	–46.1
3700 MHz	28.7	17.7	–46.4
3800 MHz	28.5	17.9	–46.2

A3I35D025WNR1
A3I35D025WGNR1

3200–4000 MHz, 3.4 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

TO-270WB-17 PLASTIC A3I35D025WN

TO-270WBG-17 PLASTIC A3I35D025WGN

Features

- Designed for wide instantaneous bandwidth applications
- On-chip matching (50 ohm input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function (2)
- Designed for digital predistortion error correction systems
- Optimized for Doherty applications

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

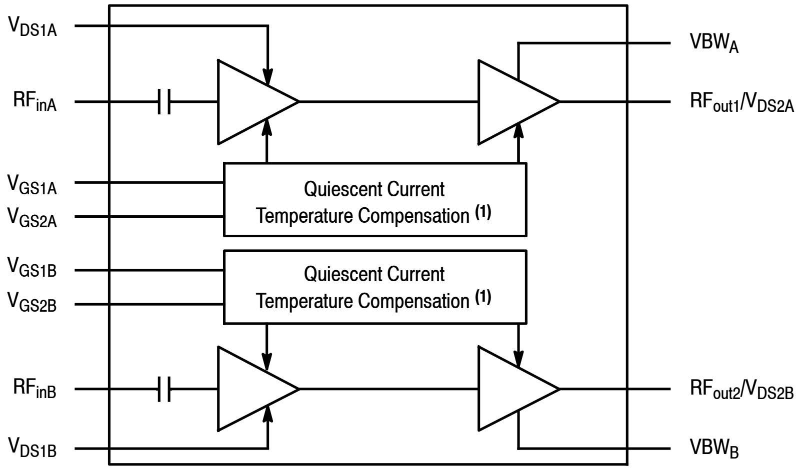
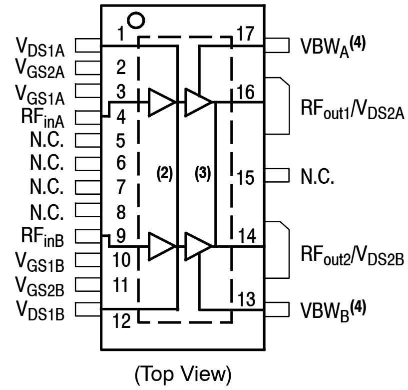


Figure 1. Functional Block Diagram



Note: Exposed backside of the package is the source terminal for the transistor.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

2. Pin connections 1 and 12 are DC coupled and RF independent.
3. Pin connections 14 and 16 are DC coupled and RF independent.
4. Device can operate with V_{DD} current supplied through pin 13 and pin 17.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (5,6)	T_J	–40 to +225	°C
Input Power	P_{in}	28	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (6,7)	Unit
Thermal Resistance, Junction to Case Case Temperature 70°C, 3.4 W, 3600 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 64 mA Stage 2, 28 Vdc, $I_{DQ2(A+B)}$ = 260 mA	$R_{\theta JC}$	 5.6 1.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1A
Charge Device Model (per JS-002-2014)	C1

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

5. Continuous use at maximum temperature will affect MTTF.
6. MTTF calculator available at http://www.nxp.com/RF/calculators.
7. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 – Off Characteristics					
Zero Gate Voltage Drain Leakage Current (1) (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (1) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (2) (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 – On Characteristics					
Gate Threshold Voltage (2) (V_{DS} = 10 Vdc, I_D = 3 μAdc)	$V_{GS(th)}$	1.9	2.3	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ1(A+B)}$ = 72 mAdc)	$V_{GS(Q)}$	—	3.6	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 72 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6.0	7.2	8.0	Vdc
Stage 2 – Off Characteristics					
Zero Gate Voltage Drain Leakage Current (1) (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (1) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (2) (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 – On Characteristics					
Gate Threshold Voltage (2) (V_{DS} = 10 Vdc, I_D = 18 μAdc)	$V_{GS(th)}$	1.9	2.3	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ2(A+B)}$ = 260 mAdc)	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ2(A+B)}$ = 260 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	5.0	5.5	6.0	Vdc
Drain-Source On-Voltage (1) (V_{GS} = 10 Vdc, I_D = 360 mAdc)	$V_{DS(on)}$	0.05	0.16	0.3	Vdc

1. Side A and Side B are tied together for these measurements.
2. Each side of device measured separately.

(continued)

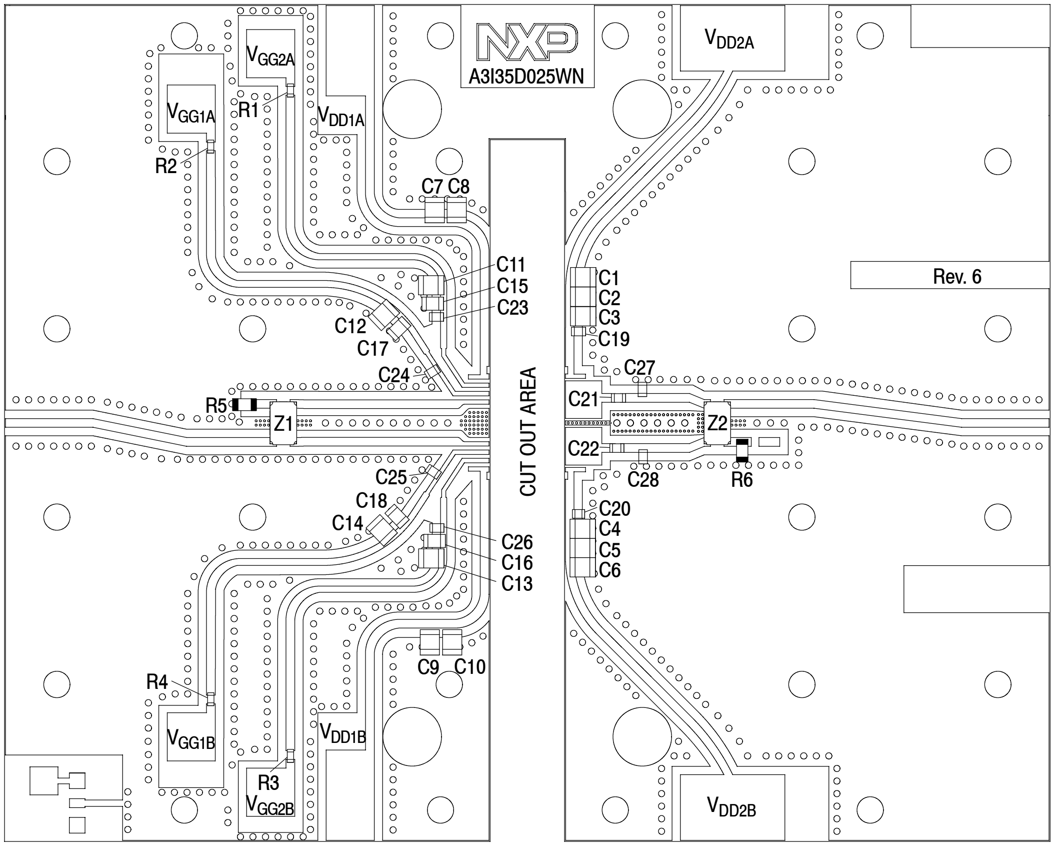
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2,3] (In NXP Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 72 mA, $I_{DQ2(A+B)}$ = 260 mA, P_{out} = 3.4 W Avg., f = 3600 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	26.5	28.9	30.5	dB
Power Added Efficiency	PAE	15.5	17.3	—	%
Adjacent Channel Power Ratio	ACPR	—	–46.1	–42.5	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	30.9	35.5	—	W
Load Mismatch (In NXP Production Test Fixture, 50 ohm system) $I_{DQ1(A+B)}$ = 72 mA, $I_{DQ2(A+B)}$ = 260 mA, f = 3600 MHz					
VSWR 10:1 at 32 Vdc, 34 W CW Output Power (3 dB Input Overdrive from 24 W CW Rated Power)	No Device Degradation				
Typical Performance [4] (In NXP Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 72 mA, $I_{DQ2(A+B)}$ = 260 mA, 3400–3800 MHz Bandwidth					
P_{out} @ 3 dB Compression Point [5]	P3dB	—	35	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 3400–3800 MHz frequency range.)	Φ	—	–11	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	> 300	—	MHz
Quiescent Current Accuracy over Temperature [6] with 2.2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 2.2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	 — —	 2.11 3.27	 — —	%
Gain Flatness in 400 MHz Bandwidth @ P_{out} = 3.4 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.039	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP1dB	—	0.012	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A3I35D025WNR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-17
A3I35D025WGNR1		TO-270WBG-17

1. The first stage drains (V_{DD1A} and V_{DD1B}) and second stage drains (V_{DD2A} and V_{DD2B}) must be tied together and powered by a single DC power supply.
2. Part internally input and output matched.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. All data measured in fixture with device soldered to heatsink.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
6. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

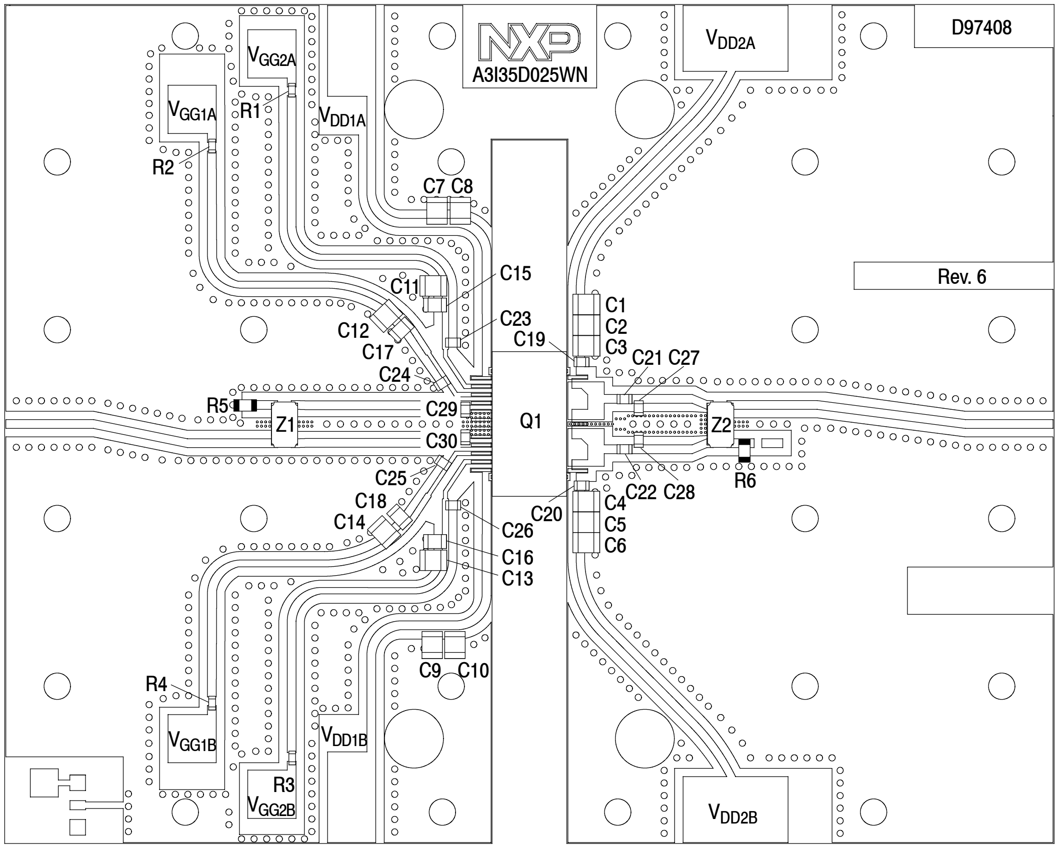


Note: The first stage drains (V_{DD1A} and V_{DD1B}) and second stage drains (V_{DD2A} and V_{DD2B}) must be tied together and powered by a single DC power supply.

Figure 3. A3I35D025WNR1 Production Test Circuit Component Layout

Table 7. A3I35D025WNR1 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	10 μF Chip Capacitor	C3225X7S1H106M250AB	TDK
C15, C16, C17, C18	10 nF Chip Capacitor	C0805C103K5RAC	Kemet
C19, C20, C21, C22, C23, C24, C25, C26	3.3 pF Chip Capacitor	ATC600S3R3BT250XT	ATC
C27, C28	0.2 pF Chip Capacitor	ATC600S0R2BT250XT	ATC
R1, R2, R3, R4	2.2 kΩ, 1/8 W Chip Resistor	CRCW08052K20JNEA	Vishay
R5, R6	50 Ω, 8 W Termination Chip Resistor	C8A50Z4B	Anaren
Z1, Z2	3300–3800 MHz Band, 90°, 3 dB Hybrid Coupler	X3C35F1-03S	Anaren
PCB	Taconic RF35A2, 0.020″, ε_r = 3.66	—	MTL



Note 1: All data measured in fixture with device soldered to heatsink.

Note 2: The first stage drains (V_{DD1A} and V_{DD1B}) and second stage drains (V_{DD2A} and V_{DD2B}) must be tied together and powered by a single DC power supply.

Figure 4. A3I35D025WNR1 Characterization Test Circuit Component Layout — 3400–3800 MHz

Table 8. A3I35D025WNR1 Characterization Test Circuit Component Designations and Values — 3400–3800 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	10 μF Chip Capacitor	C3225X7S1H106M250AB	TDK
C15, C16, C17, C18	10 nF Chip Capacitor	C0805C103K5RAC	Kemet
C19, C20, C21, C22, C23, C24, C25, C26	3.3 pF Chip Capacitor	ATC600S3R3BT250XT	ATC
C27, C28	0.2 pF Chip Capacitor	ATC600S0R2BT250XT	ATC
C29, C30	0.5 pF Chip Capacitor	ATC600S0R5BT250XT	ATC
Q1	RF Power LDMOS Transistor	A3I35D025WN	NXP
R1, R2, R3, R4	2.2 kΩ, 1/8 W Chip Resistor	CRCW08052K20JNEA	Vishay
R5, R6	50 Ω, 8 W Termination Chip Resistor	C8A50Z4B	Anaren
Z1, Z2	3300–3800 MHz Band, 90°, 3 dB Hybrid Coupler	X3C35F1-03S	Anaren
PCB	Taconic RF35A2, 0.020″, ε_r = 3.66	D97408	MTL

Table 9. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, $I_{DQ1(A)}$ = 36 mA, $I_{DQ2(A)}$ = 130 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
3200	78.0 – j14.9	80.6 + j7.43	17.9 – j24.2	27.6	42.1	16	50.5	–7
3400	60.6 + j14.4	60.6 – j15.9	20.1 – j19.5	28.1	42.1	16	50.7	–3
3600	47.3 + j7.35	54.7 – j8.11	16.3 – j18.7	27.7	42.4	17	53.7	–3
3800	37.2 – j9.77	47.6 + j6.54	14.1 – j18.3	26.6	42.6	18	52.6	–3
4000	27.5 – j10.3	40.8 + j9.76	14.2 – j18.1	25.9	42.6	18	51.1	–6

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
3200	78.0 – j14.9	78.1 + j4.47	16.9 – j23.9	25.4	43.0	20	52.3	–11
3400	60.6 + j14.4	57.7 – j15.1	19.3 – j21.4	25.9	42.9	20	52.1	–5
3600	47.3 + j7.35	51.6 – j6.64	16.5 – j20.7	25.5	43.2	21	54.5	–3
3800	37.2 – j9.77	44.4 + j8.20	14.4 – j19.6	24.5	43.3	21	52.7	–3
4000	27.5 – j10.3	37.9 + j12.7	15.0 – j19.2	23.8	43.2	21	50.6	–9

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

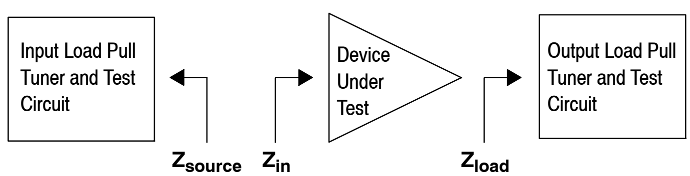


Table 10. Load Pull Performance — Maximum Efficiency Tuning

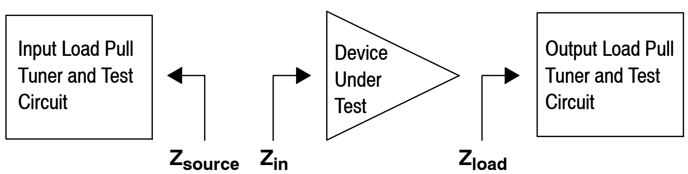
V_{DD} = 28 Vdc, $I_{DQ1(A)}$ = 36 mA, $I_{DQ2(A)}$ = 130 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
3200	78.0 – j14.9	89.3 + j9.63	31.4 – j22.6	28.9	41.2	13	55.7	–9
3400	60.6 + j14.4	64.5 – j22.5	26.7 – j8.05	29.3	41.1	13	56.4	–6
3600	47.3 + j7.35	57.7 – j16.2	15.1 – j6.90	28.7	41.0	12	59.2	–8
3800	37.2 – j9.77	48.5 + j0.17	12.3 – j11.0	27.5	41.6	15	58.1	–7
4000	27.5 – j10.3	40.6 + j2.95	9.72 – j12.6	26.8	41.7	15	56.2	–9

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
3200	78.0 – j14.9	88.3 + j6.72	32.6 – j22.0	27.0	42.0	16	57.7	–14
3400	60.6 + j14.4	62.8 – j22.2	27.2 – j7.61	27.4	41.8	15	58.1	–9
3600	47.3 + j7.35	53.9 – j12.9	17.0 – j9.75	26.5	42.3	17	60.5	–8
3800	37.2 – j9.77	45.7 + j1.91	11.8 – j11.6	25.4	42.4	17	57.8	–7
4000	27.5 – j10.3	37.1 + j7.45	11.0 – j13.2	24.7	42.5	18	55.1	–12

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB – TYPICAL LOAD PULL CONTOURS — 3600 MHz

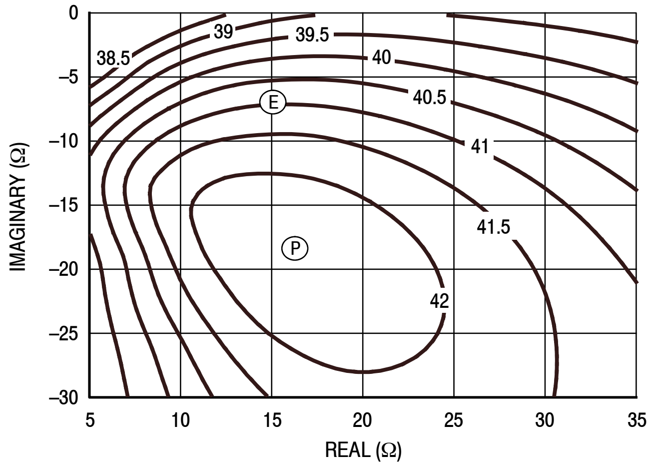


Figure 5. P1dB Load Pull Output Power Contours (dBm)

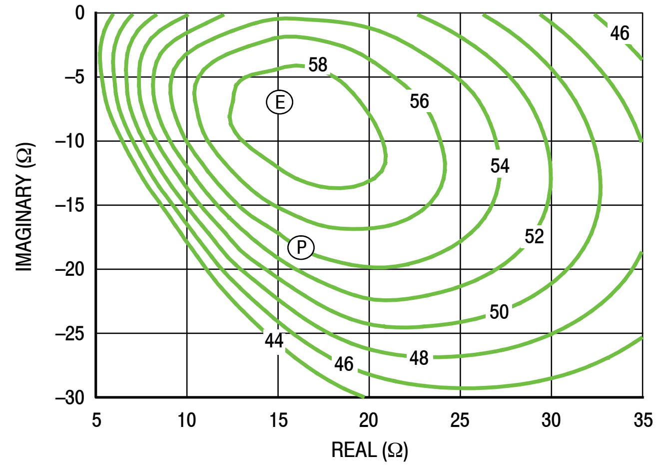


Figure 6. P1dB Load Pull Efficiency Contours (%)

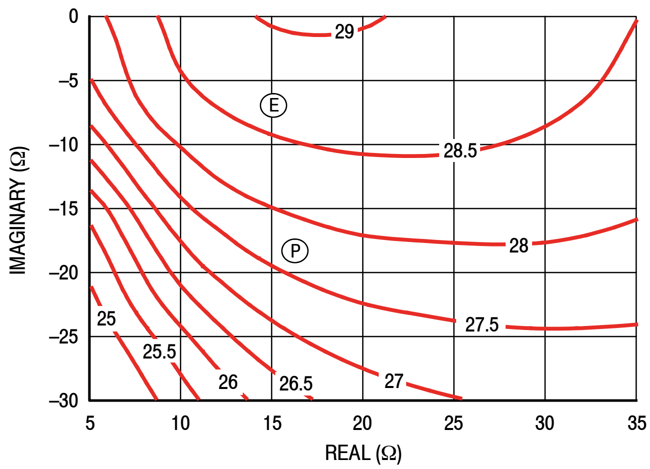


Figure 7. P1dB Load Pull Gain Contours (dB)

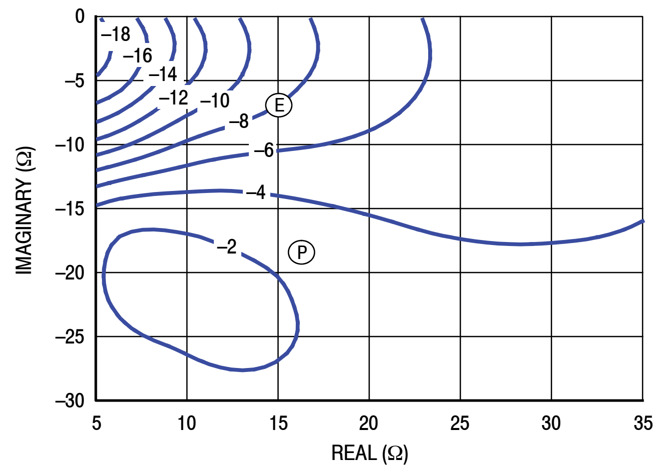


Figure 8. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 3600 MHz

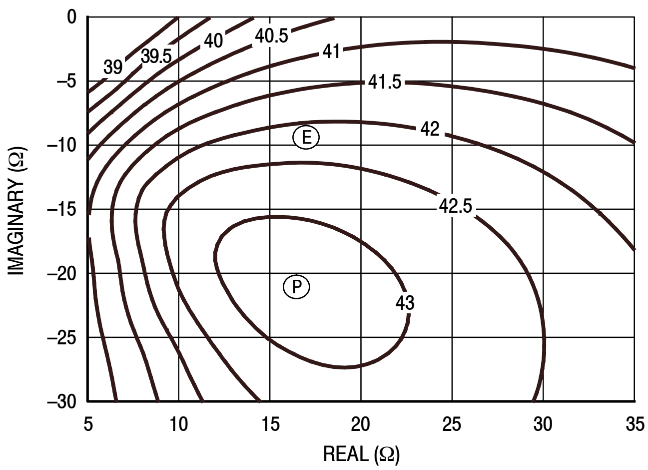


Figure 9. P3dB Load Pull Output Power Contours (dBm)

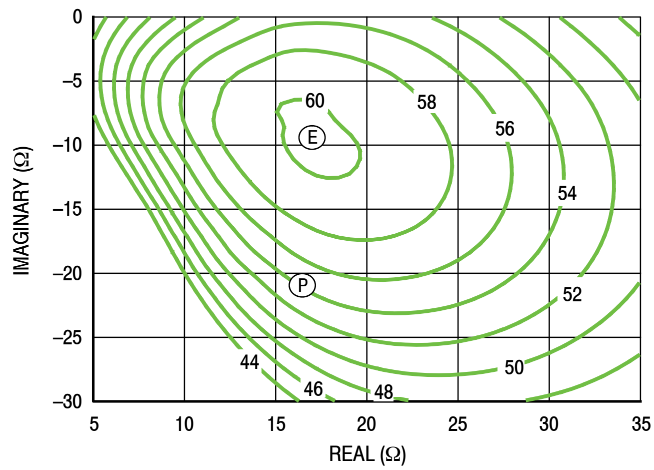


Figure 10. P3dB Load Pull Efficiency Contours (%)

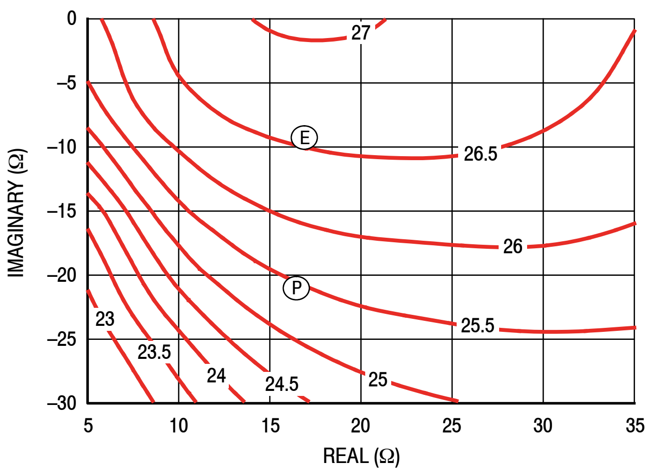


Figure 11. P3dB Load Pull Gain Contours (dB)

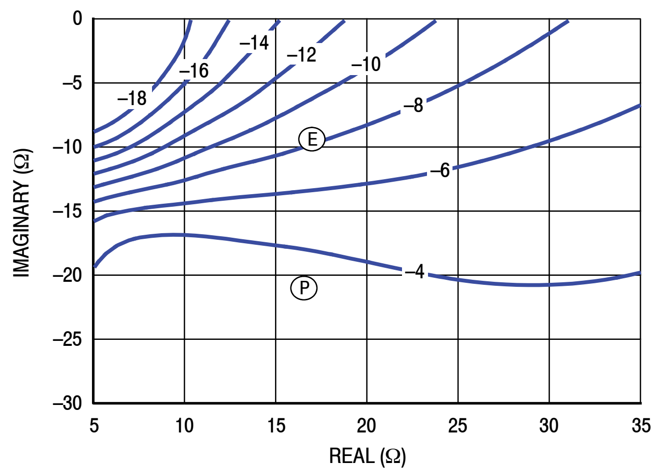


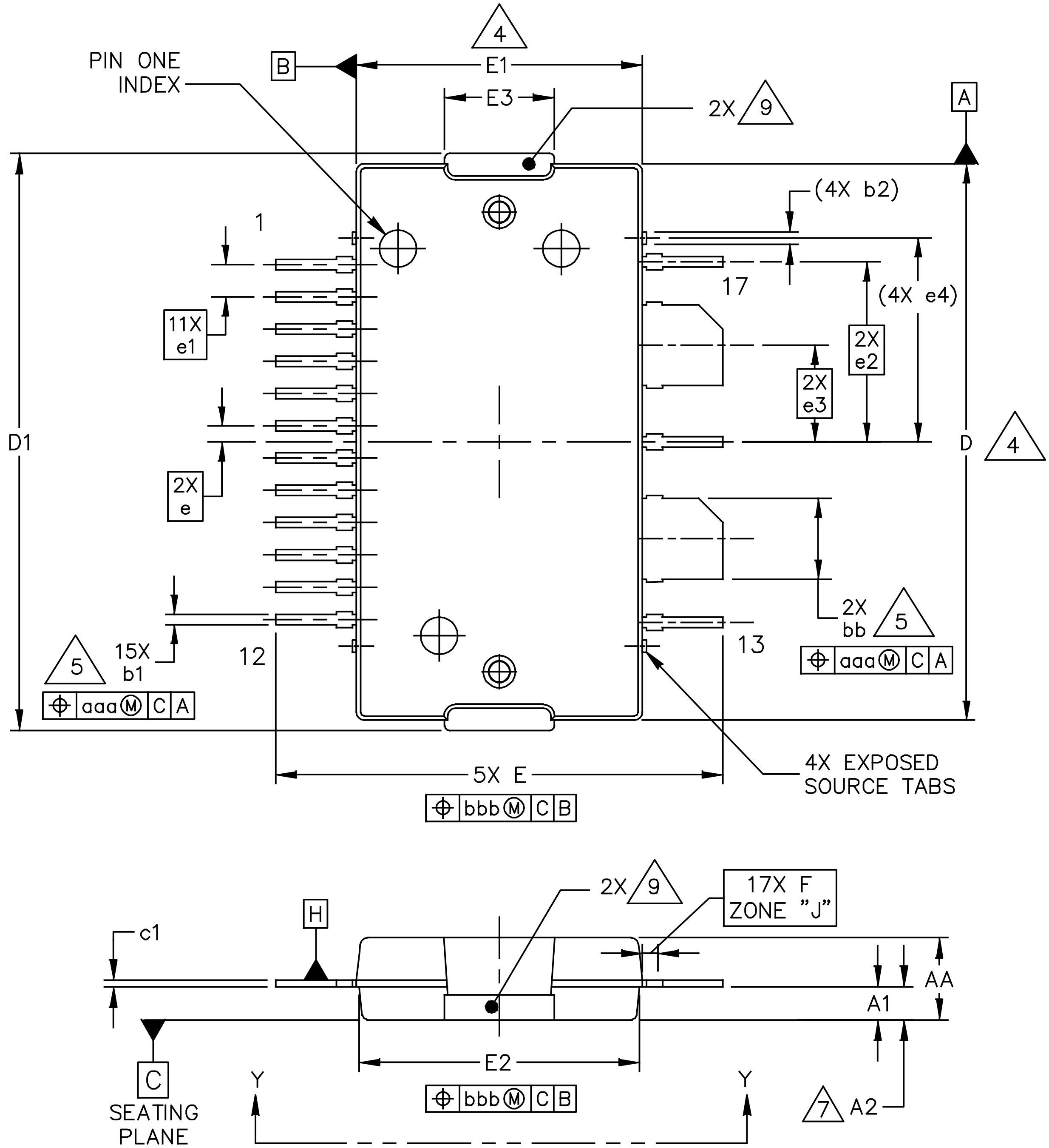
Figure 12. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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	STANDARD: NON–JEDEC	
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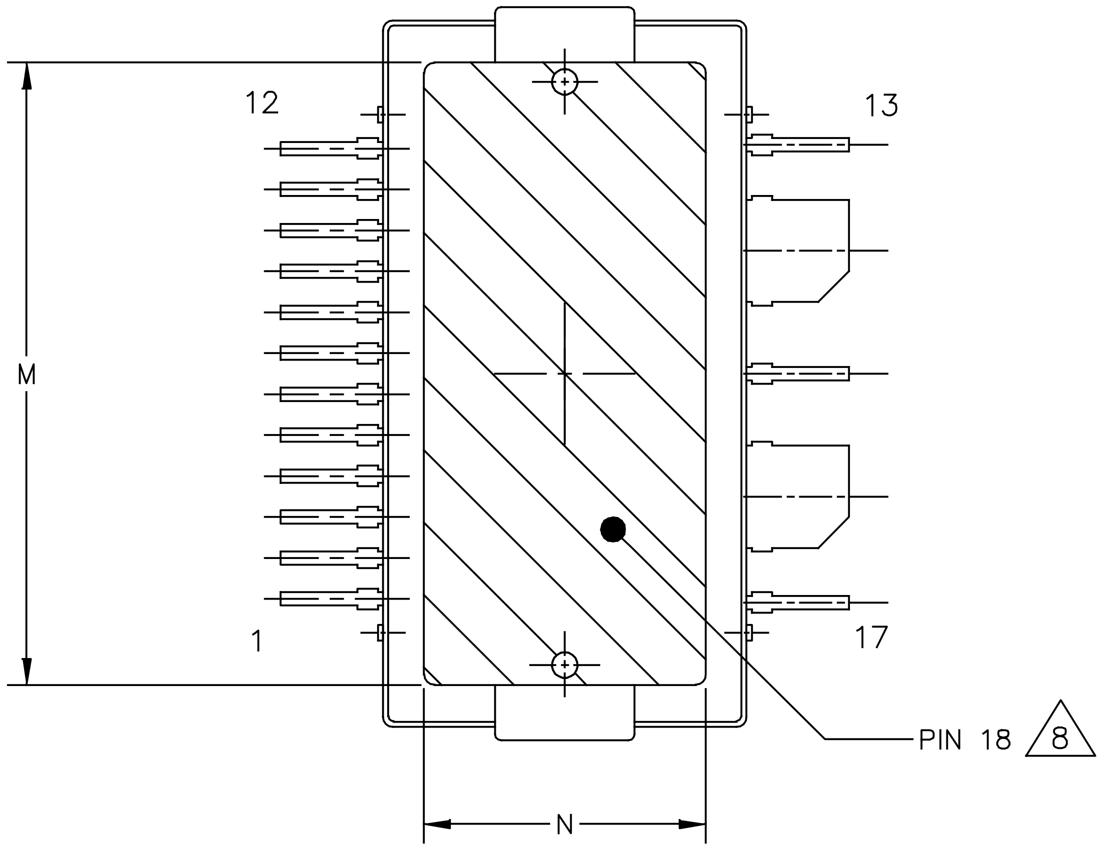

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TITLE: TO–270WB–17	DOCUMENT NO: 98ASA00583D REV: B	
	STANDARD: NON–JEDEC	
	SOT1730–1 21 JAN 2016	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

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TITLE: TO—270WB—17	DOCUMENT NO: 98ASA00583D	REV: B
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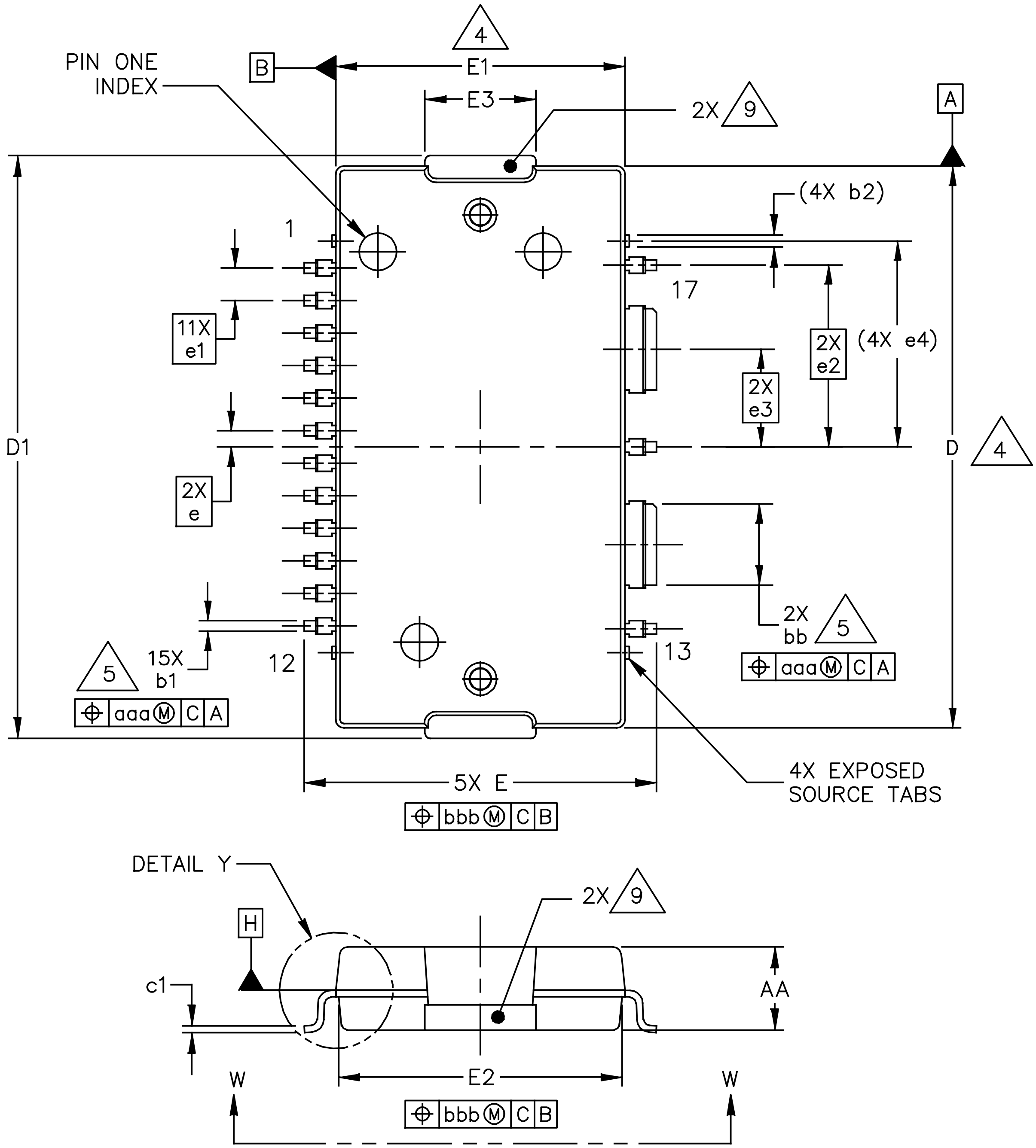
	SOT1730—1	21 JAN 2016



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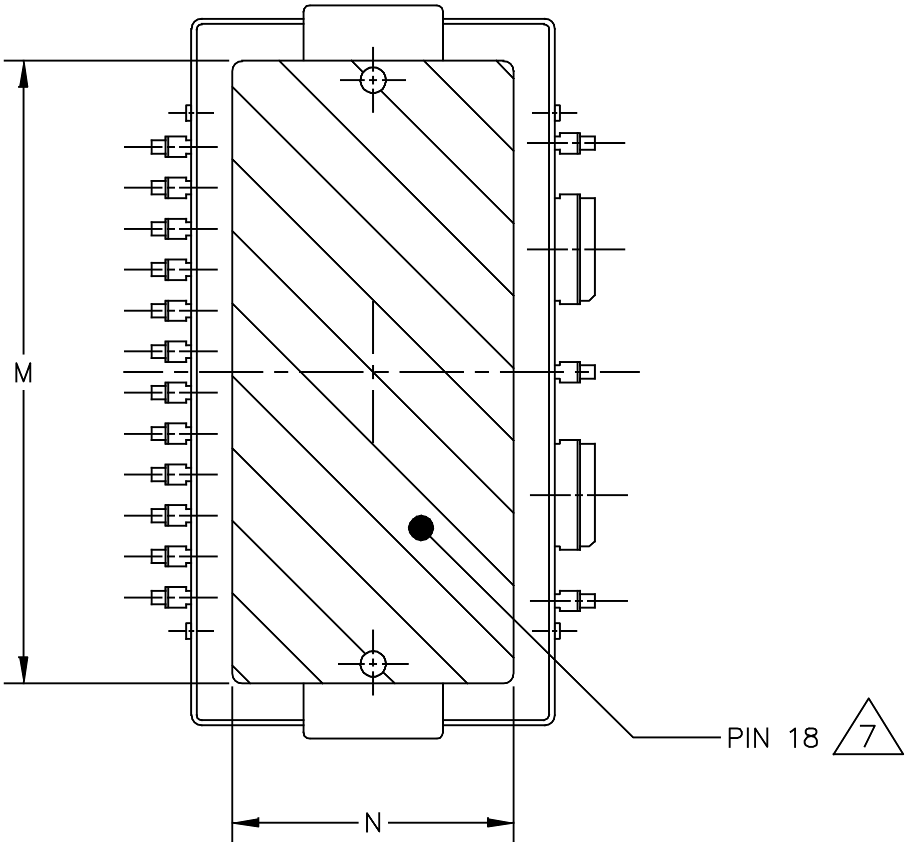
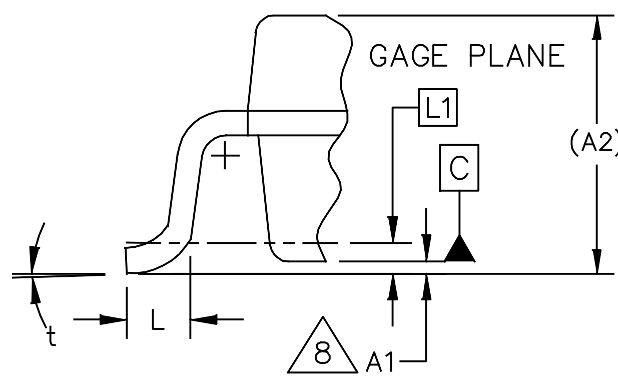
TITLE: TO–270WBG–17	DOCUMENT NO: 98ASA00729D REV: B	
	STANDARD: NON–JEDEC	
	SOT1730–2 12 JAN 2016	





	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270WBG–17	DOCUMENT NO: 98ASA00729D REV: B	
	STANDARD: NON–JEDEC	
	SOT1730–2 12 JAN 2016	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

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TITLE: TO—270WBG—17	DOCUMENT NO: 98ASA00729D	REV: B
	STANDARD: NON—JEDEC	
	SOT1730—2	12 JAN 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2018	• Initial release of data sheet

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