



QUADRUPLE BUS SWITCH WITH INDIVIDUAL POSITIVE ENABLES

IDT74FST3126

FEATURES:

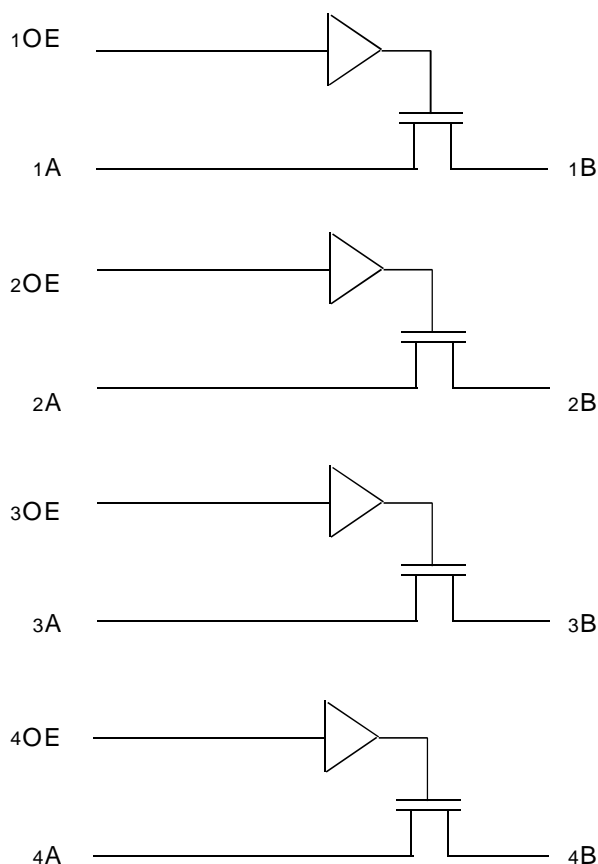
- Bus switches provide zero delay paths
- Extended commercial range of -40°C to +85°C
- Low switch on-resistance: FST3xxx – 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP Packages
- Hot insertion capability
- Very low power dissipation

DESCRIPTION:

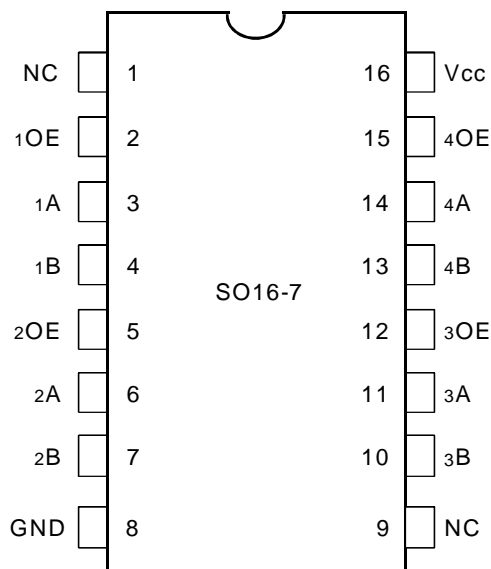
The FST3126 belongs to IDT's family of Bus Switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero. The FST3126 is pin compatible with the industry standard '126 pin out in QSOP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	Maximum Continuous Channel Current	128	mA

FST LINK

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{cc}, Control, and Switch terminals.

CAPACITANCE (1)

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
C _{IN}	Control Input Capacitance		8	pF
C _{I/O}	Switch Input/Output Capacitance	Switch Off	13	pF

NOTES:

- Capacitance is characterized but not tested.
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

PIN DESCRIPTION

Pin Names	I/O	Description
xOE	I	Bus Switch Enable (Active HIGH)
xA	I/O	Bus A
xB	I/O	Bus B

FUNCTION TABLE (1)

OE	A, B	Description
L	Hi-Z	Disconnect
H	A = B	Connect

NOTE:

- H = HIGH
L = LOW

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Control Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V _{IL}	Control Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I _{IH}	Control Input HIGH Current	V _{CC} = Max. V _I = V _{CC} V _I = GND	—	—	±1	μA
I _{IL}	Control Input LOW Current		—	—	±1	μA
I _{OZH}	Current during	V _{CC} = Max., V _O = 0 to 5V	—	—	±1	μA
I _{OZL}	Bus Switch DISCONNECT		—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
I _{OFF}	Switch Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V	—	—	±1	μA
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}	—	0.1	3	μA

FST LINK

BUS SWITCH IMPEDANCE OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
R _{ON}	Switch CONNECT Resistance, A to B ⁽²⁾	V _{CC} = Min. V _{IN} = 0V I _{ON} = 64mA	—	4	7	Ω
		V _{CC} = Min. V _{IN} = 0V I _{ON} = 30mA	—	4	7	Ω
		V _{CC} = Min. V _{IN} = 2.4V I _{ON} = 15mA	—	6	15	Ω
I _{OS}	Short Circuit Current, A to B ⁽³⁾	A(B) = 0V, B(A) = V _{CC}	100	—	—	mA

NOTES:

- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- The voltage drop between the indicated ports divided by the current through the switch.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^(4,5)	$V_{CC} = \text{Max.}$ Outputs Open One Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	35	55	$\mu A/$ MHz/ Enable
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ One Enable Pin Toggling $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.35	0.55	mA
			$V_{IN} = 3.4$ $V_{IN} = GND$		0.6	1.3	
		$V_{CC} = \text{Max.}$ 4 Enable Pins Toggling $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$		1.4	2.2	
			$V_{IN} = 3.4$ $V_{IN} = GND$	—	2.4	5.2	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND . Switch inputs do not contribute to ΔI_{CC} .
- This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency.
Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $C_{PD} = I_{CCD}/V_{CC}$
 C_{PD} = Power Dissipation Capacitance
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot D_{HNT} + I_{CCD} (f_i N)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_i = Control Input Frequency
 N = Number of Control Inputs Toggling at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0V \pm 10\%$

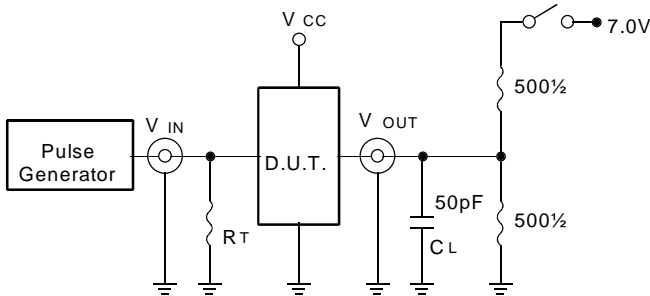
Symbol	Description	Min. ⁽²⁾	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay x_A to $x_B^{(2)}$	—	—	0.25	ns
t_{PZH} t_{PZL}	Switch CONNECT Delay OE to x_A , x_B	1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch DISCONNECT Delay OE to x_A , x_B	1.5	—	5.5	ns
$ Q_{CI} $	Charge Injection, During Switch DISCONNECT, x_{OE} to A or B ⁽³⁾	—	1.5	—	pC

NOTES:

- See test circuits and waveforms.
- The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.
- $|Q_{CI}|$ is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers.
 $|Q_{DCI}|$ is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

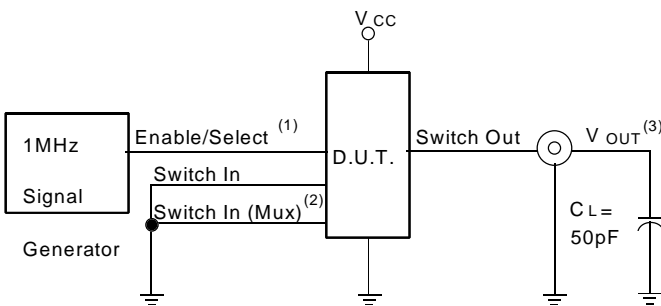
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

FCT LINK

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

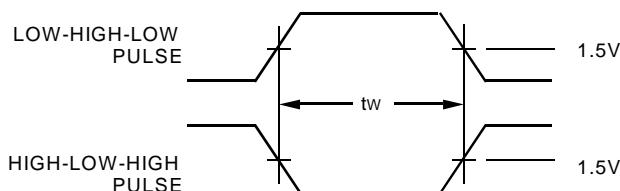
CHARGE INJECTION



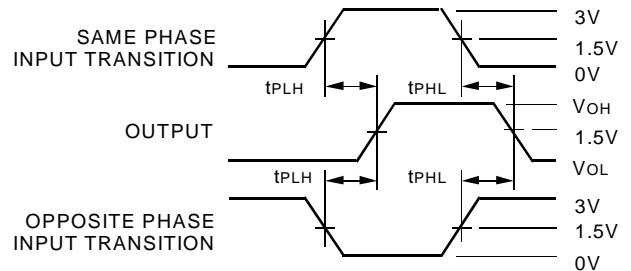
NOTES:

- Select is used with multiplexers for measuring I_{Qbcil} during multiplexer select. During all other tests Enable is used.
- Used with multiplexers to measure I_{Qbcil} only.
- Charge Injection = $\Delta V_{OUT} C_L$, with Enable toggling for I_{Qbcil} or Select toggling for I_{Qbcil}. ΔV_{OUT} is the change in V_{OUT} and is measured with a 10MΩ probe.

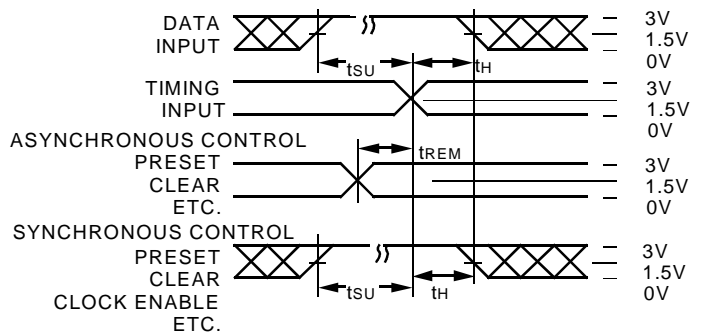
PULSE WIDTH



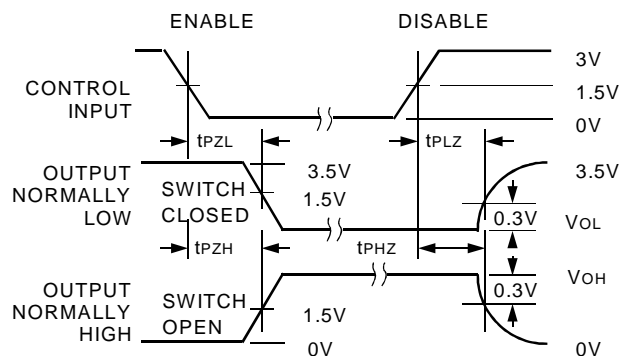
PROPAGATION DELAY



SET-UP, HOLD, AND RELEASE TIMES



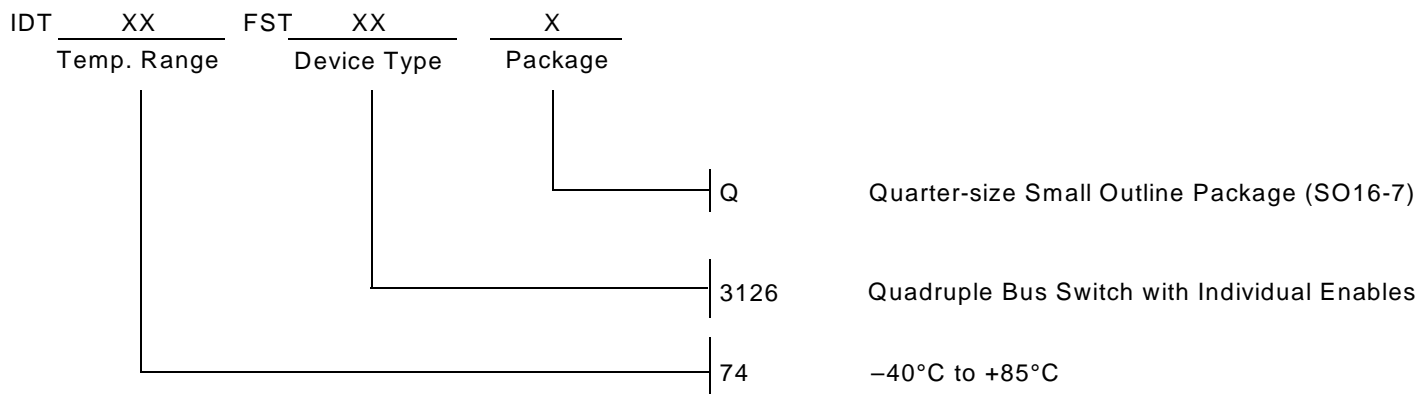
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate \leq 1.0MHz; t_f \leq 2.5ns; t_r \leq 2.5ns

ORDERING INFORMATION



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