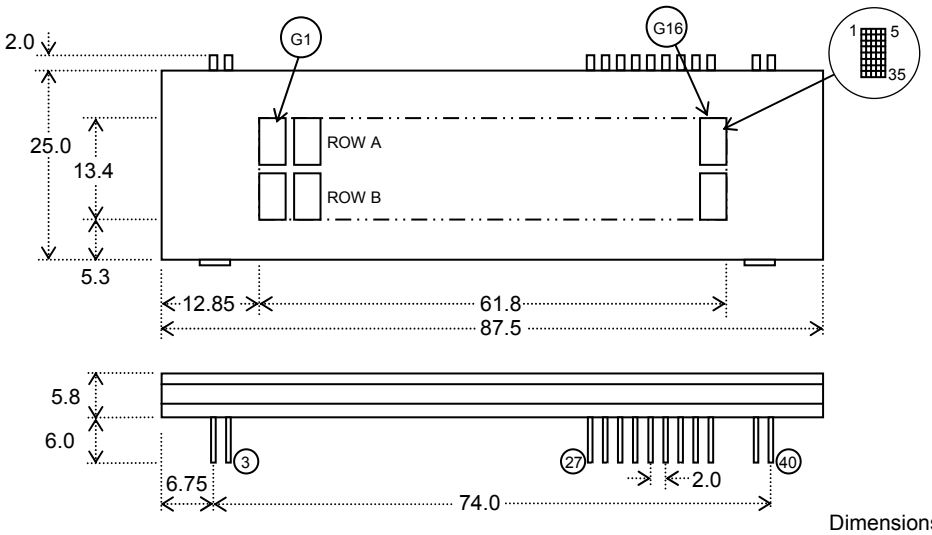
5 x 7 Dot Character Chip In Glass VFD DN1625L

- 2 Lines of 16 Characters
- 5mm High 5 x 7 Dot Matrix Font
- Chip In Glass Driver IC
- High Brightness Blue Green Display
- Low Pinout Count
- Wide Operating Temperature

This VF glass includes a 96 bit serial shift register, latched driver which connects to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor.



Dimensions in mm
See full spec for tolerances

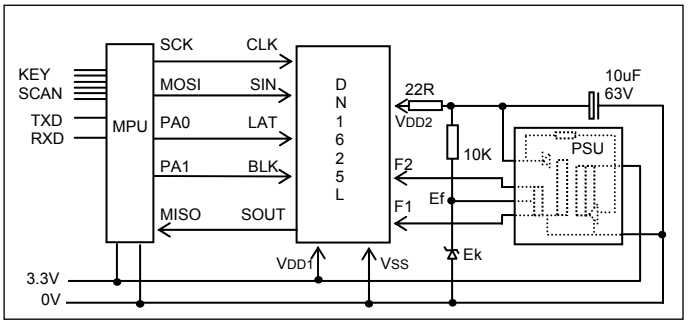
PIN OUT

Pin	Sig
1	NP
2	F+
3	F+
27	SIN
28	VDD 1
29	SOUT
30	LAT
31	BLK
32	CLK
33	VSS
34	VSS
35	VDD2
38	F-
39	F-
40	NP

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V DD1	3.0	3.3	3.6	V	VSS=0V
Logic Current	I DD1	-	1.0	2.0	mA	VDD1=3.3V
Filament Voltage	E f	3.2	3.5	3.8	Vdc	VDD2=0V
Filament Current	I f	64.0	71	78.0	mAdc	VDD2=0V
Display Voltage	V DD2	20.0	28	32.0	V	VSS=0V
Display Current	I DD2	-	6.0	12.0	mA	VDD2=28V
Filament Bias	E K	1.0	1.5	-	V	VSS=0V
Logic High Input	VIH	V DD1x0.85	-	V DD1	V	VSS=0V
Logic Low Input	VIL	VSS	-	V DD1x0.15	V	VSS=0V
Logic High Input	IIH	-0.1	-	0.1	µA	VDD1=3.3V
Logic Low Input	IIL	-30	-12	-5	µA	VDD1=3.3V

INTERFACE EXAMPLE

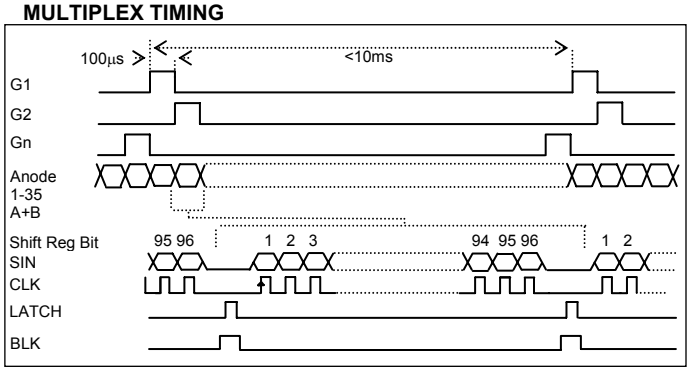


ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Character Size/Pitch (XxY mm)	2.55 x 4.7/3.95 x 8.7
Dot Size/Pitch (XxY mm)	0.35 x 0.5/0.55 x 0.7
Luminance	700 cd/m^2 Typ
Colour of Illumination	Blue-Green (505nm)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. Optical filters can provide additional colours.
2. The power on rise time should be less than 50ms.
3. The 22R resistor at the VDD2 input is required to prevent current surge during switching.
4. If scanning of the display stops with VDD2 applied, the BLK input must be set high to prevent damage to the display

MULTIPLEX TIMING



SHIFT REGISTER ASSIGNMENT

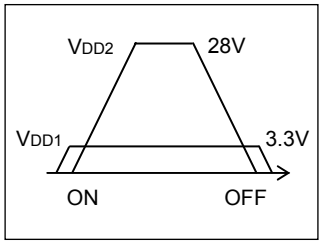
Electrode	Bit Numbers
Grid G1-G16	1-16
Dot PA1 – PA35	96 - 62
Dot PB1 – PB35	58 - 24
Not Connected	17-23, 59-61

The interlaced dot anode and grid data is clocked into the shift register in the above 96 bit sequence for each character scanned.

INTERFACE TIMING

Parameter	Time
CLK Cycle	300ns min
CLK High	140ns min
CLK Low	140ns min
SIN Setup	120ns min
SIN Hold	120ns min
LAT High	480ns min
CLK then LAT	3.73us min
BLK Hold	10µs min

POWER SEQUENCE



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Doc Ref: 17789 Iss:1 06Jun07