MC74HC14A

Hex Schmitt-Trigger Inverter

High−Performance Silicon−Gate CMOS

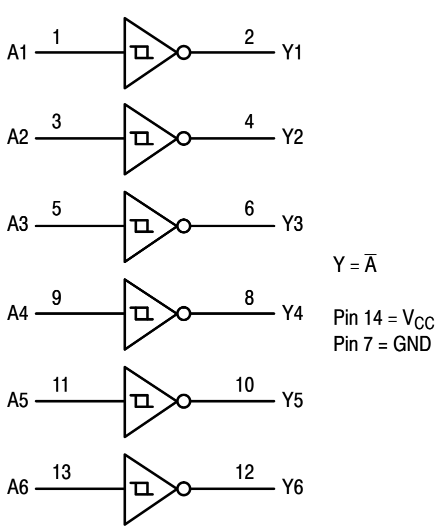
The MC74HC14A is identical in pinout to the LS14, LS04 and the HC04. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC14A is useful to “square up” slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the HC14A finds applications in noisy environments.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 60 FETs or 15 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

LOGIC DIAGRAM



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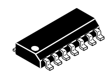
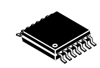
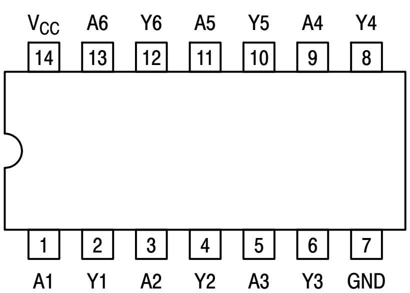


SOIC−14 NB
D SUFFIX
CASE 751A



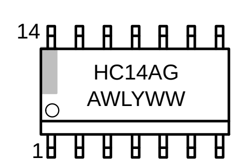
TSSOP−14
DT SUFFIX
CASE 948G

PIN ASSIGNMENT

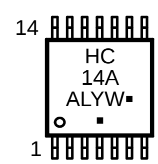


14−Lead (Top View)

MARKING DIAGRAMS



SOIC−14 NB



TSSOP−14

A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	 260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: −6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	–55	+125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	No Limit* No Limit* No Limit*	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*When V_{in} = 50% V_{CC}, I_{CC} > 1mA

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{T+} max	Maximum Positive−Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	V
V_{T+} min	Minimum Positive−Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	1.0 1.5 2.3 3.0	0.95 1.45 2.25 2.95	0.95 1.45 2.25 2.95	V
V_{T-} max	Maximum Negative−Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	0.9 1.4 2.0 2.6	0.95 1.45 2.05 2.65	0.95 1.45 2.05 2.65	V
V_{T-} min	Minimum Negative−Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	V
$V_H$max (Note 1)	Maximum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or $V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	V
$V_H$min (Note 1)	Minimum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or $V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} \le V_{T-}$ min $\lvert I_{out}\rvert \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} \le V_{T-}$ min $\lvert I_{out}\rvert \le 2.4mA$ $\lvert I_{out}\rvert \le 4.0mA$ $\lvert I_{out}\rvert \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} \ge V_{T+}$ max $\lvert I_{out}\rvert \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} \ge V_{T+}$ max $\lvert I_{out}\rvert \le 2.4mA$ $\lvert I_{out}\rvert \le 4.0mA$ $\lvert I_{out}\rvert \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	6.0	1.0	10	40	μA

1. $V_H$min > (V_{T+} min) − (V_{T-} max); $V_H$max = (V_{T+} max) − (V_{T-} min).

AC CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

Symbol	Parameter	Typical @ 25°C, V_{CC} = 5.0 V	Unit
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	22	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

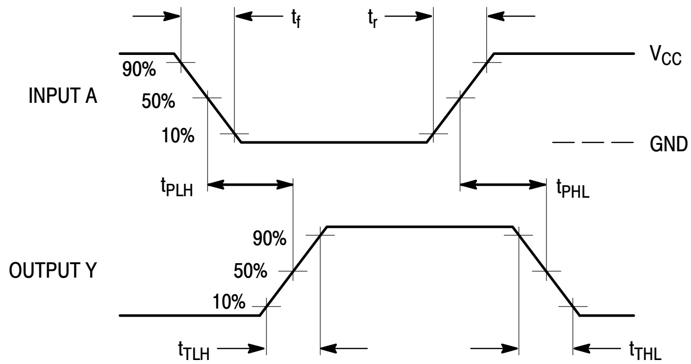
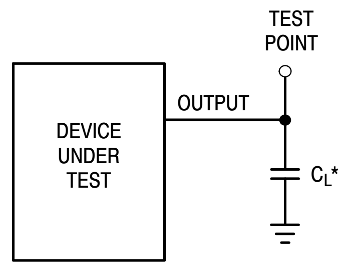


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

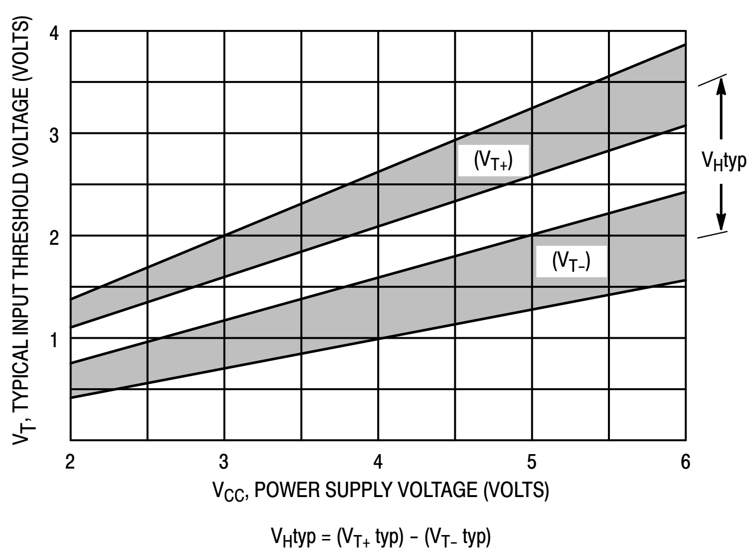


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

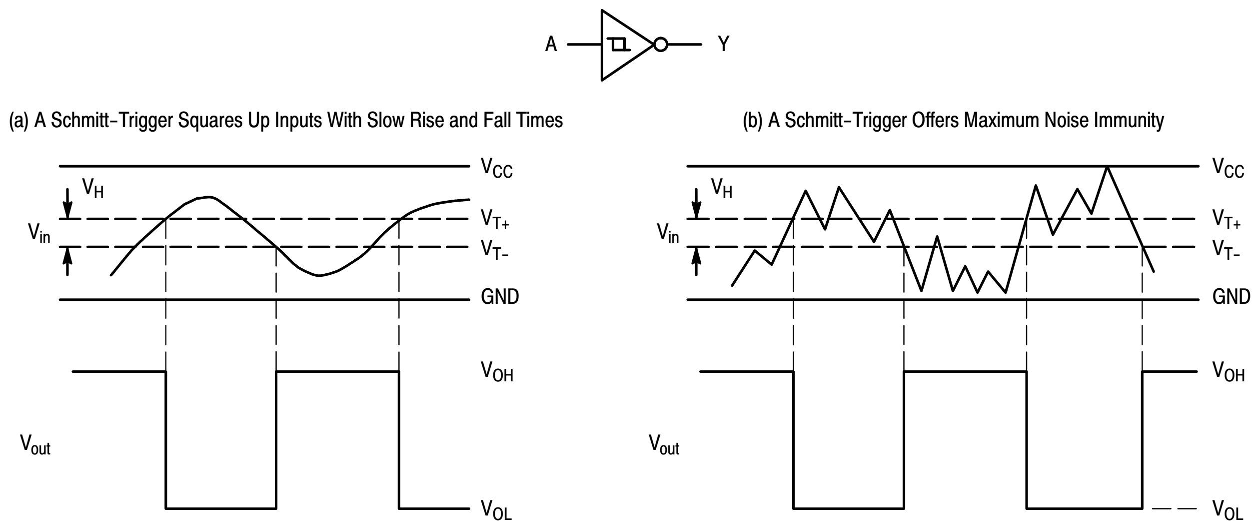


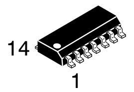
Figure 4. Typical Schmitt−Trigger Applications

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC14ADG	SOIC−14 NB (Pb−Free)	55 Units / Rail
MC74HC14ADR2G	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
MC74HC14ADTG	TSSOP−14 (Pb−Free)	96 Units / Rail
MC74HC14ADTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NLV74HC14ADG*	SOIC−14 NB (Pb−Free)	55 Units / Rail
NLV74HC14ADR2G*	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
NLV74HC14ADTG*	TSSOP−14 (Pb−Free)	96 Units / Rail
NLV74HC14ADTR2G*	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

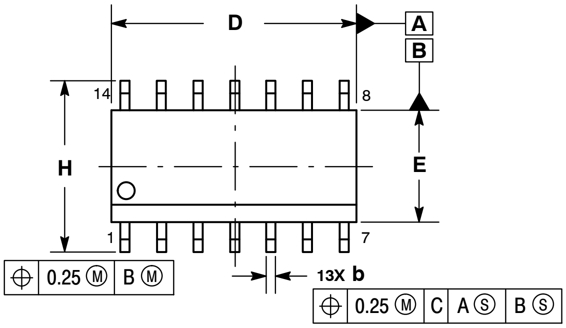
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

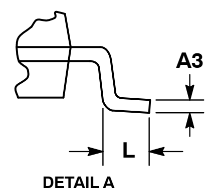


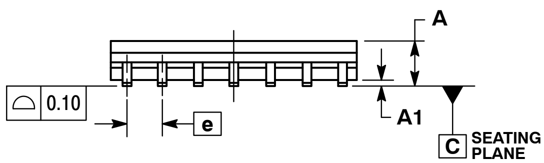
SCALE 1:1

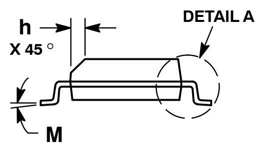
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016





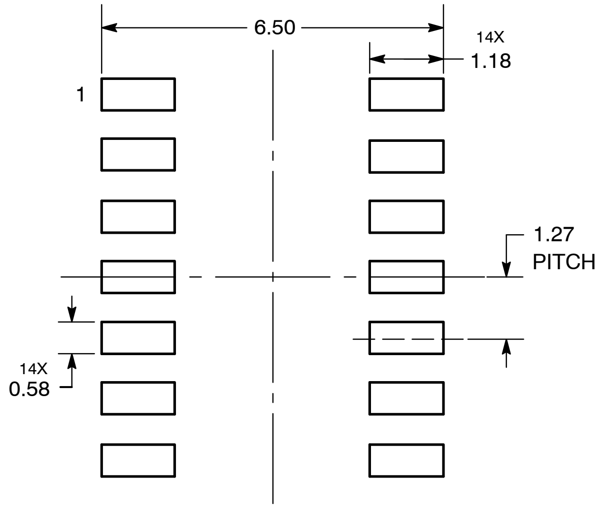




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

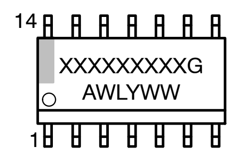
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−14 NB	PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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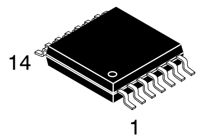
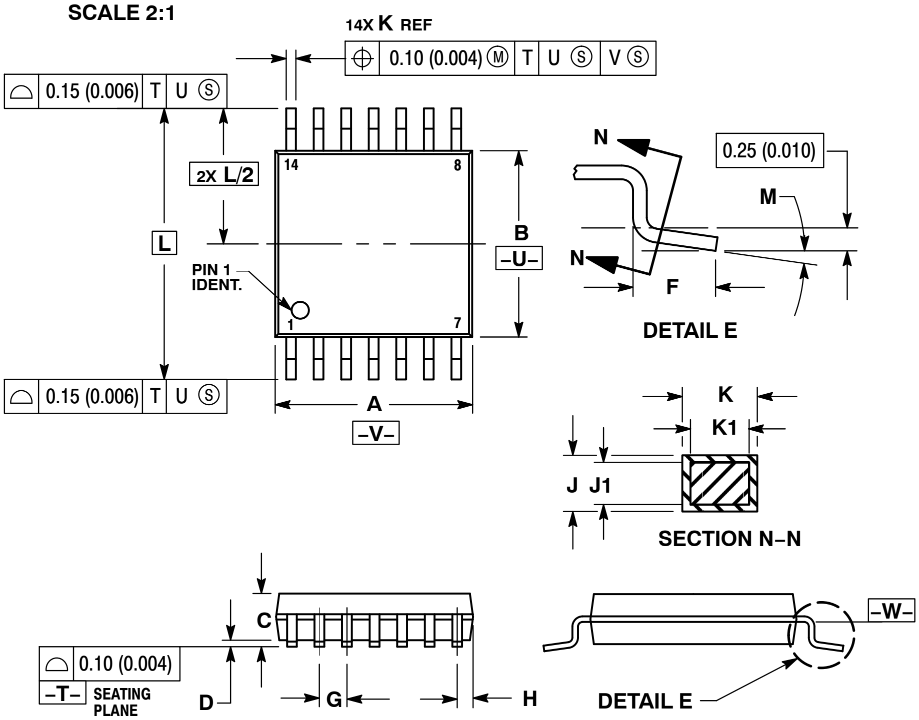


SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

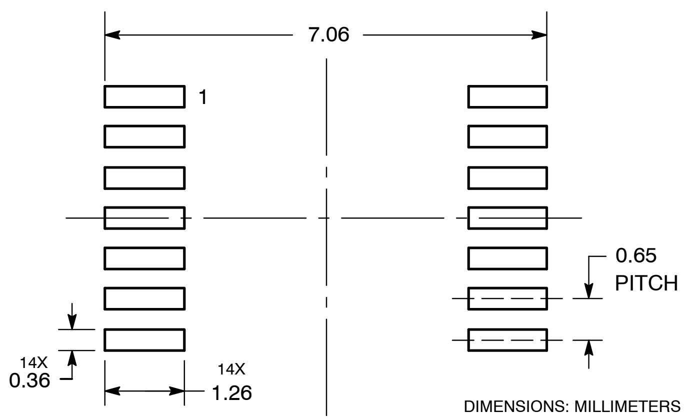
DATE 17 FEB 2016



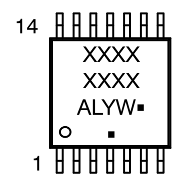
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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