# *GENLINX*™ GS9005B
## Serial Digital Receiver

DATA SHEET

### FEATURES

- **automatic cable equalization (typically 300m of high quality cable at 270Mb/s)**
- **fully compatible with SMPTE 259M and operational to 400 Mb/s**
- **adjustment free receiver when used with the GS9000B or GS9000S decoder and GS9010A Automatic Tuning Sub-system**
- **signal strength indicator**
- **selectable cable or direct digital inputs**
- **28 pin PLCC packaging**
- **Pb-free and Green**

### APPLICATIONS

- $4f_{SC}$, 4:2:2 and 360 Mb/s serial digital interfaces

### ORDERING INFORMATION

| Part Number | Package | Temperature | Pb-Free and Green |
|---|---|---|---|
| GS9005BCPJ | 28 Pin PLCC | 0°C to 70°C | No |
| GS9005BCTJ | 28 Pin PLCC Tape | 0°C to 70°C | No |
| GS9005BCPJE3 | 28 Pin PLCC | 0°C to 70°C | Yes |

### DEVICE DESCRIPTION

The GS9005B is a monolithic IC designed to receive SMPTE 259M serial digital video signals. This device performs the functions of automatic cable equalization and data and clock recovery. It interfaces directly with the ***GENLINX***™ GS9000B or GS9000S decoder, and GS9010A Automatic Tuning Subsystem.

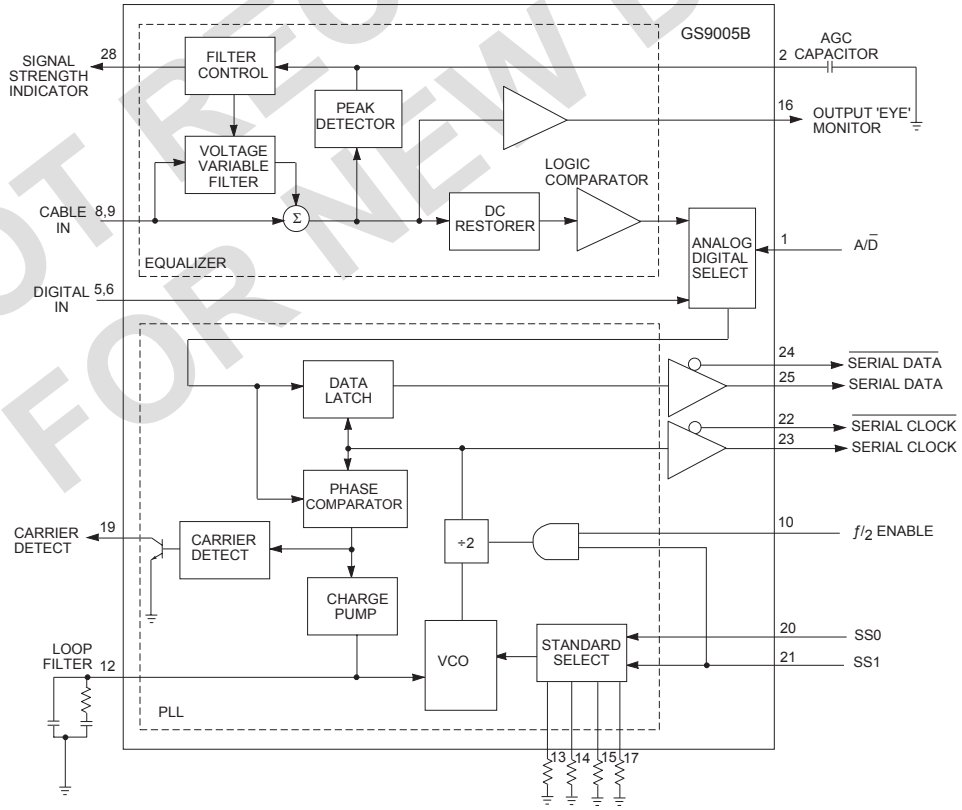
The VCO centre frequencies are controlled by external resistors which can be selected by applying a two bit binary code to the Standards Select input pins.

An additional feature is the Signal Strength Indicator output which provides a 0.5V to 0V analog output relative to $V_{CC}$ indicating the amount of equalization being applied to the signal.

The GS9005B is packaged in a 28 pin PLCC operating from a single +5 or -5 volt supply.

**SPECIAL NOTE:** $R_{VCO1}$ and $R_{VCO2}$ are functional over a reduced temperature range of $T_A$=0° C to 50° C. $R_{VCO0}$ and $R_{VCO3}$ are functional over the full temperature range of $T_A$=0° C to 70° C. This limitation does not affect operation with the GS9010A ATS.






FUNCTIONAL BLOCK DIAGRAM

Revision Date: November 2004

Document No. 32466 - 1

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (905) 632-2996 fax: (905) 632-5946
Gennum Japan: Shinjuku Green Tower Building 27F 6-14-1, Nishi Shinjuku Shinjuku-ku, Tokyo 160-0023 Japan Tel: +81 (03) 3349-5501 Fax: +81 (03) 3349-5505

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | VALUE / UNITS |
|---|---|
| Supply Voltage | 5.5 V |
| Input Voltage Range (any input) | $V_{CC}$+0.5 to $V_{EE}$-0.5 V |
| DC Input Current (any one input) | 5 mA |
| Power Dissipation | 750 mW |
| Operating Temperature Range | 0°C ≤ $T_A$ ≤70°C |
| Storage Temperature Range | -65°C ≤ $T_S$≤150°C |
| Lead Temperature (soldering, 10 seconds) | 260°C |

**CAUTION**
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



## GS9005B RECEIVER DC ELECTRICAL CHARACTERISTICS

$V_S$ = 5V, $T_A$ = 0°C to 70°C, $R_L$ = 100Ω to ($V_{CC}$ - 2V) unless otherwise shown.

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | | $V_S$ | Operating Range | 4.75 | 5.0 | 5.25 | V | |
| Power Consumption | | $P_D$ | | - | 500 | 700 | mW | |
| Supply Current (Total) | | $I_S$ | | - | 122 | 160 | mA | see Figure13 |
| Serial Data & Clock Output | - High | $V_{OH}$ | $T_A$ = 25°C | -1.025 | - | -0.88 | V | with respect to $V_{CC}$ |
| | - Low | $V_{OL}$ | $T_A$ = 25°C | -1.9 | - | -1.6 | V | with respect to $V_{CC}$ |
| Logic Inputs (1, 10, 20, 21) | - High | $V_{IH\ MIN}$ | | +2.0 | - | - | V | with respect to $V_{EE}$ |
| | - Low | $V_{IL\ MAX}$ | | - | - | +0.8 | V | with respect to $V_{EE}$ |
| Carrier Detect Output Voltage | | $V_{CDL}$ | $R_L$ = 10 kΩ to $V_{CC}$ | - | 0.2 | 0.4 | V | with respect to $V_{EE}$ Open Collector - Active High |
| | | $V_{CDH}$ | | 4.0 | 5.0 | - | V | |
| Signal Strength Indicator Output | | $V_{SS}$ | See Note 2 | -0.6 | - | 0 | V | with respect to $V_{CC}$ |
| Direct Digital Input Levels (5, 6) | | $V_{DDI}$ | | 200 | - | 2000 | mVp-p | Differential Drive |

## GS9005B RECEIVER AC ELECTRICAL CHARACTERISTICS

$V_S$ = 5V, $T_A$ = 0°C to 70°C, $R_L$ = 100Ω to ($V_{CC}$ - 2V) unless otherwise shown.

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Serial Data Bit Rate | $BR_{SDO}$ | $T_A$ = 25°C | 100 | - | 400 | Mb/s | |
| Serial Clock Frequency | $f_{SLK}$ | $T_A$ = 25°C | 100 | - | 400 | MHz | see Figure11 |
| Output Signal Swing | $V_O$ | $T_A$ = 25°C | 700 | 800 | 900 | mV p-p | see Figure12 |
| Serial Data to Serial Clock Synchronization | $t_d$ | See Waveforms | - | -500 | - | ps | Data lags Clock |
| Lock Times | $t_{LOCK}$ | See Note 1 | - | - | 10 | µs | |
| Equalizer Gain | $AV_{EQ}$ | $T_A$ = 25°C | 30 | 36 | - | dB | at 135 MHz |
| Jitter | $t_J$ | $T_A$ = 25°C<br>0 metres, 270 Mb/s | - | ±100 | - | ps p-p | see Figure15 |
| Input Resistance ($\overline{SDI}$/SDI) | $R_{IN}$ | $T_A$ = 25½C | 3k | 5k | - | Ω | see Figure14 |
| Input Capacitance ($\overline{SDI}$/SDI) | $C_{IN}$ | $T_A$ = 25½C | - | 1.8 | - | pF | see Figure14 |
| Output Eye Monitor | $V_{OEM}$ | $R_L$ = 50Ω to $V_{CC}$ | - | 40 | - | mVp-p | |

**NOTES:** **1.** Switching between two sources of the same data rate.
**2.** With weaker signals $V_{SS}$ approaches $V_{CC}$.

The GS9005B Reclocking Receiver is a bipolar integrated circuit containing a built-in cable equalizer and circuitry necessary to re-clock and regenerate the NRZI serial data stream.

Packaged in a 28 pin PLCC, the receiver operates from a single five volt supply at data rates in excess of 400 Mb/s. Typical power consumption is 500 mW. Typical output jitter is ±100 ps at 270 Mb/s.

Serial Digital signals are applied to either a built-in analog cable equalizer via the SDI and $\overline{\text{SDI}}$ inputs (pins 8,9) or via the direct digital inputs DDI and $\overline{\text{DDI}}$ (pins 5,6).

### Cable Equalizer

The Serial Digital signal is connected to the input either differentially or single ended with the unused input being decoupled. The equalized signal is generated by passing the cable signal through a voltage variable filter having a characteristic which closely matches the inverse cable loss characteristic. Additionally, the variation of the filter characteristic with control voltage is designed to imitate the variation of the inverse cable loss characteristic as the cable length is varied.

The amplitude of the equalized signal is monitored by a peak detector circuit which produces an output current with a polarity corresponding to the difference between the desired peak signal level and the actual peak signal level. This output is integrated by an external AGC filter capacitor (AGC CAP pin 2), providing a steady control voltage for the voltage variable filter.

A separate signal strength indicator output, (SSI pin 28), proportional to the amount of AGC is also provided. As the filter characteristic is varied automatically by the application of negative feedback, the amplitude of the equalized signal is kept at a constant level which is representative of the original amplitude at the transmitter.

The equalized signal is then DC restored, effectively restoring the logic threshold of the equalized signal to its correct level irrespective of shifts due to AC coupling.

As the final stage of signal conditioning, a comparator converts the analog output of the DC restorer to a regenerated digital output signal.

An OUTPUT 'EYE' MONITOR (pin 16), allows verification of signal integrity after equalization but before reslicing.

### Analog/$\overline{\text{Digital}}$ Select

A 2:1 multiplexer selects either the equalized (analog) signal or a differential ECL data (digital) signal as input to the reclocker PLL.

A logical HIGH applied to the Analog/$\overline{\text{Digital}}$ Select input (1) routes the equalized signal while a logic LOW routes the direct digital signal to the reclocker.

### Phase Locked Loop

The phase comparator itself compares the position of transitions in the incoming signal with the phase of the local oscillator (VCO). The error-correcting output signals are fed to the charge pump in the form of short pulses. The charge pump converts these pulses into a “charge packet” which is accurately proportional to the system phase error.

The charge packet is then integrated by the second-order loop filter to produce a control voltage for the VCO.

During periods when there are no transitions in the signal, the loop filter voltage is required to hold precisely at its last value so that the VCO does not drift significantly between corrections. Commutating diodes in the charge pump keep the output leakage current extremely low, minimizing VCO frequency drift.

The VCO is implemented using a current-controlled multivibrator, designed to deliver good stability, low phase noise and wide operating frequency capability. The frequency range is design-limited to ±10% about the oscillator centre frequency.

### VCO Centre Frequency Selection

The centre frequency of theVCO is set by one of four external current reference resistors (RVCO0-RVCO3) connected to pins 13,14,15 or 17. These are selected by two logic inputs SS0 and SS1 (pins 20, 21) through a 2:4 decoder according to the following truth table.

| SS1 | SS0 | Resistor Selected |
|---|---|---|
| 0 | 0 | RVCO0 (13) |
| 0 | 1 | RVCO1 (14) |
| 1 | 0 | RVCO2 (15) |
| 1 | 1 | RVCO3 (17) |

As an alternative, the GS9010A Automatic Tuning Sub-system and the GS9000B or GS9000S Decoder may be used in conjunction with the GS9005B to obtain adjustment free and automatic standard select operation (see Figure 20).

With the VCO operating at twice the clock frequency, a clock phase which is centred on the eye of the locked signal is used to latch the incoming data, thus maximising immunity to jitter-induced errors. The alternate phase is used to latch the output re-clocked data SDO and $\overline{\text{SDO}}$ (pins 25, 24). The true and inverse clock signals themselves are available from the SCO and $\overline{\text{SCO}}$ pins 23 and 22.

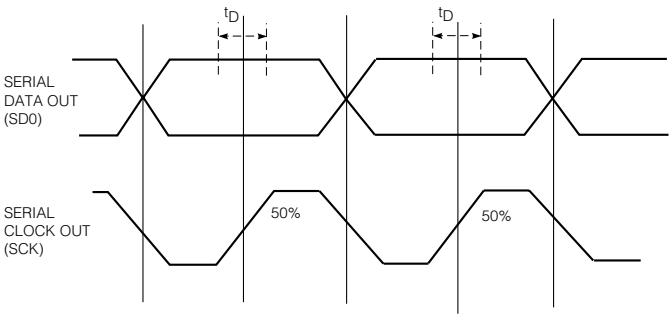



Fig.1 Waveforms

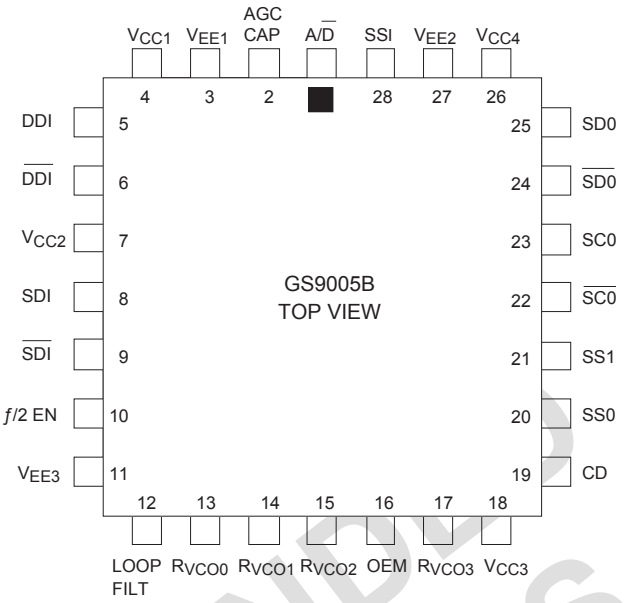



Fig. 2 GS9005B Pin Connections

GS9005B PIN DESCRIPTIONS

| PIN NO. | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | A/$\overline{D}$ | Input | **Analog/$\overline{\text{Digital}}$ Select.** TTL compatible input used to select the input signal source. A logic HIGH routes the Equalizer inputs (pins 8 and 9) to the PLL and a logic LOW routes the Direct Digital inputs (pins 5 and 6) to the PLL. |
| 2 | AGC CAP | Input | **AGC Capacitor.** Connection for the AGC capacitor. |
| 3 | $V_{EE1}$ | | **Power Supply.** Most negative power supply connection. (Equalizer) |
| 4 | $V_{CC1}$ | | **Power Supply**. Most positive power supply connection. (Equalizer) |
| 5,6 | DDI/$\overline{DDI}$ | Input | **Direct Data Inputs (true and inverse).** Pseudo-ECL, differential serial data inputs. These are selected when the A/$\overline{D}$ input (pin 1) is at logic LOW and are self biased to 1.2 volts below $V_{CC}$. They may be directly driven from true ECL drivers when $V_{EE}$ = -5V and $V_{CC}$= 0 V. |
| 7 | $V_{CC2}$ | | **Power Supply**. Most positive power supply connection. ( Phase detector, A/$\overline{D}$ select, carrier detect). |
| 8,9 | SDI/$\overline{SDI}$ | Input | **Serial Data Inputs (true and inverse).** Differential analog serial data inputs. Inputs must be AC coupled and may be driven single ended. These inputs are selected when the A/$\overline{D}$ input (pin 1) is logic HIGH. |
| 10 | ƒ/2 EN | Input | **ƒ/2 Enable**-TTL compatible input used to enable the divide by 2 function. |
| 11 | $V_{EE3}$ | | **Power Supply.** Most negative power supply connection. (VCO, Mux, Standard Select) |
| 12 | LOOP FILT | | **Loop Filter.** Node for connecting the loop filter components. |
| 13 | $R_{VCO0}$ | Input | **VCO Resistor 0.** Analog current input used to set the centre frequency of the VCO when the two Standard Select bits (pins 20 and 21) are set to logic 0,0. A resistor is connected from this pin to $V_{EE}$. |
| 14 | $R_{VCO1}$ | Input | **VCO Resistor 1.** Analog current input used to set the centre frequency of the VCO when Standard Select bit 0 (pin 20) is set HIGH and bit 1 (pin 21) is set LOW. A resistor is connected from this pin to $V_{EE}$. |
| 15 | $R_{VCO2}$ | Input | **VCO Resistor 2.** Analog current input used to set the centre frequency of the VCO when Standard Select bit 0 (pin 20) is set LOW and bit 1 (pin 21) is set HIGH. A resistor is connected from this pin to $V_{EE}$. |
| 16 | OEM | Output | **Output Eye Monitor** Analog voltage representing the serial bit stream after equalization but before reslicing. |
| 17 | $R_{VCO3}$ | Input | **VCO Resistor 3.** Analog current input used to set the centre frequency of the VCO when the two Standard Select bits (pins 20 and 21) are set HIGH. A resistor is connected from this pin to $V_{EE}$. |

| PIN NO | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 18 | $V_{CC3}$ | | **Power Supply.** Most positive power supply connection. (VCO, MUX, standards select). |
| 19 | CD | Output | **Carrier Detect**. Open collector output which goes HIGH when a signal is present at either the Serial Data inputs or the Direct Digital inputs. This output is used in conjunction with the GS9000B or GS9000S in the Automatic Standards Select Mode to disable the 2 bit standard select counter. This pin should see a low impedance (e.g. 1nF to AC Gnd) |
| 20,21 | SS0, SS1 | Inputs | **Standard Select Inputs.** TTL inputs to the 2:4 multiplexer used to select one of four VCO centre frequency setting resistors ($R_{VCO0}$ - $R_{VCO3}$). When both SS0 and SS1 are LOW, $R_{VCO0}$ is selected. When SS0 is HIGH and SS1 is LOW, $R_{VCO1}$ is selected. When SS0 is LOW and SS1 is HIGH, $R_{VCO2}$ is selected and when both SS0 and SS1 are HIGH, $R_{VCO3}$ is selected. These pins should see a low impedance (e.g. 1nF to AC Gnd) |
| 22,23 | $\overline{SCO}$/SCO | Outputs | **Serial Clock Outputs (inverse and true).** Pseudo-ECL differential outputs of the extracted serial clock. These outputs require 390 Ω pull-down resistors to $V_{EE}$. |
| 24,25 | $\overline{SDO}$/SDO | Outputs | **Serial Data Outputs (inverse and true).** Pseudo-ECL differential outputs of the regenerated serial data. These outputs require 390 Ω pull-down resistors to $V_{EE}$. |
| 26 | $V_{CC4}$ | | **Power Supply.** Most positive power supply connection. (ECL outputs) |
| 27 | $V_{EE2}$ | | **Power Supply.** Most negative power supply connection. (Phase detector, $A/\overline{D}$ select, Carrier detect) |
| 28 | SSI | | **Signal Strength Indicator.** Analog output which indicates the amount of AGC action. This output indirectly indicates the amount of equalization and thus cable length. |



INPUT / OUTPUT CIRCUITS

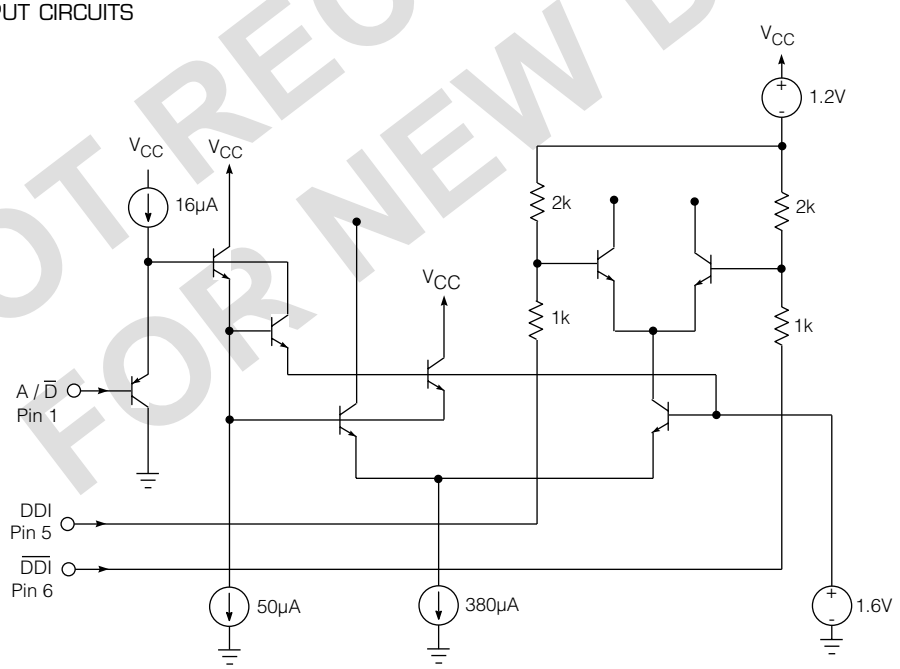



Fig. 3 Pins 1, 5 and 6

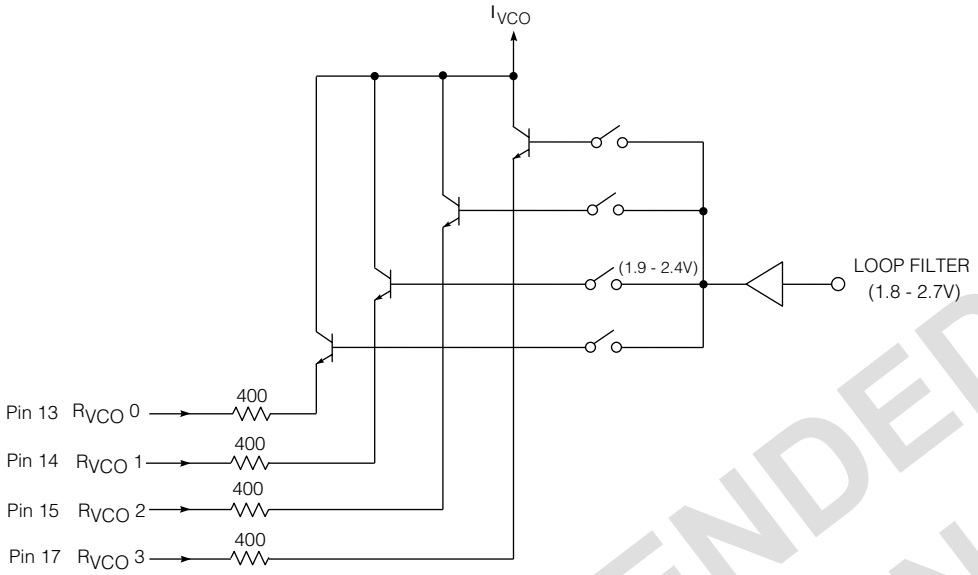



Fig. 4 Pins 13, 14, 15 and 17

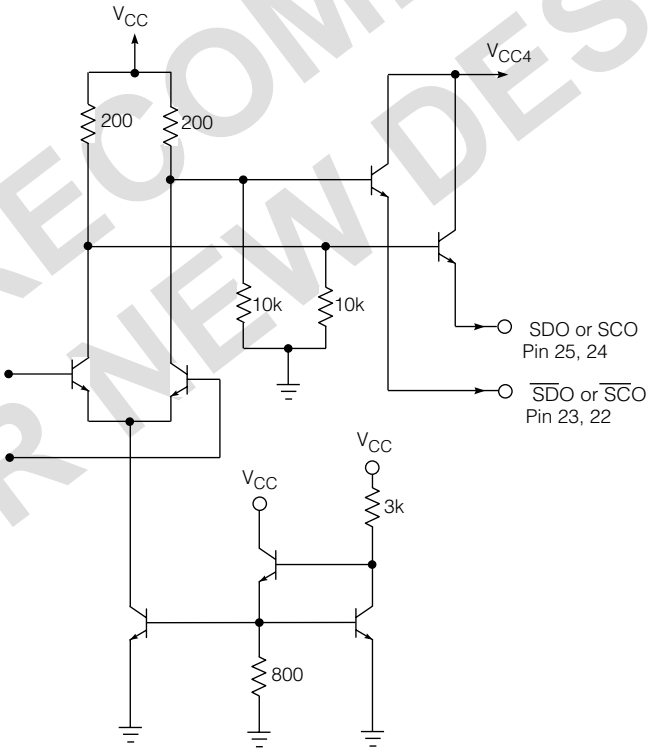



Fig. 5 Pins 25, 24, 23 and 22

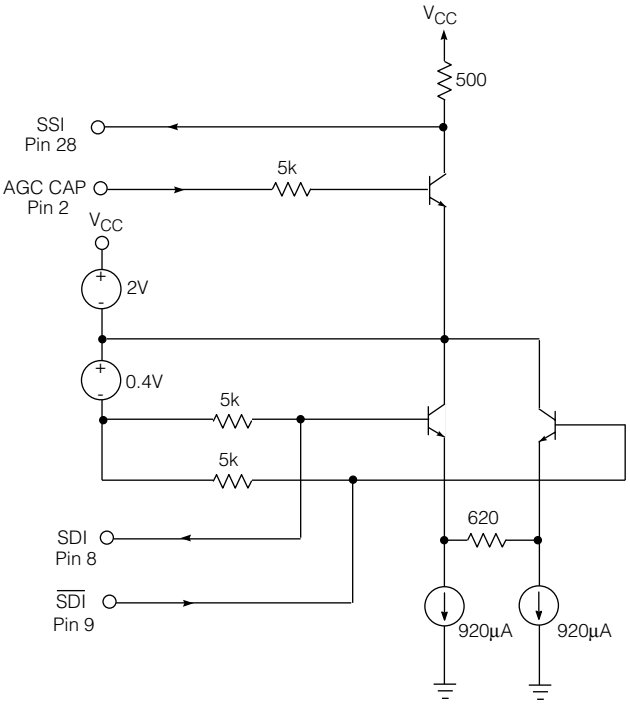



Fig. 6 Pins 28, 2, 8 and 9

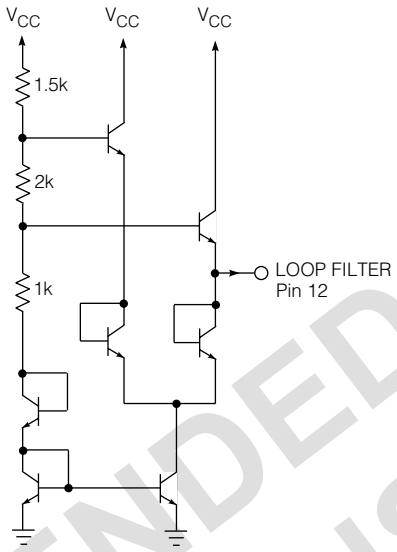



Fig. 7 Pin 12

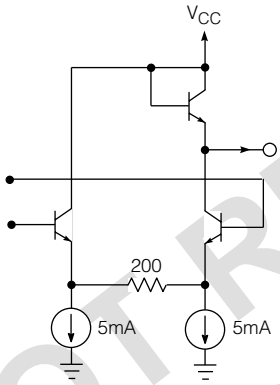



Fig. 8 Pin 16

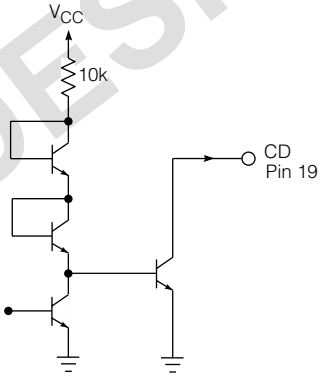



Fig. 9 Pin 19

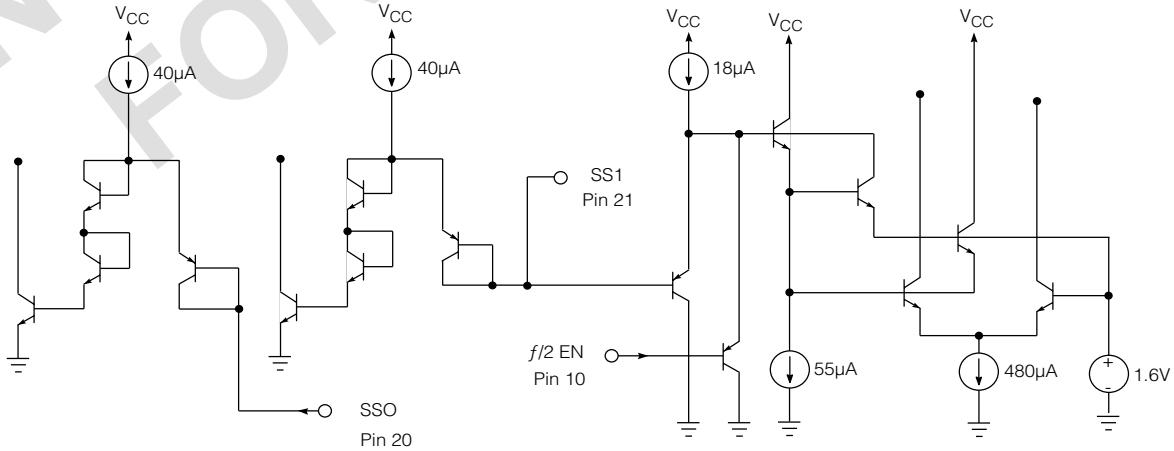



Fig. 10 Pins 20, 21 and 10

## TYPICAL PERFORMANCE CURVES

($V_S$ = 5V, $T_A$ = 25°C)

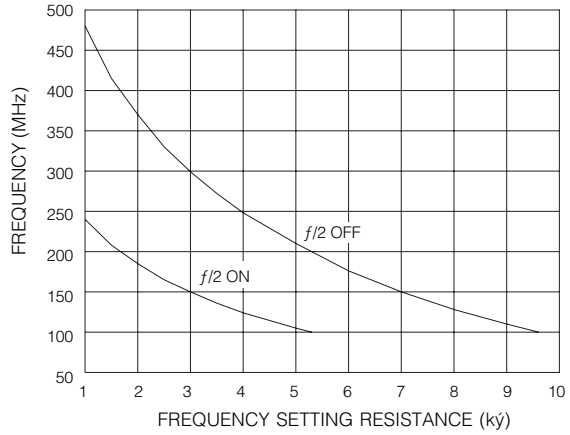



Fig. 11 Clock Frequency

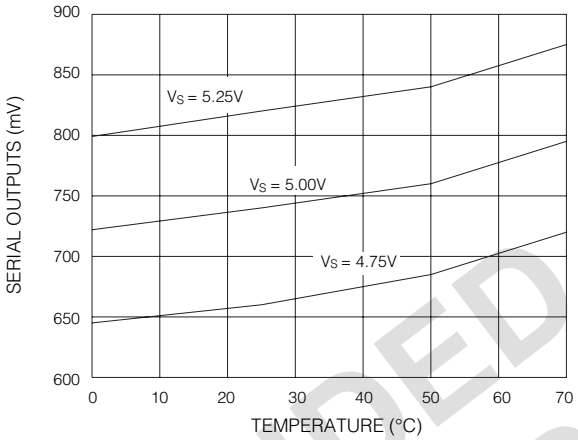



Fig. 12 Serial Outputs

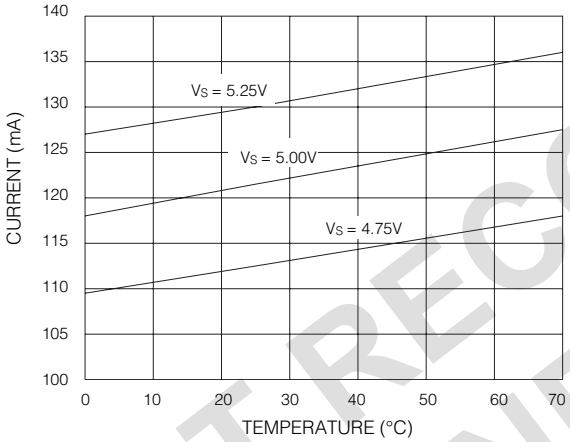



Fig. 13 Supply Current

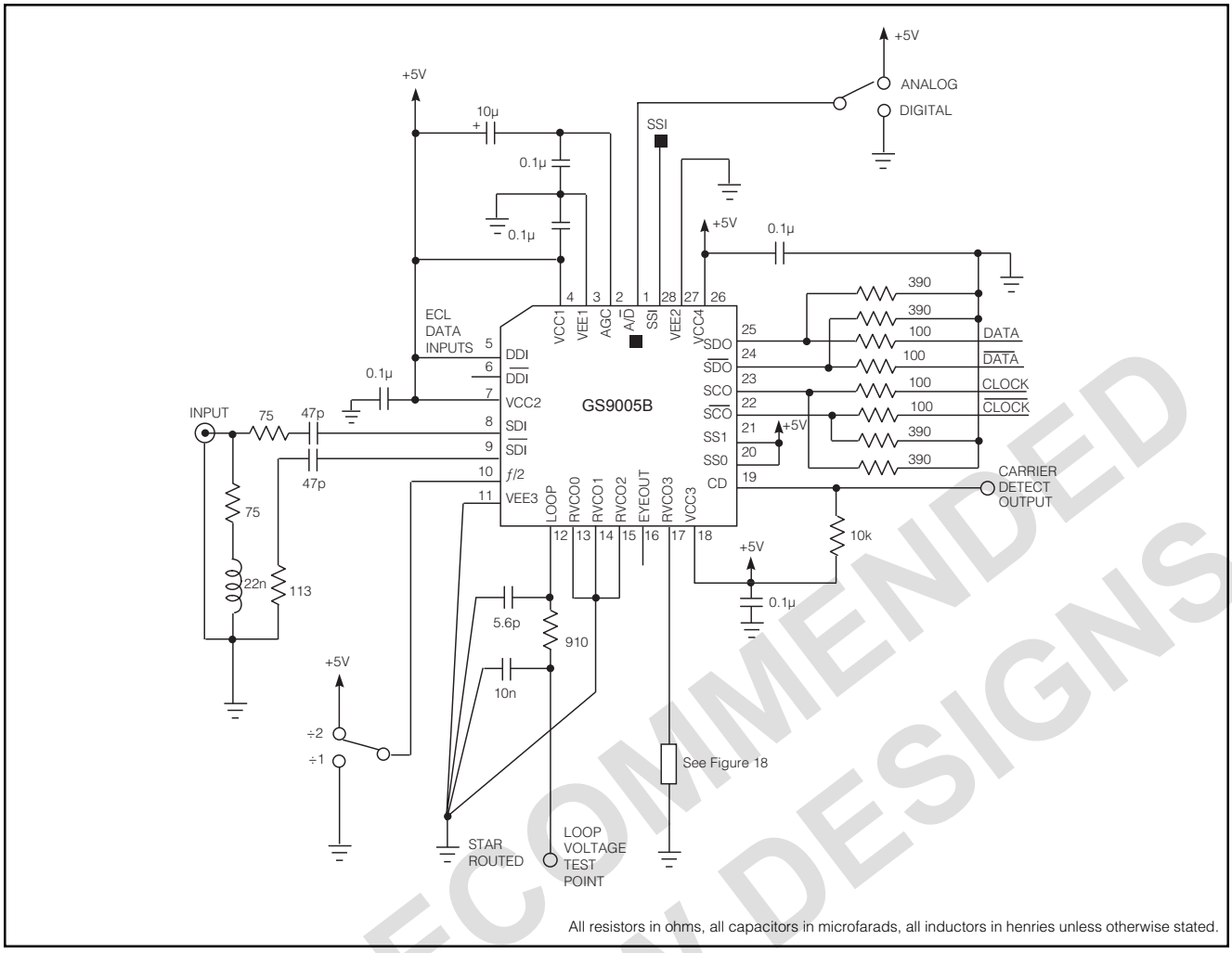



Fig.14 GS9005B Typical Test Circuit Using +5V Supply



## TEST SETUP

Figure 14 shows a typical circuit for the GS9005B using a +5 volt supply. The four 0.1µF decoupling capacitors must be placed as close as possible to the corresponding $V_{CC}$ pins.

The loop voltage can be conveniently measured across the 10nF capacitor in the loop filter. Tuning procedures are described in the Temperature Compensation Section (page 11). The fixed value frequency setting resistors should be placed close to the corresponding pins on the GS9005B.

The layout of the loop filter and RVCO components requires careful attention. This has been detailed in an application note entitled "Optimizing Circuit and Layout Design of the GS9005A/15A", Document No. 521 - 32 - 00.

When the Direct Digital Inputs are not used, one of these inputs should be connected to $V_{CC}$ to avoid picking up noise and unwanted signals.

The Carrier Detect is an open-collector active high output requiring a pull-up resistor of approximately 10 kΩ.

The SS0, SS1, CD pins should see a low AC impedance. This is particularly important when driving the SS0, SS1 pins with external logic. The use of 1 nF decoupling capacitors at these pins ensures this.

Figure 15 shows the GS9005B connections when using a -5 volt supply.

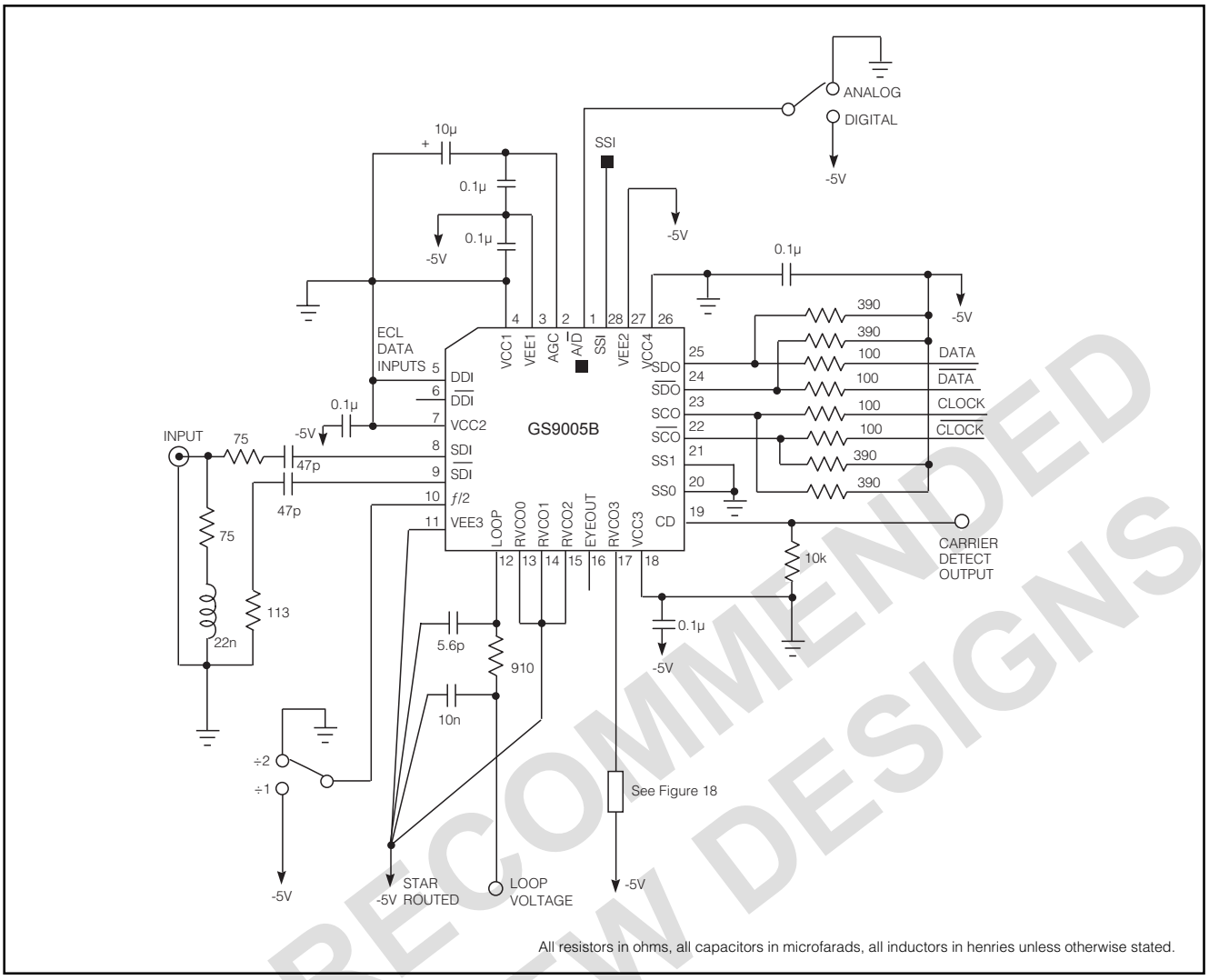



Fig. 15 GS9005B Typical Test Circuit Using -5V Supply



### VCO Frequency Setting Resistors

There are two modes of VCO operation available in the GS9005B. When the *ƒ*/2 ENABLE (pin 10) is LOW, any of the four VCO frequency setting resistors, RVCO0 through RVCO3 (pins 13, 14, 15 and 17) may be used for any data rate from 100 Mb/s to over 400 Mb/s. For example, for 143 Mb/s data rate, the value of the total $R_{VCO}$ resistance is approximately 6k8 and for 270 Mb/s operation, the value is approximately 3k5. The 5k potentiometers will then tune the desired data rate near their mid-points.

Jitter performance at the lower data rates (143, 177 Mb/s) is improved by operating the VCO at twice the normal frequency. This is accomplished by enabling the *ƒ*/2 function which activates an additional divide by two block in the PLL section of the GS9005B.

When the *ƒ*/2 ENABLE is HIGH two of the RVCO pins are assigned to data rates below 200 Mb/s and two are assigned to data rates over 200 Mb/s.

The selection is dependent upon the level of the STANDARD SELECT BIT, SS1 (pin 21). When SS1 is LOW, RVCO0 and RVCO1 (pins 13 and 14) are used for the higher data rates. When SS1 is HIGH, the VCO frequency is now twice the bit rate and its frequency is set by RVCO2 and RVCO3 (pins 15 and 17).

For 143 Mb/s and 270 Mb/s operation, (the VCO is at 286 MHz and 270 MHz respectively) the total resistance required is approximately the same for both data rates. This also applies for 177 Mb/s and 360 Mb/s operation (the VCO is tuned to 354 MHz and 360 MHz respectively). This means that one potentiometer may be used for each frequency pair with only a small variation of the fixed resistor value. This halves the number of adjustments required.

### Temperature Compensation

Figure 16 shows the connections for the frequency setting resistors for the various data rates. The compensation shown for 360 Mb/s and 177 Mb/s with Divide by 2 ON, is useful to a maximum ambient temperature of 50°C. If the Divide by 2 function is not enabled by the *f*/2 ENABLE input, no compensation is needed for the 143 Mb/s and 177 Mb/s data rates. The resistor connections are shown in Figure 17. In both cases, the 0.1 µF capacitor that bypasses the potentiometer should be star routed to VEE 3.

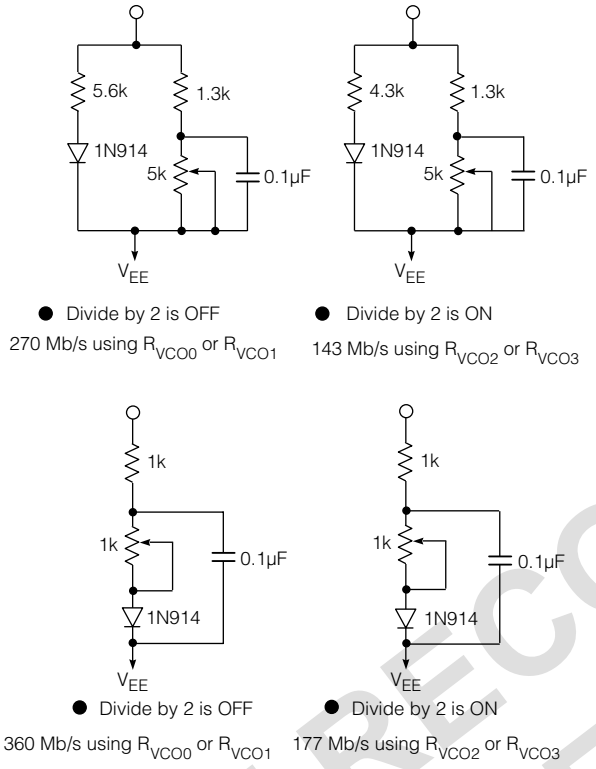



Fig. 16 Frequency Setting Resistor Values & Temperature Compensation

### Temperature Compensation Procedure

In order to correctly set the VCO frequency so that the PLL will always re-acquire lock over the full temperature range, the following procedure should be used. The circuit should be powered on for at least one minute prior to starting this procedure.

Monitor the loop filter voltage at the junction of the loop filter resistor and 10 nF loop filter capacitor (LOOP FILTER TEST POINT). Using the appropriate network shown above, the VCO frequency is set by first tuning the potentiometer so that the PLL loses lock at the low end (lowest loop filter voltage). The loop filter voltage is then slowly increased by adjusting the the potentiometer to determine the error free low limit of the capture range. Error free operation is determined by using a suitable CRC or EDH measurement method to obtain a stable signal with no errors. Record the loop filter voltage at this point as $V_{CL}$. Now adjust the potentiometer so that the loop filter voltage is 250 mV above $V_{CL}$.

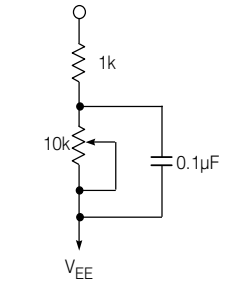



Fig. 17 Non - Temperature Compensated Resistor Values for 143 Mb/s and 177 Mb/s

### Loop Bandwidth

The loop bandwidth is dependant upon the internal PLL gain constants along with the loop filter components connected to pin 12. In addition, the impedance seen by the RVCO pin also influences the loop characteristics such that as the impedance drops, the loop gain increases.

### Applications Circuit

Figure 18 shows an application of the GS9005B in an adjustment free, multi-standard serial to parallel convertor. This circuit uses the GS9010A Automatic Tuning Subsystem IC and a GS9000B or GS9000S Decoder IC. The GS9005B may be replaced with a GS9015B Reclocker IC if cable equalization is not required.

The GS9010A ATS eliminates the need to manually set or externally temperature compensate the Receiver or Reclocker VCO. The GS9010A can also determine whether the incoming data stream is 4*f*sc NTSC,4*f*sc PAL or component 4:2:2.

The GS9010A includes a ramp generator/oscillator which repeatedly sweeps the Receiver VCO frequency over a set range until the system is correctly locked. An automatic fine tuning (AFT) loop maintains the VCO control voltage at it's centre point through continuous, long term adjustments of the VCO centre frequency.

When an interruption to the incoming data stream is detected by the Receiver, the Carrier Detect goes LOW and opens the AFT loop in order to maintain the correct VCO frequency for a period of at least 2 seconds. This allows the Receiver to rapidly relock when the signal is re-established.

During normal operation, the GS9000B or GS9000S Decoder provides continuous HSYNC pulses which disable the ramp/oscillator of the GS9010A. This maintains the correct Receiver VCO frequency.

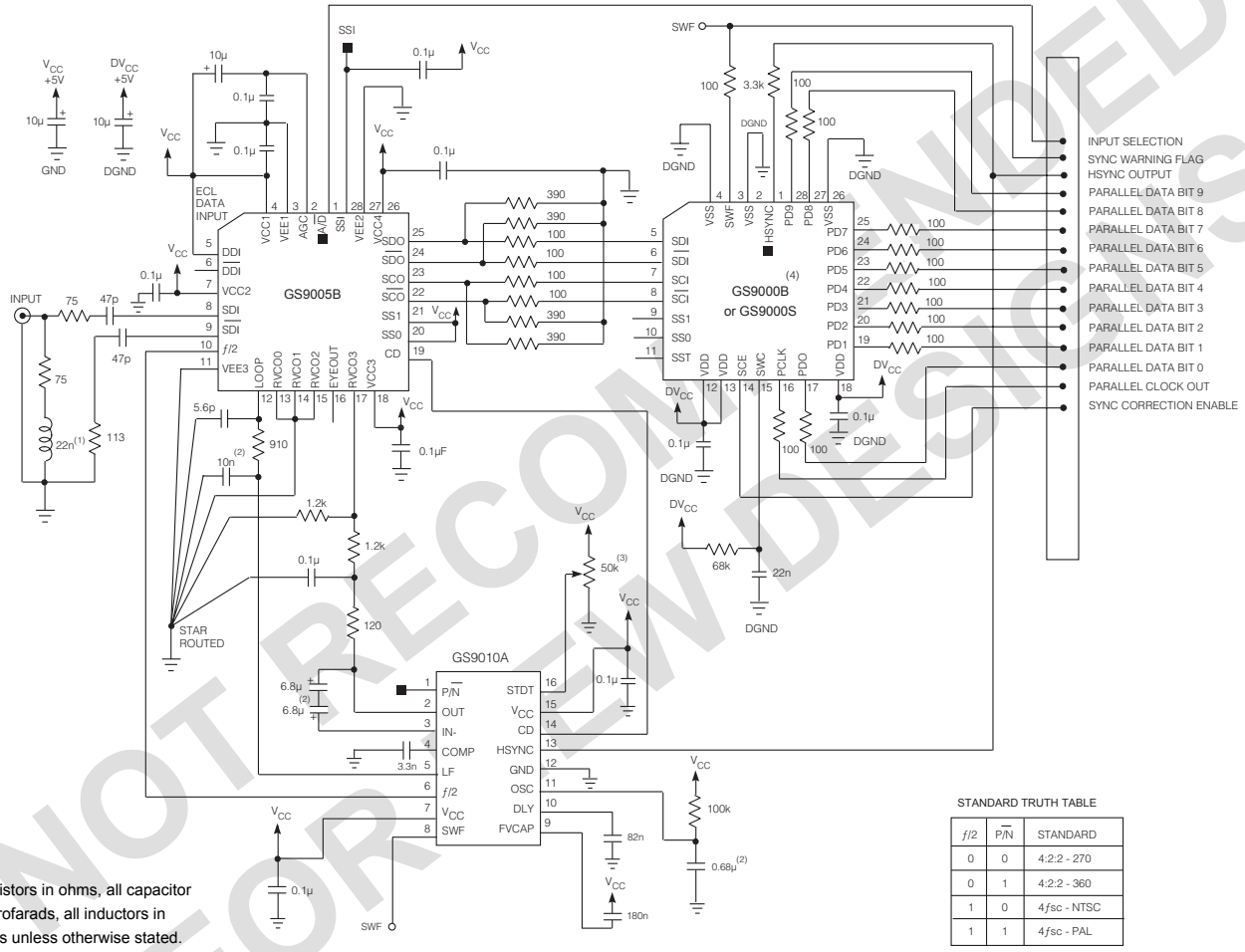
## Application Note - PCB Layout

Special attention must be paid to component layout when designing high performance serial digital receivers. For background information on high speed circuit and layout design concepts, refer to Document No. 521-32-00, “Optimizing Circuit and Layout Design of the GS90005A/15A”. A recommended PCB layout can be found in the Gennum Application Note “EB9010B Deserializer Evaluation Board.”

The use of a star grounding technique is required for the loop filter components of the GS9005B/15B.

Controlled impedance PCB traces should be used for the differential clock and data interconnection between the GS9005B and the GS9000B or GS9000S. These differential traces must not pass over any ground plane discontinuities. A slot antenna is formed when a microstrip trace runs across a break in the ground plane.

The series resistors at the parallel data output of the GS9000B or GS9000S are used to slow down the fast rise/fall time of the GS9000B or GS9000S outputs. These resistors should be placed as close as possible to the GS9000B or GS9000S output pins to minimize radiation from these pins.




All resistors in ohms, all capacitor in microfarads, all inductors in henries unless otherwise stated.

STANDARD TRUTH TABLE

| f/2 | P/N | STANDARD |
|---|---|---|
| 0 | 0 | 4:2:2 - 270 |
| 0 | 1 | 4:2:2 - 360 |
| 1 | 0 | 4fsc - NTSC |
| 1 | 1 | 4fsc - PAL |

(1) Typical value for input return loss matching

(2) To reduce board space, the two anti-series 6.8µF capacitors (connected across pins 2 and 3 of the GS9010A) may be replaced with a 1.0 µF non-polarized capacitor provided that:

(a) the 0.68 µF capacitor connected to the OSC pin (11) of the GS9010A is replaced with a 0.33 µF capacitor and

(b) the GS9005B/15B Loop Filter Capacitor is 10nF.

(3) Remove this potentiometer if P/N function is not required, and ground pin 16 of the GS9010A.

(4) The GS9000B will operate to a maximum frequency of 370 Mbps. The GS9000S will operate to a maximum frequency of 300 Mbps.

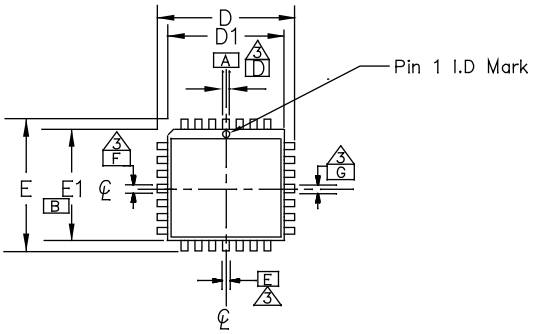
Fig. 18 Typical Application Circuit

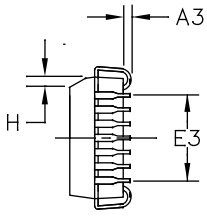
REVISION NOTES
New document.

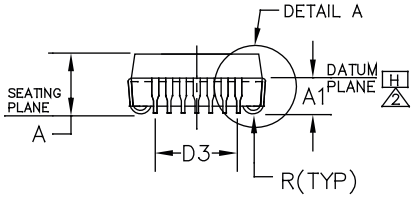
*For latest product information, visit www.gennum.com*

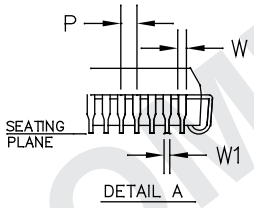
DOCUMENT IDENTIFICATION
PRODUCT PROPOSAL
This data has been compiled for market investigation purposes only, and does not constitute an offer for sale.
ADVANCE INFORMATION NOTE
This product is in development phase and specifications are subject to change without notice. Gennum reserves the right to remove the product at any time. Listing the product does not constitute an offer for sale.
PRELIMINARY
The product is in a preproduction phase and specifications are subject to change without notice.
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

# GS9005B Package Outline Drawing




| SYMBOL | 28 PLCC | |
|---|---|---|
| | MIN | MAX |
| A | 0.165 | 0.180 |
| A1 | 0.090 | 0.120 |
| A3 | 0.020 | 0.040 |
| D | 0.485 | 0.495 |
| D1 | 0.450 | 0.456 |
| D3 | 0.300 REF | |
| E | 0.485 | 0.495 |
| E1 | 0.450 | 0.456 |
| E3 | 0.300 REF | |
| H | 0.042 | 0.048 |
| P | 0.050 BSC | |
| R | 0.025 | 0.045 |
| W | 0.026 | 0.032 |
| W1 | 0.013 | 0.021 |

NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE [H] LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
3. DATUM [D-E] AND [F-G] TO BE DETERMINED AT DATUM PLANE [H].
4. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION ALLOWABLE PROTRUSION IS 0.010 PER SIDE DIMENSION D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
5. DETAILS OF PIN NO.1 IDENTIFICATION ARE OPTIONAL BUT LOCATED WITHIN THE ZONE INDICATED.
6. DATUM [A] AND [B] TO BE DETERMINED AT PLANE [H].



REVISION NOTES

November 2007 - Version 1
Added Package Outline Drawing (ECR #148311)

For latest product information, visit www.gennum.com

DOCUMENT IDENTIFICATION
PRODUCT PROPOSAL
This data has been compiled for market investigation purposes only, and does not constitute an offer for sale.
ADVANCE INFORMATION NOTE
This product is in development phase and specifications are subject to change without notice. Gennum reserves the right to remove the product at any time. Listing the product does not constitute an offer for sale.
PRELIMINARY
The product is in a preproduction phase and specifications are subject to change without notice.
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.