0.3A/0.6A Half-Bridge Gate Driver

General Description

The RT7020 is a high-voltage gate driver IC with dual outputs. The IC, together with an external bootstrap network, drives dual N-MOSFETs or IGBTs in a half-bridge configuration with input voltage rail up to 600V.

The IC is equipped with a "common-mode dV/dt noise canceling technique" to provide high dV/dt immunity which enables stable operation under high dV/dt noise circumstances. Two Under-Voltage Lockout (UVLO) functions continuously monitor the bias voltages on VCC and BOOT-to-LX for preventing malfunction when the bias voltages are lower than the specified threshold voltages. A dead time control prevents shoot-through of the external power MOSFETs. The logic level of the PWM signal input pins are compatible with standard TTL logic level for ease of interfacing with controlling devices.

Applications

- PDP Scan Driver
- Fluorescent Lamp Ballast
- SMPS
- Motor Driver

Features

- **Floating Channel Designed for Bootstrap Operation with Input Voltage up to 600V**
- **300mA/600mA Sourcing/Sinking Current**
- **High dV/dt Immunity : ±50V/ns**
- **V_{CC} and $V_{BOOT-LX}$ Supply Range from 10V to 20V**
- **Under-Voltage Lockout Functions for Both Channels**
- **Matched Propagation Delays Between Both Channels**
- **TTL Compatible Logic Input**
- **Internal Dead-Time Setting**
- **High-Side Output In-Phase with HIN Input Signal**
- **Low-Side Output Out of Phase with $\overline{\text{LIN}}$ Input Signal**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT7020□□

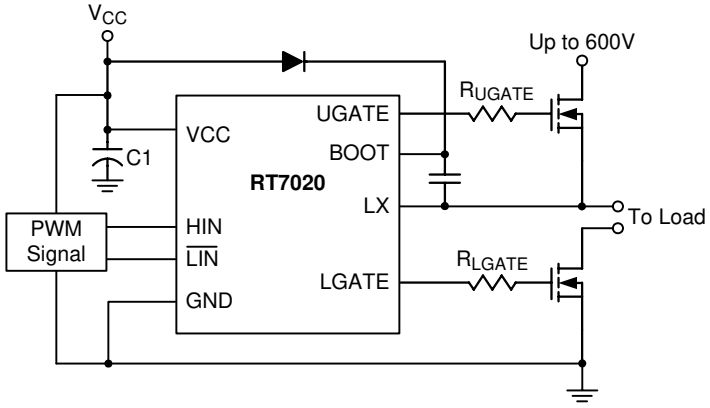
- Package Type
  - S : SOP-8
  - N : DIP-8
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

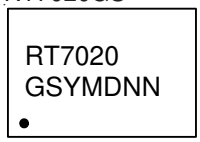
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit



Marking Information

RT7020GS



RT7020GS : Product Number

YMDNN : Date Code

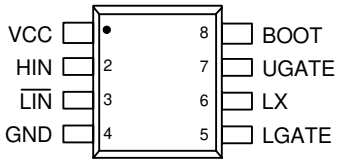
RT7020GN

RT7020GN : Product Number

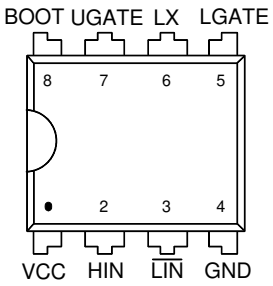
YMDNN : Date Code

Pin Configurations

(TOP VIEW)



SOP-8

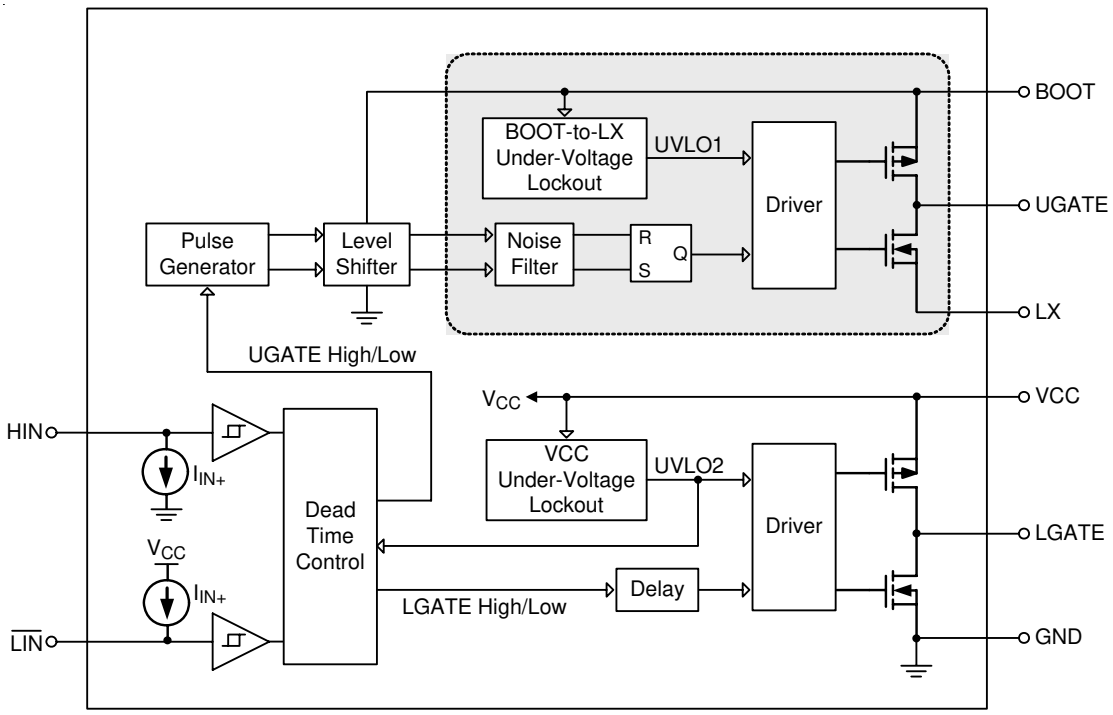


DIP-8

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-8	DIP-8		
1	1	VCC	Supply Voltage Input.
2	2	HIN	Logic Input for High-Side Gate Driver.
3	3	$\overline{\text{LIN}}$	Logic Input for Low-Side Gate Driver.
4	4	GND	Logic Ground and Low-Side Driver Return.
5	5	LGATE	Low-Side Driver Output.
6	6	LX	Return for High-Side Gate Driver.
7	7	UGATE	High-Side Driver Output.
8	8	BOOT	Bootstrap Supply for High-Side Gate Driver.

Function Block Diagram



Operation

The RT7020 is a high-voltage gate driver for driving high-side and low-side MOSFETs in a half-bridge configuration. The RT7020 uses ultra high voltage device and floating well to allow UGATE to drive external MOSFET operating up to 600V. When the HIN voltage is above the logic-high threshold, the UGATE voltage goes to turn on the external MOSFET. When the HIN voltage is below the logic-low threshold, the MOSFET is turned off.

The operating behavior of the LGATE, controlled by the $\overline{\text{LIN}}$ pin, is like the behavior of the UGATE.

Under-Voltage Lockout (UVLO) Function

When the VCC or BOOT-to-LX voltage is lower than the UVLO threshold, the UGATE and LGATE output will be disabled.

Pulse Generator

The pulse generator is used to transmit the HIN input signal to the UGATE driver.

Dead-Time Control

The dead-time control function is designed to prevent the high-side and low-side MOSFETs form shoot-through.

Absolute Maximum Ratings (Note 1)

- VCC Supply Voltage, V_{CC} ---------- –0.3 to 25V
- LX to GND ---------- –0.3V to 625V
- BOOT to LX, $V_{BOOT-LX}$ ---------- –0.3V to 25V
- UGATE to LX ---------- –0.3V to $V_{BOOT-LX}$ + 0.3V
- LGATE to GND ---------- –0.3V to V_{CC} + 0.3V
- HIN, $\overline{LIN}$ to GND ---------- –0.3V to V_{CC} + 0.3V
- Allowable LX Voltage Slew Rate,dV_{LX}/dt ---------- –50V/ns to 50V/ns
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 ---------- 0.53W
  - DIP-8 ---------- 0.74W
- Package Thermal Resistance (Note 2)
  - SOP-8, θ_{JA} ---------- 188°C/W
  - DIP-8, θ_{JA} ---------- 134.9°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

Recommended Operating Conditions (Note 3)

- VCC Supply Voltage, V_{CC} ---------- 10V to 20V
- BOOT-to-LX, $V_{BOOT-LX}$ ---------- 10V to 20V
- LX to GND ---------- 0 to 600V
- UGATE to LX ---------- 0 to $V_{BOOT-LX}$
- LGATE to GND ---------- 0 to V_{CC}
- HIN, $\overline{LIN}$ to GND ---------- 0 to V_{CC}
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = $V_{BOOT-LX}$ = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} Under-Voltage Lockout Threshold (On)	V_{THON_VCC}		9	10.5	12	V
$V_{BOOT-LX}$ Under-Voltage Lockout Threshold (On)	V_{THON_BOOT}		9	10.5	12	V
V_{CC} Under-Voltage Lockout Threshold (Off)	V_{THOFF_VCC}		8	9.5	11	V
$V_{BOOT-LX}$ Under-Voltage Lockout Threshold (Off)	V_{THOFF_BOOT}		8	9.5	11	V
V_{CC} Under-Voltage Lockout Hysteresis	V_{HYS_VCC}		--	1	--	V
$V_{BOOT-LX}$ Under-Voltage Lockout Hysteresis	V_{HYS_BOOT}		--	1	--	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
LX Leakage Current		I_{LK}	V_{BOOT} = V_{LX} = 600V	--	--	50	μA
VCC Quiescent Current		I_{Q_VCC}		--	220	400	μA
BOOT-to-LX Quiescent Current		$I_{Q\_BOOT-LX}$		--	100	200	μA
VCC Operating Current		I_{P_VCC}	Frequency = 20kHz, UGATE = LGATE = Open	--	--	600	μA
BOOT-to-LX Operating Current		$I_{P\_BOOT-LX}$		--	--	600	μA
HIN, $\overline{LIN}$ Input Voltage	Logic-High	V_{IH}		2.5	--	--	V
	Logic-Low	V_{IL}		--	--	0.8	
UGATE, LGATE Output Voltage	High-Level	V_{OH}	Sinking Current = 2mA, V_{BOOT} – V_{UGATE}, V_{CC} – V_{LGATE}	--	50	200	mV
	Low-Level	V_{OL}	Sinking Current = 2mA, $V_{UGATE-LX}$, V_{LGATE}	--	20	100	
HIN Input Current	Logic-High	I_{IN+}	HIN = VCC, $\overline{LIN}$ = GND	--	2	10	μA
	Logic-Low	I_{IN-}	HIN = GND, $\overline{LIN}$ = VCC	–1	--	--	
UGATE and LGATE Sourcing Current		I_{O+}	UGATE = LX, LGATE = GND, Current pulse width < 10μs, Low duty	--	290	--	mA
UGATE and LGATE Sinking Current		I_{O-}	UGATE = LX, LGATE = GND, Current pulse width < 10μs, Low duty	--	600	--	

Dynamic Electrical Characteristics (Note 4)

(V_{CC} = $V_{BOOT-LX}$ = 15V, LX = GND, C_L = 1000pF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-on Delay	t_{ON}		--	680	820	ns
Turn-off Delay	t_{OFF}	V_{LX} = 0 or 600V (Note 5)	--	150	300	ns
Turn-on Rising Time	t_R		--	70	170	ns
Turn-off Falling Time	t_F		--	35	90	ns
Dead-Time	t_{Dead}		--	520	650	ns

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

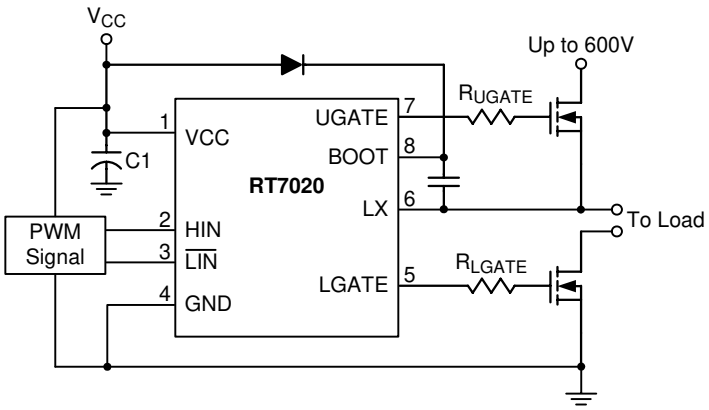
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. The device is not guaranteed to function outside its operating conditions.

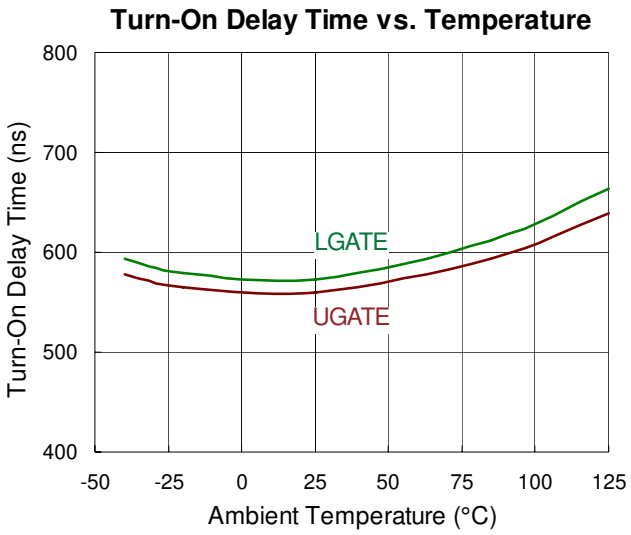
Note 4. Please refer to the Timing Diagram and Dynamic Waveforms in the Application Information.

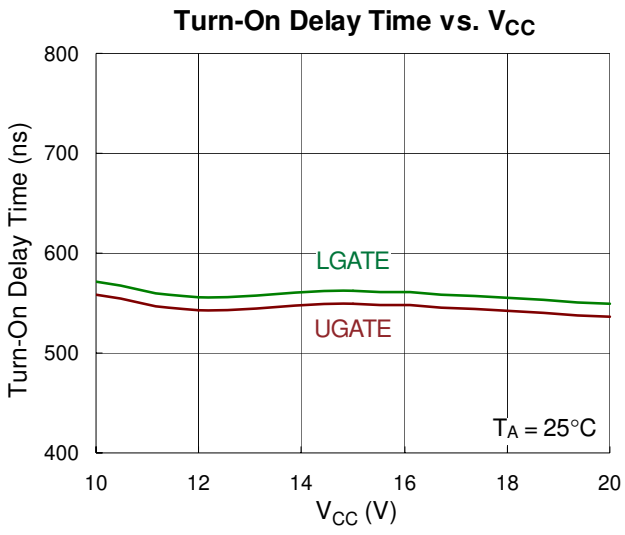
Note 5. Turn-off Delay for V_{LX} = 600V is guaranteed by design.

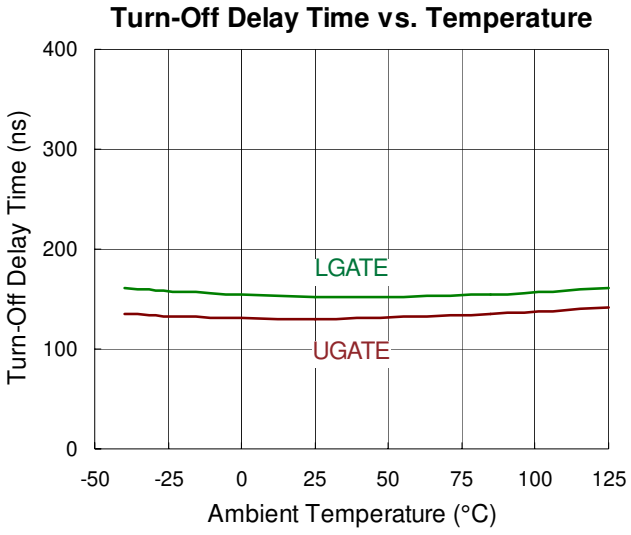
Typical Application Circuit

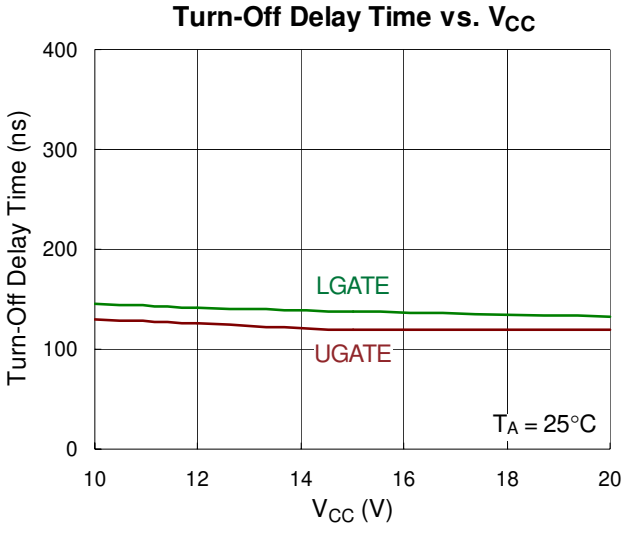


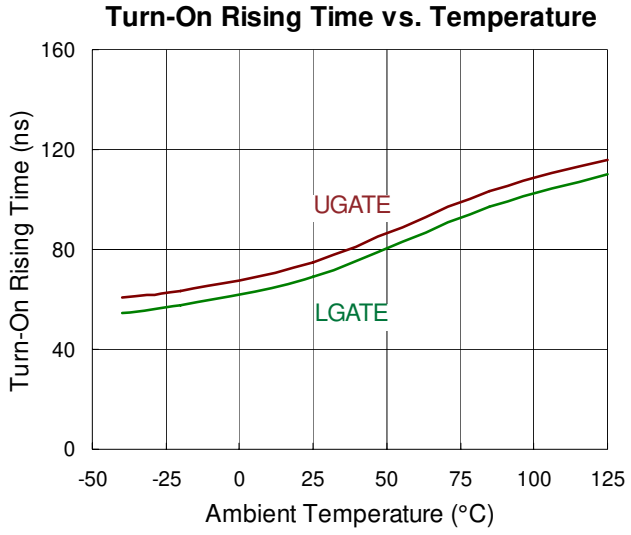
Typical Operating Characteristics

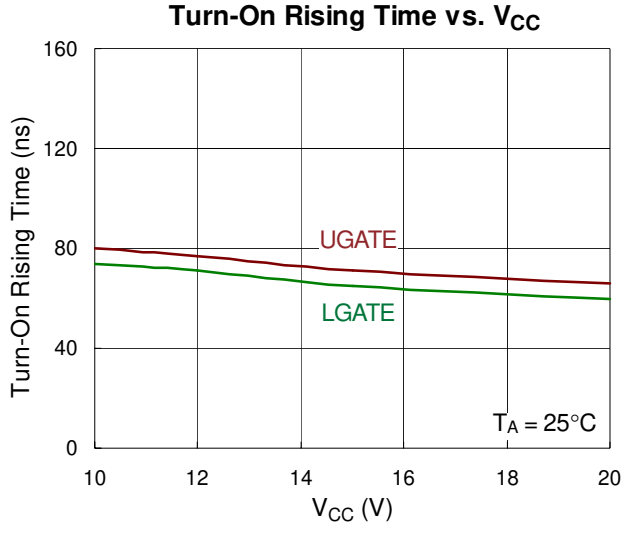




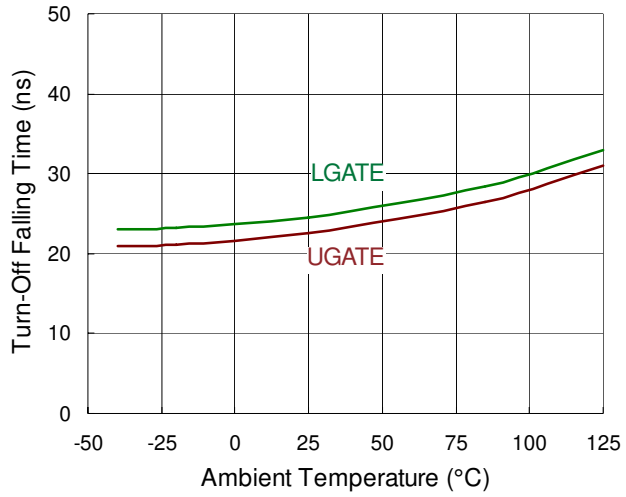




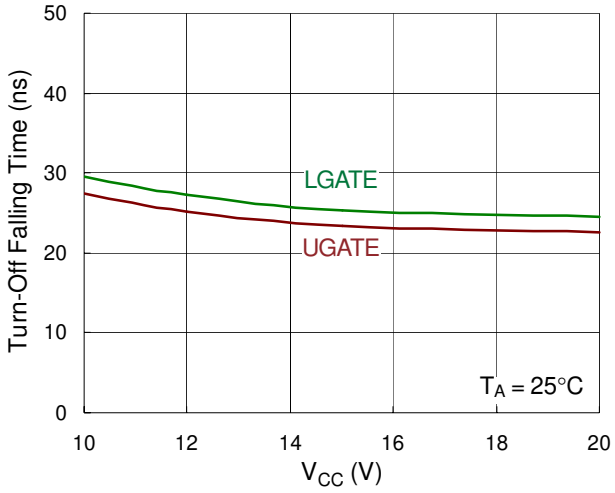




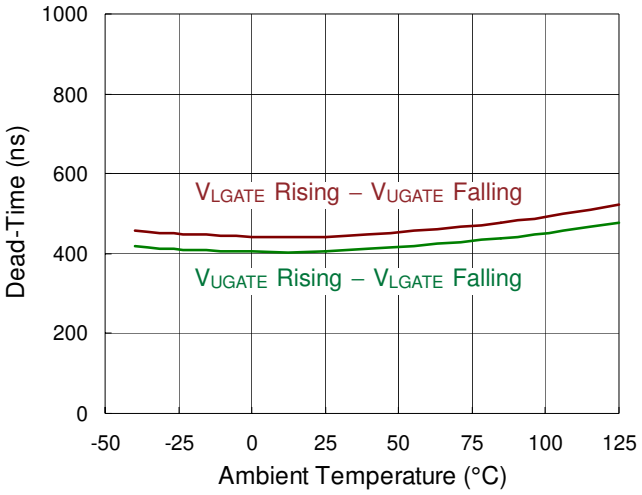
Turn-Off Falling Time vs. Temperature



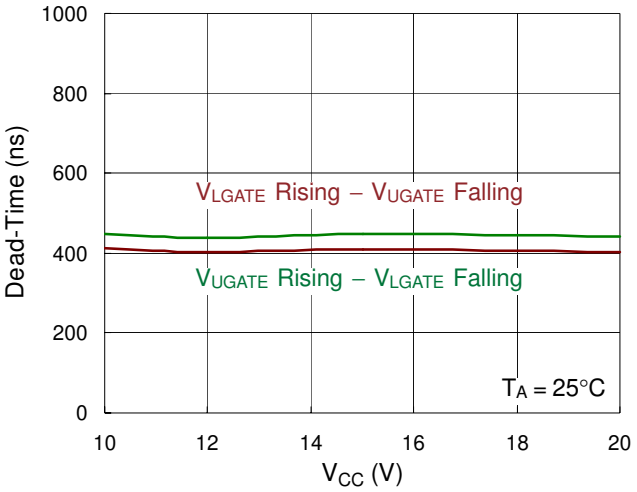
Turn-Off Falling Time vs. V_{CC}



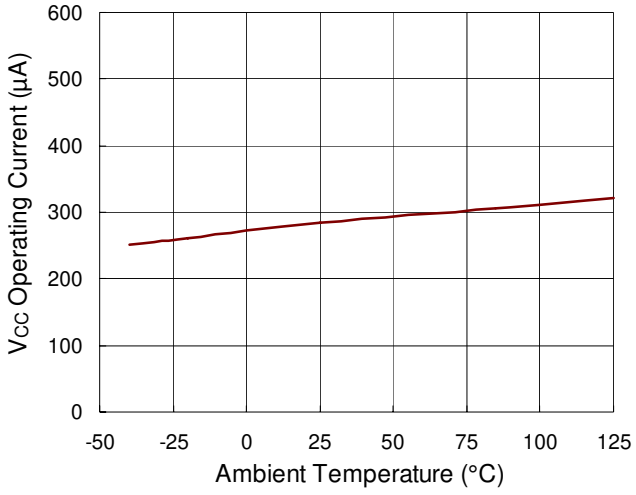
Dead-Time vs. Temperature



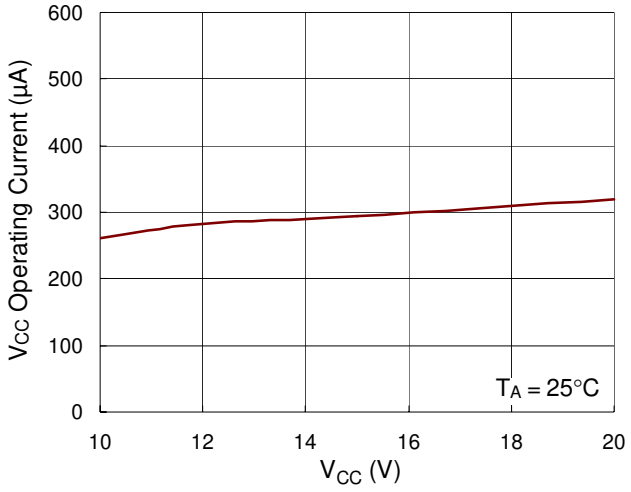
Dead-Time vs. V_{CC}



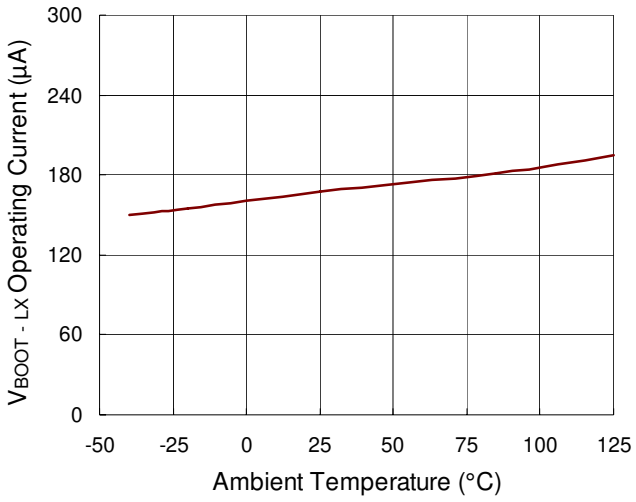
V_{CC} Operating Current vs. Temperature



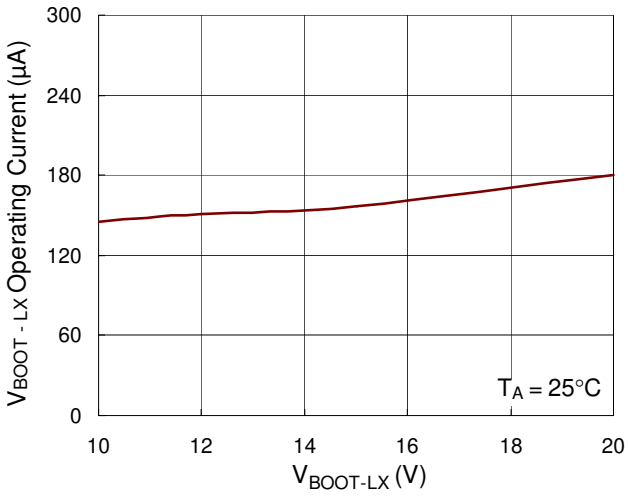
V_{CC} Operating Current vs. V_{CC}



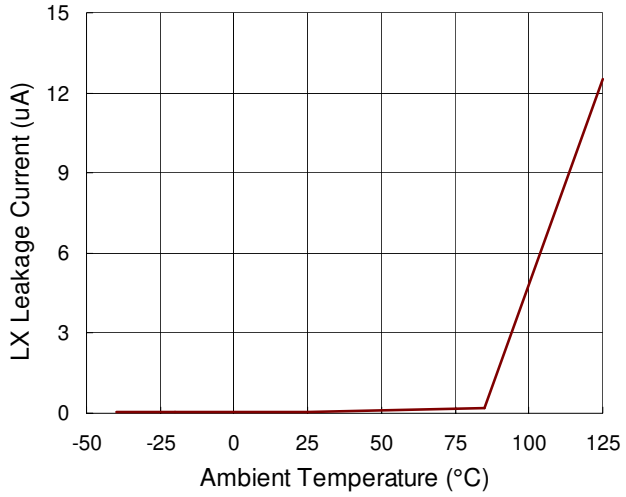
$V_{BOOT-LX}$ Operating Current vs. Temperature



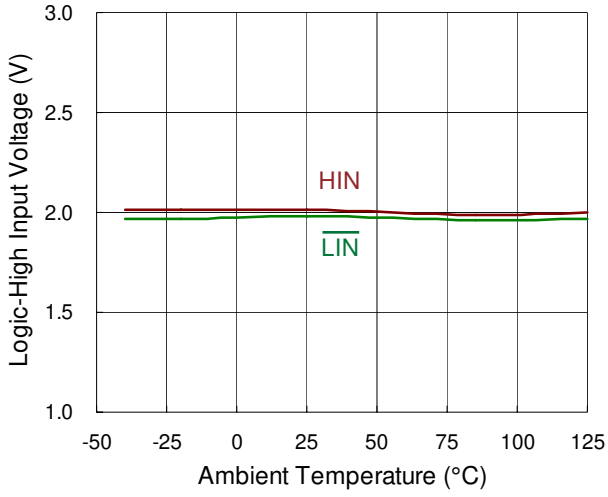
$V_{BOOT-LX}$ Operating Current vs. $V_{BOOT-LX}$



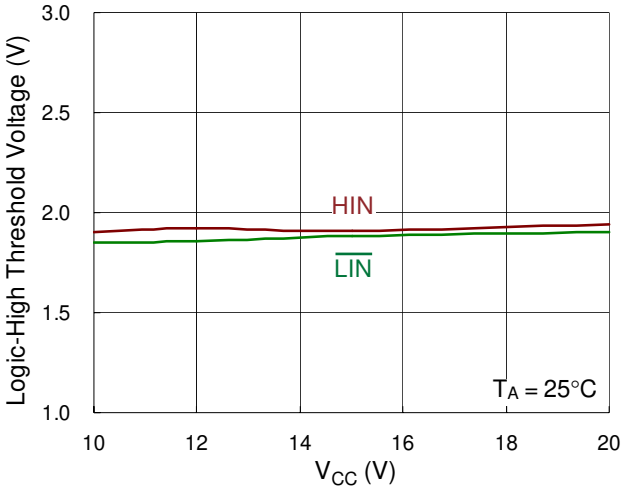
LX Leakage Current vs. Temperature



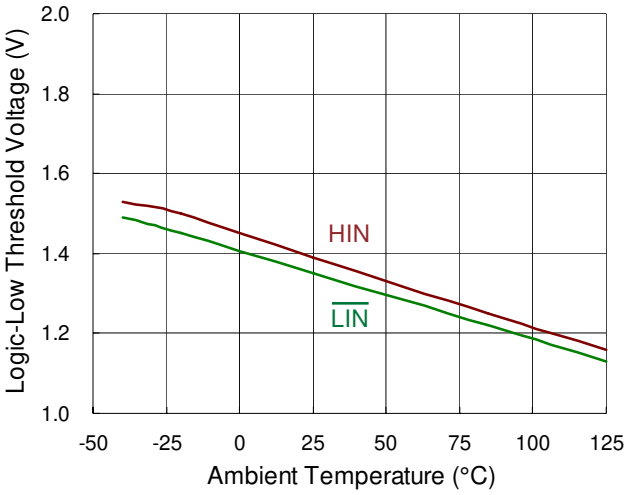
Logic-High Threshold Voltage vs. Temperature



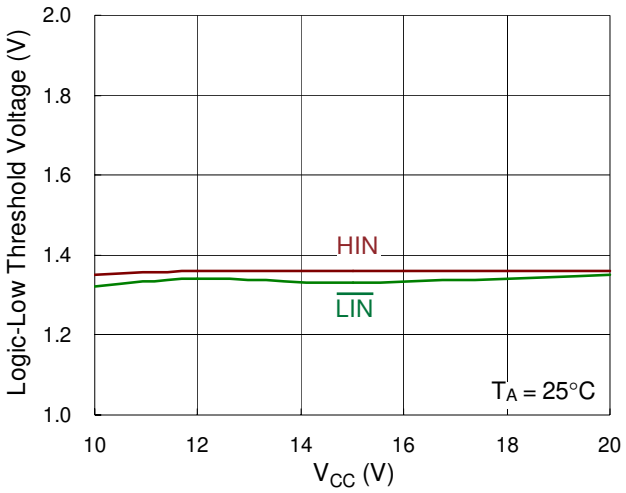
Logic-High Threshold Voltage vs. V_{CC}



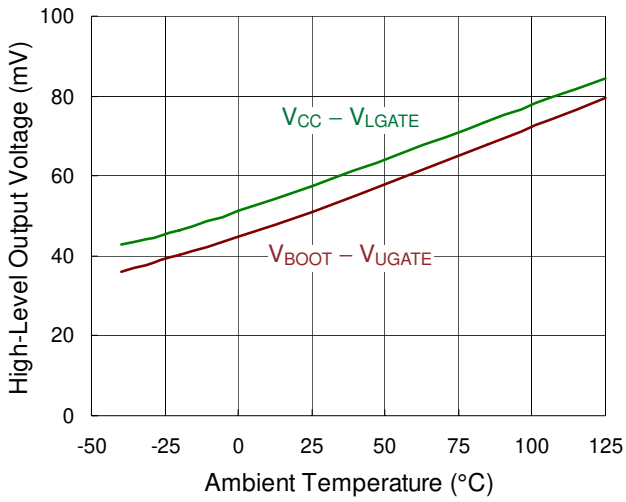
Logic-Low Threshold Voltage vs. Temperature



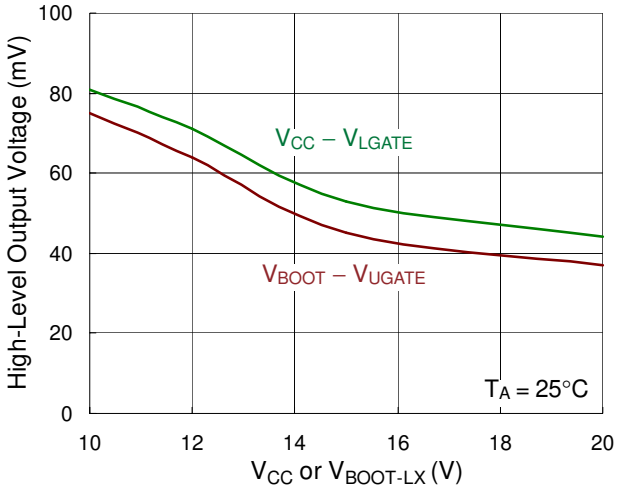
Logic-Low Threshold Voltage vs. V_{CC}



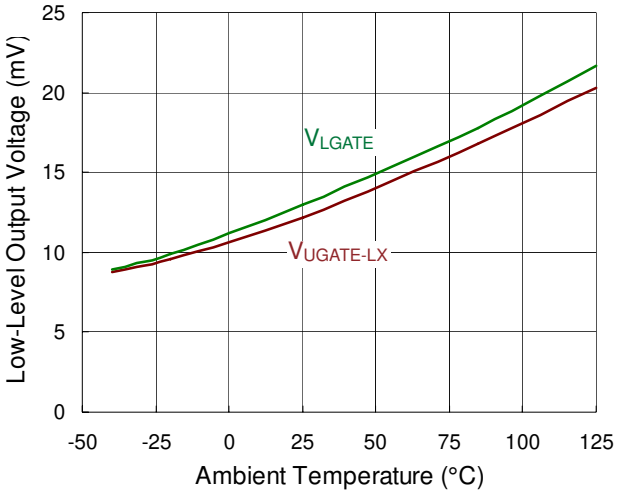
High-Level Output Voltage vs. Temperature



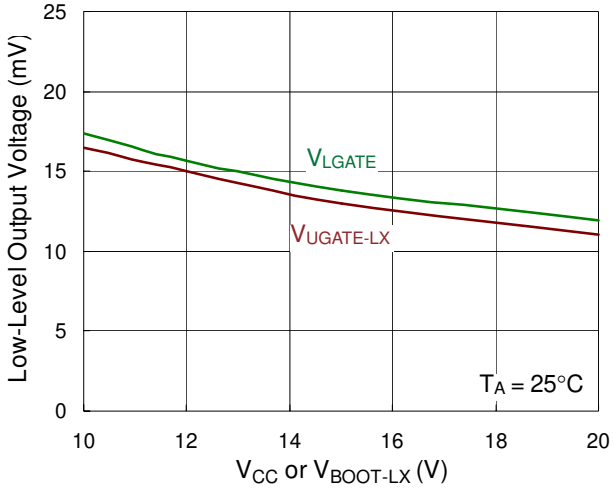
High-Level Output Voltage vs. V_{CC} or $V_{BOOT-LX}$



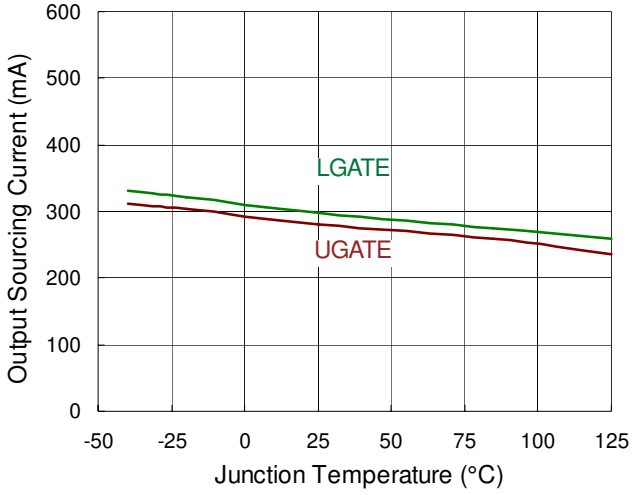
Low-Level Output Voltage vs. Temperature



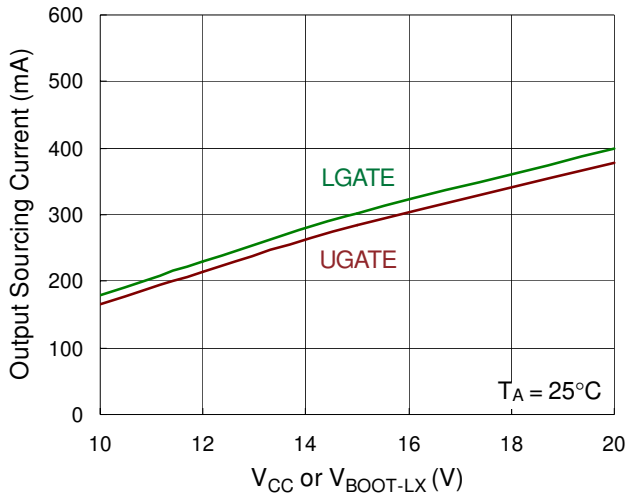
Low-Level Output Voltage vs. V_{CC} or $V_{BOOT-LX}$



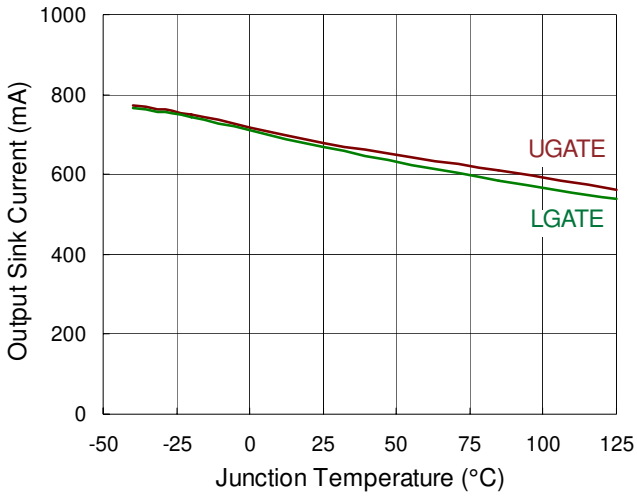
Output Sourcing Current vs. Temperature



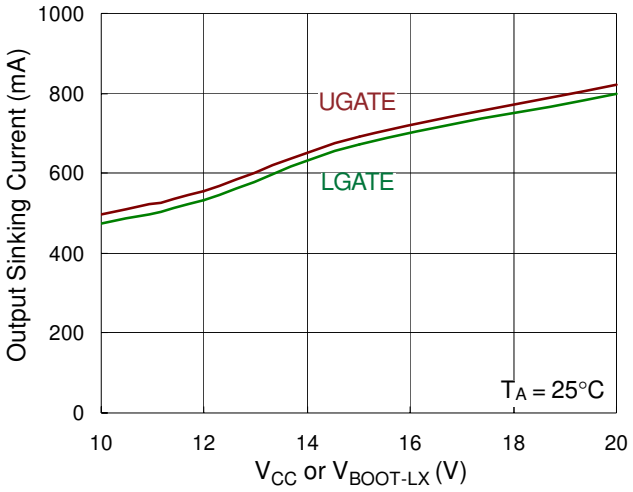
Output Sourcing Current vs. V_{CC} or $V_{BOOT-LX}$



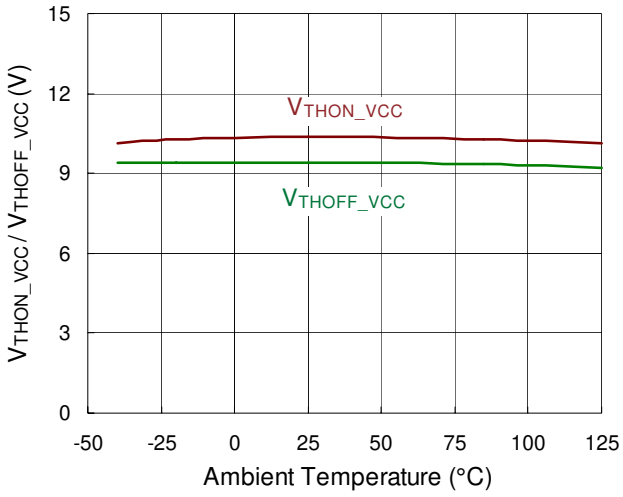
Output Sinking Current vs. Temperature



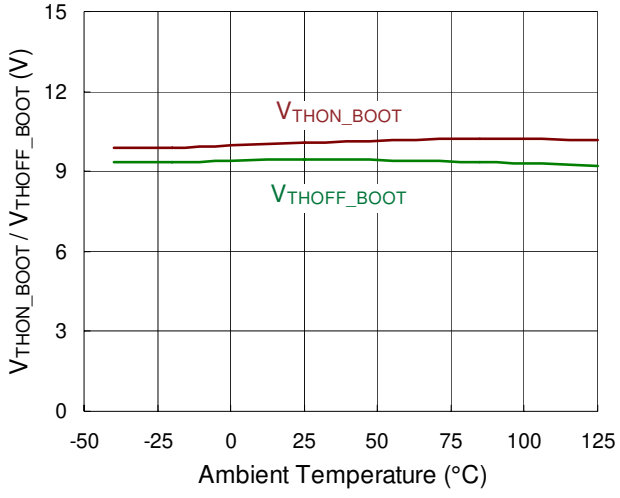
Output Sinking Current vs. V_{CC} or $V_{BOOT-LX}$



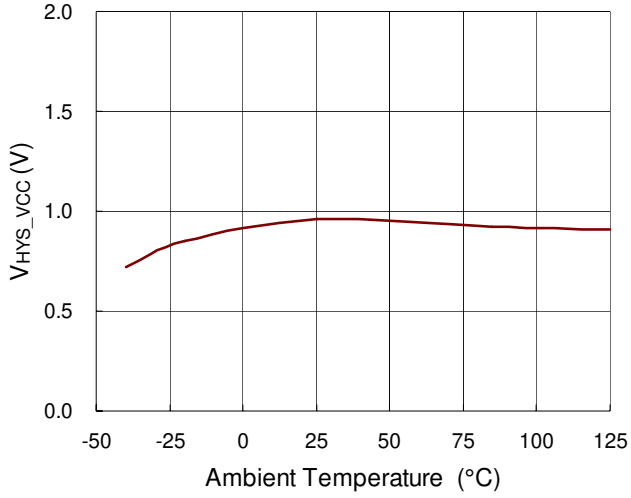
V_{THON_VCC} / V_{THOFF_VCC} vs. Temperature

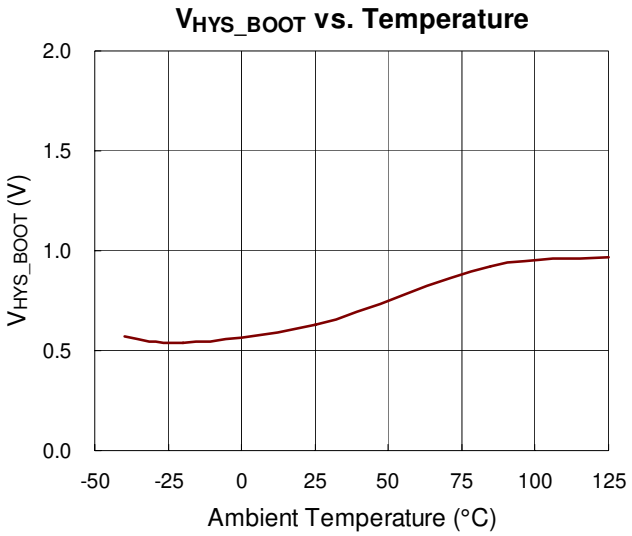


V_{THON_BOOT} / V_{THOFF_BOOT} vs. Temperature



V_{HYS_VCC} vs. Temperature





Application Information

Timing Diagram and Dynamic Waveforms

Figure 1 is the RT7020 input/output timing diagram, and Figure 2 is a definition of dynamic characteristics. You can know those definitions and the relationship between input and output from these figures. For example : t_{ON}, t_{OFF}, t_R, t_F...

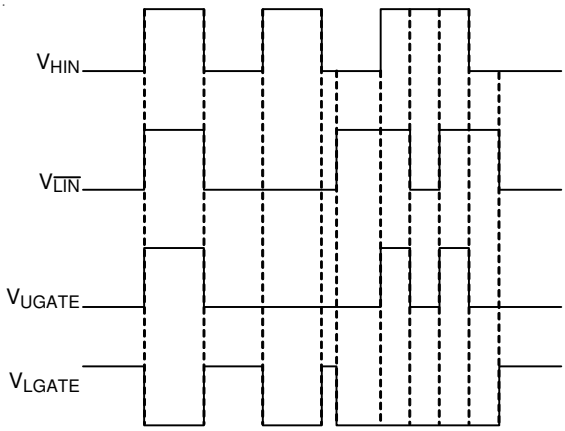


Figure 1. Input/Output Timing Diagram

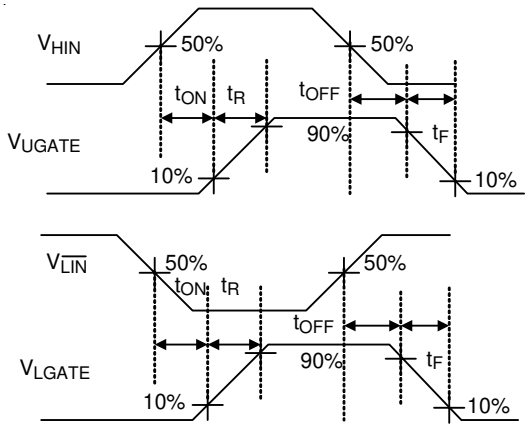


Figure 2. Dynamic Electrical Characteristics Definition

Deadtime, t_{Dead}

To avoid the simultaneous conduction of high-side and low-side power switches cause shoot through, the switching operation of the IC control circuit introduces a deadtime function. In the deadtime period, even if the input sends another power switch conduction signal, the control circuit will remain closed drive state. Figure 3 illustrates the definition of deadtime and the relationship between the high-side and low-side gate signals.

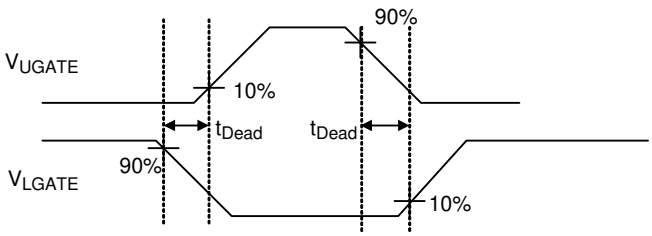


Figure 3. Deadtime Definition

Matched Propagation Delays between Both Channels

Because the IC internal level shifter circuit causes the propagation delay of the high-side output signal, shown in Figure 4. The RT7020 adds a propagation delay matching circuit in the low-side logic circuit, so that high-side and low-side output signals approximately synchronization.

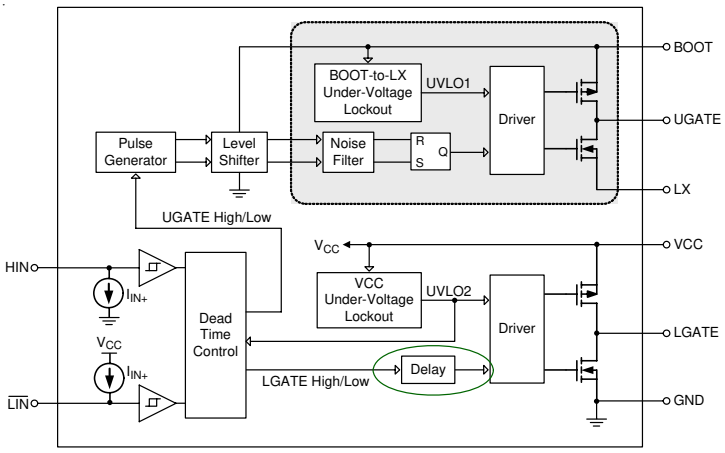


Figure 4. Propagation Delay Matching Circuit

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 package, the thermal resistance, θ_{JA}, is 188°C/W on a standard JEDEC 51-7 four-layer thermal test board.For DIP-8 package, the thermal resistance, θ_{JA}, is 134.9°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (188°C/W) = 0.53W for SOP-8 package

$P_{D(MAX)}$ = (125°C − 25°C) / (134.9°C/W) = 0.74W for DIP-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

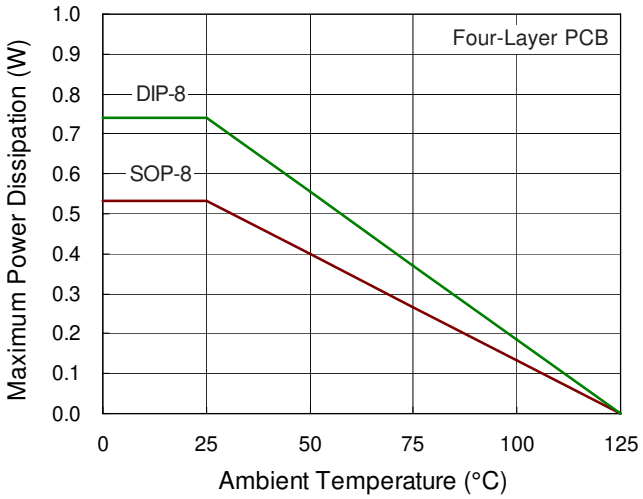


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Consideration

A proper PCB layout for power supply can reduce unnecessary waveform noise and electromagnetic interference problems to ensure proper system operation, please refer to the following PCB layout considerations:

- For the high voltage and high current loop layout of power supply should be as thick and short. Avoid excessive layout generated parasitic inductance and resistors to cause significant noise.
- In order to shorten the length of IC layout, you need to consider the relative placement for IC and the power switches. It is recommended that the power switches placed in a symmetrical manner, and the IC close to high-side and low-side elements.
- In order to reduce the noise coupling, it is recommended that the ground layout should not be placed under or near the high voltage floating side.
- The layout between high-side and low-side power switches should be thick and straight, avoiding the formation of long loops. Too long distance will increase the loop area, and electromagnetic interference suppression capabilities would be affected. However, too short distance may cause overheating situation. It is necessary to consider the most appropriate way.
- Refer to typical application circuit, the VCC capacitor (C1), BOOT to LX capacitor (C_{BOOT}), and bootstrap diode (D_{BOOT}) need to be placed as close to the IC as possible to minimize parasitic inductance and resistance. The C_{BOOT} selected range is from 0.1µF to 0.47µF, and the VCC capacitor (C1) is greater than ten times C_{BOOT}. It is recommended to use fast or ultra fast reverse recovery time bootstrap diode D_{BOOT}.
- In Figure 5, the LX pin voltage drop can be improved by adding R_{LX} (R_{LX} = 1 to 10Ω), because the dv/dt is affected by (R_{LX} + R_{UGATE}).

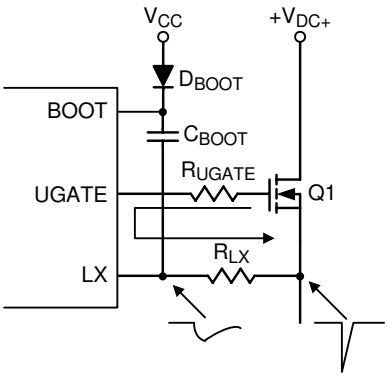


Figure 5. LX Pin Resister

- If the gate current loop opens circuit for some factors, at this time, the current flows through the gate loop via the power MOSFET drain-to-gate parasitic capacitor. The current will charge the gate-to-source parasitic capacitor to result in power MOSFET wrong action. The power switches can be damaged or burned out, the resisters (about least 10kΩ) are connected between the gate and source pin can prevent malfunction of the power switches.
- The selection of larger parasitic capacitor power switch or gate resister may result in too long turn-off time making the high-side and low-side power switches shoot through. In order to prevent the situation, reverse parallel with diodes (D_{UGATE} & D_{LGATE}) in the R_{UGATE} and R_{LGATE} (shown in Figure 6), providing a fast discharge path for the power switches in a short time to complete the closing operation.

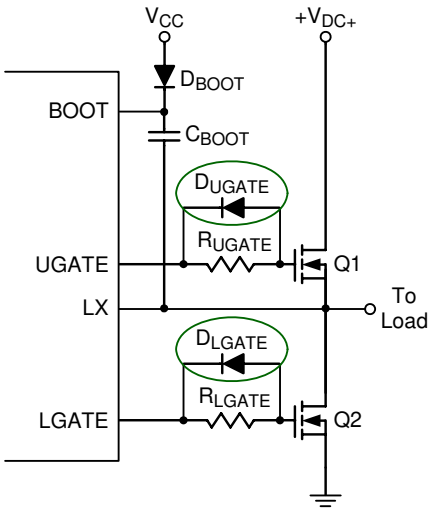
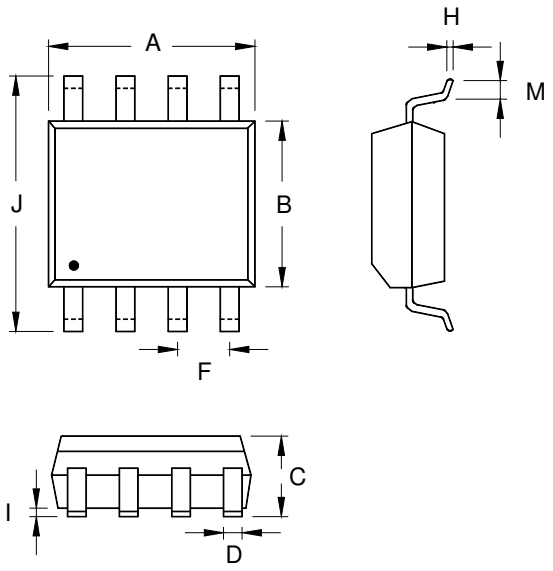


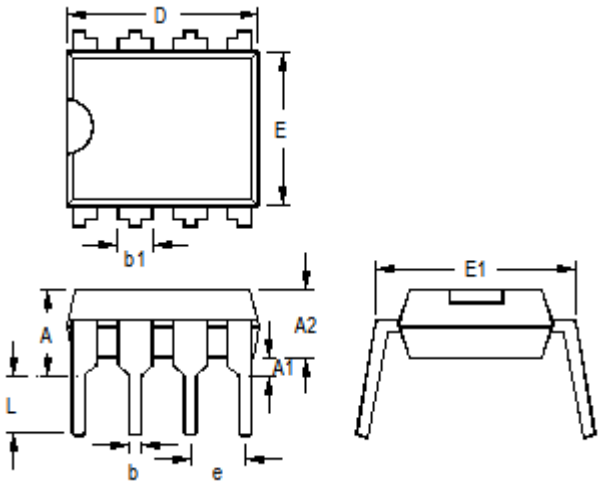
Figure 6. Reverse Parallel with Diodes

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.700	4.320	0.146	0.170
A1	0.381	0.710	0.015	0.028
A2	3.200	3.600	0.126	0.142
b	0.360	0.560	0.014	0.022
b1	1.143	1.778	0.045	0.070
D	9.050	9.550	0.356	0.376
E	6.200	6.600	0.244	0.260
E1	7.620	8.255	0.300	0.325
e	2.540		0.100	
L	3.000	3.600	0.118	0.142

8-Lead DIP Plastic Package

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