KSZ8862-16M/-32M

Two-Port Ethernet Switch with Non-PCI Interface and Fiber Support

Features

Switch Management

- Non-Blocking Switch Fabric Assures Fast Packet Delivery by Utilizing a 1K Entry Forwarding Table and a Store-and-Forward Architecture
- Fully Compliant with IEEE 802.3u Standards
- Full-Duplex IEEE 802.3x Flow Control (Pause) with Force Mode Option
- Half-Duplex Back Pressure Flow Control

Advanced Switch Management

- IEEE 802.1Q VLAN Support for Up to 16 Groups (Full Range of VLAN IDs)
- VLAN ID Tag/Untag Options, on a Per Port Basis
- IEEE 802.1p/Q Tag Insertion or Removal on a Per Port Basis (Egress)
- Programmable Rate Limiting at the Ingress and Egress Ports
- Broadcast Storm Protection
- IEEE 802.1d Spanning Tree Protocol Support
- MAC Filtering Function to Filter or Forward Unknown Unicast Packets
- Direct Forwarding Mode Enabling the Processor to Identify the Ingress Port and to Specify the Egress Port
- Internet Group Management Protocol (IGMP) v1/v2 Snooping Support for Multicast Packet Filtering
- IPV6 Multicast Listener Discovery (MLD) Snooping Support

Fiber Support

- Integrated LED Driver and Post Amplifier for 10BASE-FL and 100BASE-SX Optical Modules
- 100BASE-FX/SX and 10BASE-FL Fiber Support on Port 1

Monitoring

- Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port
- MIB Counters for Fully Compliant Statistics Gathering - 34 MIB Counters Per Port
- Loopback Modes for Remote Failure Diagnostics

Comprehensive Register Access

- Control Registers Configurable On-the-Fly (Port-Priority, 802.1p/d/Q)

QoS/CoS Packets Prioritization Support

- Per Port, 802.1p and DiffServ-Based
- Remapping of 802.1p Priority Field on a Per Port Basis

Power Modes, Packaging, and Power Supplies

- Full-Chip Hardware Power-Down (Register Configuration not Saved) Allows Low Power Dissipation
- Per Port-Based, Software Power-Save on PHY (Idle Link Detection, Register Configuration Preserved)
- Single Power Supply: 3.3V
- Commercial Temperature Range: 0°C to +70°C
- Available in 128-Pin PQFP
- Available in -16 Version for 8/16-Bit Bus Support and -32 version for 32-Bit Bus Support

Additional Features

In Addition to Offering All of the Features of an Integrated Layer-2 Managed Switch, the KSZ8862M Offers:

- Dynamic Buffer Memory Scheme
  - Essential for Applications Such as Video over IP where Image Jitter is Unacceptable
- 2-Port Switch with a Flexible 8-Bit, 16-Bit, or 32-Bit Generic Host Processor Interfaces
- Microchip LinkMD® Cable Diagnostic to Determine Cable Length, Diagnose Faulty Cables, and Determine Distance to Fault
- Hewlett Packard (HP) Auto-MDIX Crossover with Disable and Enable Options
- Four Priority Queues to Handle Voice, Video, Data, and Control Packets
- Ability to Transmit and Receive Frames up to 1916 bytes

Applications

- Video Distribution Systems
- High-End Cable, Satellite, and IP Set-Top Boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8862M is two-port switch with non-PCI CPU interface and fiber support, and is available in 8-/16-bit and 32-bit bus designs. This data sheet describes the KSZ8862M non-PCI CPU interface chip.

The KSZ8862M is the industry's first fully managed, two-port switch with a non-PCI CPU interface and fiber support. It is based on a proven, fourth generation, integrated two layer switch, compliant with IEEE 802.3u standards.

For industrial applications, the KSZ8862M can run in half-duplex mode regardless of the application.

In fiber mode, port one can be configurable to either 100BASE-FX or 100BASE-SX/10BASE-FL.

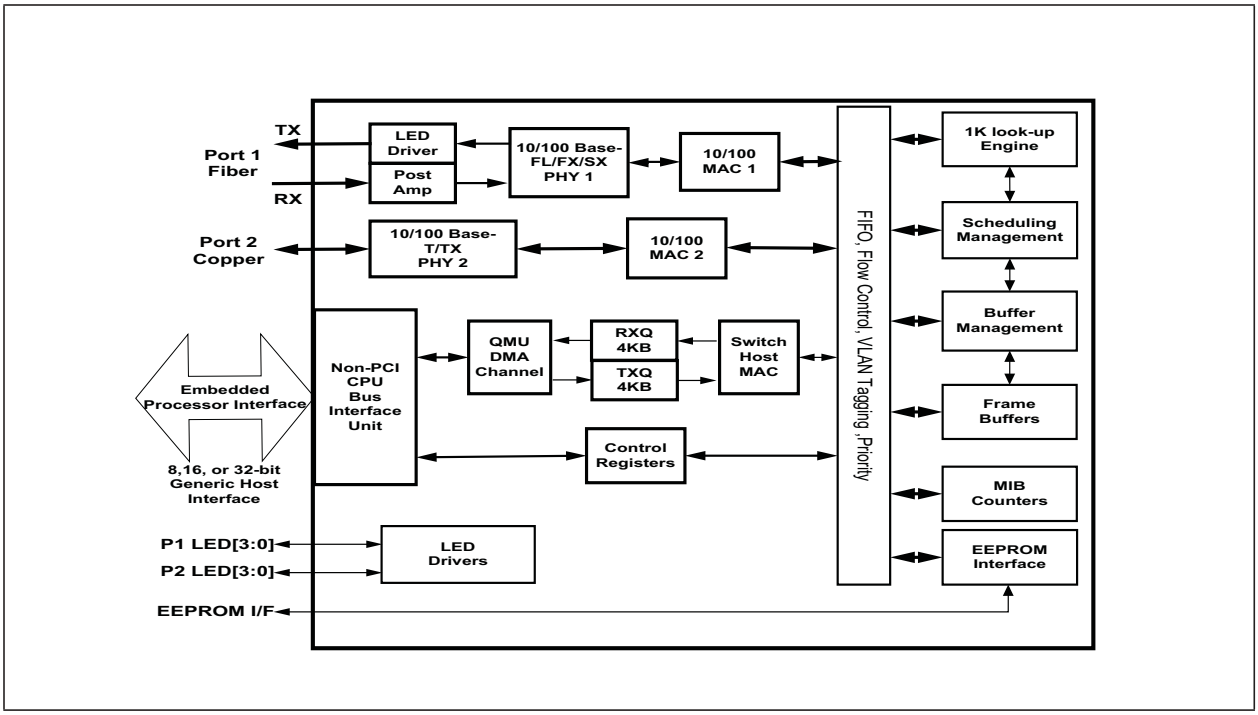
The LED driver and post amplifier are also included for 10Base-FL and 100Base-SX applications.

In copper mode, port two supports 10/100BASE-T/TX with HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables. Microchip's proprietary LinkMD® Time Domain Reflectometry (TDR)-based function is also available for determining the cable length, as well as cable diagnostics for identifying faulty cabling.

The KSZ8862M offers an extensive feature set that includes tag/port-based VLAN, quality of service (QoS) priority management, management information base (MIB) counters, and CPU control/data interfaces to effectively address Fast Ethernet applications.

The KSZ8862M contains: Two 10/100 transceivers with patented, mixed-signal, low-power technology, two media access control (MAC) units, a direct memory access (DMA) channel, a high-speed, non-blocking, switch fabric, a dedicated 1K entry forwarding table, and an on-chip frame buffer memory.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: PIN CONFIGURATION FOR KSZ8862-16MQL CHIP (8-/16-BIT)

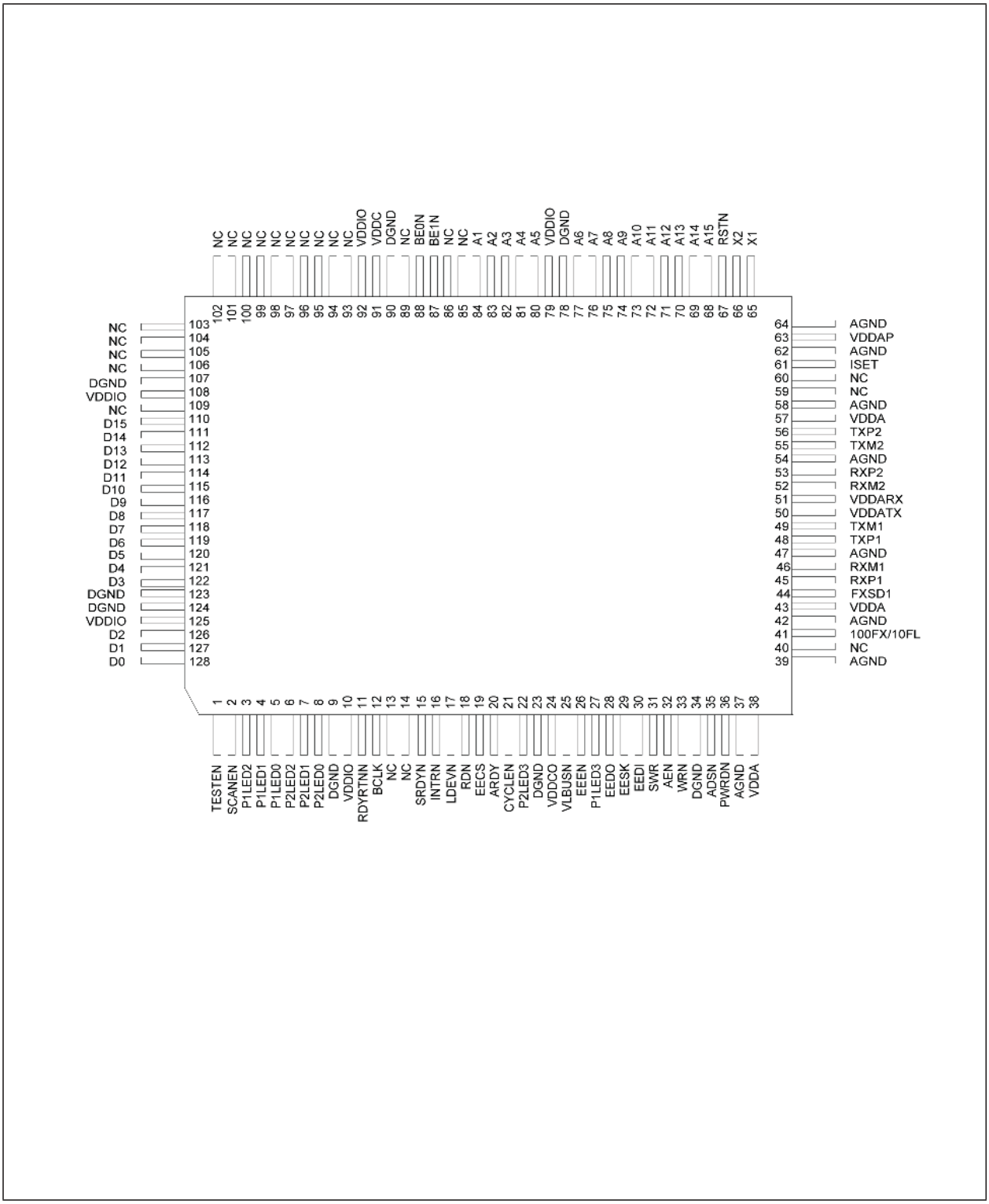


TABLE 2-1: SIGNALS

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, 1 kΩ pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, 1 kΩ pull-down this pin to ground.</td></tr>
<tr><td rowspan="15">3
4
5
6
7
8</td><td rowspan="15">P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td rowspan="15">OPU</td><td>Port 1 LED Indicators, defined as follows
<table><tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr><tr><td></td><td>[0, 0] Default</td><td>[0, 1]</td></tr><tr><td>P1LED3/P2LED3</td><td>—</td><td>—</td></tr><tr><td>P1LED2/P2LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr><tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr><tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full-Duplex</td></tr></table><table><tr><td></td><td colspan="2">Reg. SGCR5 bit [15,9]</td></tr><tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr><tr><td>P1LED3/P2LED3</td><td>Activity</td><td>—</td></tr><tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr><tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>—</td></tr><tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr></table>Note: Link = On; Activity = Blink; Link/Act = On/Blink; Full-Duplex/Col = On/Blink; Full-Duplex = On (Full-duplex); Off (Half-duplex); Speed = On (100BASE-T); Off (10BASE-T)
Note: P1LED3 is pin 27. P2LED3 is pin 22.</td></tr>
<tr><td>9</td><td>DGND</td><td>GND</td><td>Digital ground.</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>IPD</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>IPD</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50 MHz.
This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>NC</td><td>IPU</td><td>No connect.</td></tr>
<tr><td>14</td><td>NC</td><td>OPU</td><td>No connect.</td></tr>
<tr><td>15</td><td>SRDYN</td><td>OPU</td><td>Synchronous Ready Not
Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses.
For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK.
For burst mode (32-bit interface only), the KSZ8862M drives this pin low to signal wait states.</td></tr>
<tr><td>16</td><td>INTRN</td><td>OPD</td><td>Interrupt
Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7 kΩ pull-up resistor.</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
17	LDEVN	OPD	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8841M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	IPD	Read Strobe Not Asynchronous read strobe, active-low.
19	EECS	OPU	EEPROM Chip Select
20	ARDY	OPD	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. this pin need an external 4.7 kΩ pull-up resistor.
21	CYCLEN	IPD	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	P2LED3	OPD	Port 2 LED indicator See the description in pins 6, 7, and 8.
23	DGND	GND	Digital IO ground.
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite bead and capacitors).
25	VLBUSN	IPD	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode.
26	EEEN	IPD	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	OPD	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	OPD	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	OPD	EEPROM Serial Clock A 4 µs serial output clock to load configuration data from the serial EEPROM.
30	EEDI	IPD	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bit bus mode or don’t care for 32-bit bus mode when EEEN is pull-down (without EEPROM).
31	SWR	IPD	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
32	AEN	IPU	Address Enable Address qualifier for the address decoding, active-low.

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
33	WRN	IPD	Write Strobe Not Asynchronous write strobe, active-low.
34	DGND	GND	Digital IO ground
35	ADSN	IPD	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	IPU	Full-chip power-down. (Low = Power down; High or floating = Normal operation).
37	AGND	GND	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
39	AGND	GND	Analog ground
40	NC	—	No Connect
41	100FX/10FL	IPU	Fiber mode select for port 1.1 kΩ pull-up to 3.3V for 100BASE-FX, 100Ω pull-down to GND for 100 BASE-SX or 10 BASE-FL.
42	AGND	GND	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
44	FXSD1	I	Fiber signal detect input for port 1 in 100BASE-FX fiber mode. 1 kΩ pull-up to 3.3V for port 1 in 100BASE-SX or 10BASE-FL fiber modes.
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit signal (+ differential) from external fiber module.
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit signal (– differential) from external fiber module.
47	AGND	GND	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) signal (+ differential) to external fiber module
49	TXM1	I/O	Port 1 physical transmit (MDI) signal (– differential) to external fiber module
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	RXM2	I/O	No Connect
53	RXP2	I/O	No Connect
54	AGND	GND	Analog ground
55	NC	—	Port 2 physical receive (MDI) or transmit (MDIX) signal (– differential)
56	NC	—	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential)
57	VDDA	P	1.2 analog V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
58	AGND	GND	Analog ground
59	NC	IPU	No connect
60	NC	IPU	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
62	AGND	GND	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
64	AGND	GND	Analog ground

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
65	X1	I	25 MHz crystal or oscillator clock connection.
66	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ±50 ppm for either crystal or oscillator.
67	RSTN	IPU	Hardware reset pin (active-low). This reset input is required minimum of 10 ms low after stable supply voltage 3.3V.
68	A15	I	Address 15
69	A14	I	Address 14
70	A13	I	Address 13
71	A12	I	Address 12
72	A11	I	Address 11
73	A10	I	Address 10
74	A9	I	Address 9
75	A8	I	Address 8
76	A7	I	Address 7
77	A6	I	Address 6
78	DGND	GND	Digital IO ground
79	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
80	A5	I	Address 5
81	A4	I	Address 4
82	A3	I	Address 3
83	A2	I	Address 2
84	A1	I	Address 1
85	NC	I	No Connect
86	NC	I	No Connect
87	BE1N	I	Byte Enable 1 Not, Active-low for Data byte 1 enable (don't care in 8-bit bus mode).
88	BE0N	I	Byte Enable 0 Not, Active-low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode).
89	NC	I	No Connect
90	DGND	GND	Digital core ground
91	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
92	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	NC	I	No Connect
94	NC	I	No Connect
95	NC	I	No Connect
96	NC	I	No Connect
97	NC	I	No Connect
98	NC	I	No Connect
99	NC	I	No Connect
100	NC	I	No Connect
101	NC	I	No Connect

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
102	NC	I	No Connect
103	NC	I	No Connect
104	NC	I	No Connect
105	NC	I	No Connect
106	NC	I	No Connect
107	DGND	GND	Digital IO ground
108	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
109	NC	I	No Connect
110	D15	I/O	Data 15
111	D14	I/O	Data 14
112	D13	I/O	Data 13
113	D12	I/O	Data 12
114	D11	I/O	Data 11
115	D10	I/O	Data 10
116	D9	I/O	Data 9
117	D8	I/O	Data 8
118	D7	I/O	Data 7
119	D6	I/O	Data 6
120	D5	I/O	Data 5
121	D4	I/O	Data 4
122	D3	I/O	Data 3
123	DGND	GND	Digital IO ground
124	DGND	GND	Digital core ground
125	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
126	D2	I/O	Data 2
127	D1	I/O	Data 1
128	D0	I/O	Data 0

Note 2-1 P = power supply; GND = ground; I = input; O = output
I/O = bi-directional
IPU/O = Input with internal pull-up during reset; output pin otherwise.
IPU = Input with internal pull-up.
IPD = Input with internal pull-down.
OPU = Output with internal pull-up.
OPD = Output with internal pull-down.

FIGURE 2-2: PIN CONFIGURATION FOR KSZ8841-32MQL CHIP (32-BIT)

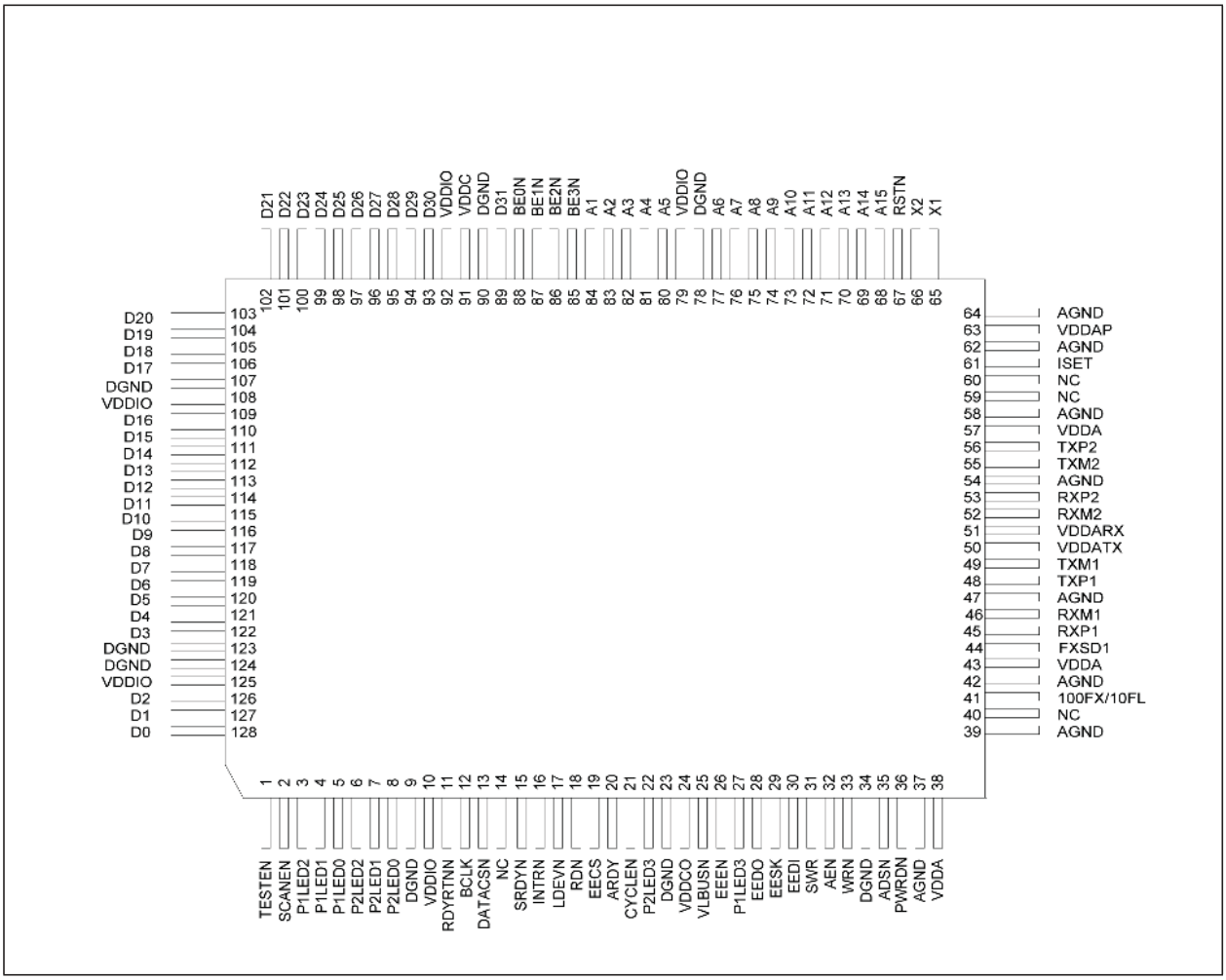


TABLE 2-2: PIN DESCRIPTION FOR KSZ8841-32 CHIP (32-BIT)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, 1 kΩ pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, 1 kΩ pull-down this pin to ground.</td></tr>
<tr><td rowspan="15">3
4
5
6
7
8</td><td rowspan="15">P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td rowspan="15">OPU</td><td>Port 1 LED Indicators, defined as follows
<table>
<tr><td></td><td colspan="2">Chip Global Control Register:
CGCR bit [15,9]</td></tr>
<tr><td></td><td>[0, 0] Default</td><td>[0, 1]</td></tr>
<tr><td>P1LED3/P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td></td><td colspan="2"></td></tr>
<tr><td></td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
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<tr><td>P1LED3/P2LED3</td><td>Activity</td><td>—</td></tr>
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<tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
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Note: Link = On; Activity = Blink; Link/Act = On/Blink; Full-Duplex/Col = On/Blink; Full-Duplex = On (Full-duplex); Off (Half-duplex); Speed = On (100BASE-T); Off (10BASE-T)
Note: P1LED3 is pin 27. P2LED3 is pin 22.</td></tr>
<tr><td>9</td><td>DGND</td><td>GND</td><td>Digital ground.</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>IPD</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>IPD</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50 MHz.
This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>DATACSN</td><td>IPU</td><td>DATA Chip Select Not (For KSZ8862-32 Mode only)
Chip select signal for QMU data register (QDRH, QDRL), active Low.
When DATACSN is Low, the data path can be accessed regardless of the value of AEN, A15-A1, and the content of the BANK select register.</td></tr>
<tr><td>14</td><td>NC</td><td>OPU</td><td>No connect.</td></tr>
<tr><td>15</td><td>SRDYN</td><td>OPU</td><td>Synchronous Ready Not
Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses.
For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK.
For burst mode (32-bit interface only), the KSZ8862M drives this pin low to signal wait states.</td></tr>
</table>

TABLE 2-2: PIN DESCRIPTION FOR KSZ8841-32 CHIP (32-BIT) (CONTINUED)

Pin Number	Pin Name	Type	Description
16	INTRN	OPD	Interrupt Active-low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7 kΩ pull-up resistor.
17	LDEVN	OPD	Local Device Not Active-low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8862M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	IPD	Read Strobe Not Asynchronous read strobe, active-low.
19	EECS	OPU	EEPROM Chip Select.
20	ARDY	OPD	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. this pin need an external 4.7 kΩ pull-up resistor.
21	CYCLEN	IPD	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	NC	OPD	No Connect
23	DGND	GND	Digital IO ground
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite Bead and capacitors).
25	VLBUSN	IPD	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 32-bit asynchronous mode or EISA-like burst mode.
26	EEEN	IPD	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	OPD	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	OPD	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	OPD	EEPROM Serial Clock A 4 µs serial output clock to load configuration data from the serial EEPROM.
30	EEDI	IPD	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bit bus mode or don't care for 32-bit bus mode when EEEN is pull-down (without EEPROM).
31	SWR	IPD	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.

TABLE 2-2: PIN DESCRIPTION FOR KSZ8841-32 CHIP (32-BIT) (CONTINUED)

Pin Number	Pin Name	Type	Description
32	AEN	IPU	Address Enable Address qualifier for the address decoding, active-low.
33	WRN	IPD	Write Strobe Not Asynchronous write strobe, active-low.
34	DGND	GND	Digital IO ground
35	ADSN	IPD	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	IPU	Full-chip power-down. Active-low (Low = Power down; High or floating = Normal operation).
37	AGND	GND	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
39	AGND	GND	Analog ground
40	NC	—	No Connect
41	NC	—	No Connect
42	AGND	GND	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
44	NC	—	No Connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	GND	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	NC	—	No Connect
53	NC	—	No Connect
54	AGND	GND	Analog ground
55	NC	—	No Connect
56	NC	—	No Connect
57	VDDA	P	1.2 analog V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
58	AGND	GND	Analog ground
59	NC	IPU	No connect
60	NC	IPU	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
62	AGND	GND	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
64	AGND	GND	Analog ground

TABLE 2-2: PIN DESCRIPTION FOR KSZ8841-32 CHIP (32-BIT) (CONTINUED)

Pin Number	Pin Name	Type	Description
65	X1	I	25 MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ±50 ppm for either crystal or oscillator.
66	X2	O	
67	RSTN	IPU	Reset Not Hardware reset pin (active-low). This reset input is required minimum of 10 ms low after stable supply voltage 3.3V.
68	A15	I	Address 15
69	A14	I	Address 14
70	A13	I	Address 13
71	A12	I	Address 12
72	A11	I	Address 11
73	A10	I	Address 10
74	A9	I	Address 9
75	A8	I	Address 8
76	A7	I	Address 7
77	A6	I	Address 6
78	DGND	GND	Digital IO ground
79	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
80	A5	I	Address 5
81	A4	I	Address 4
82	A3	I	Address 3
83	A2	I	Address 2
84	A1	I	Address 1
85	BE3N	I	Byte Enable 3 Not, Active-low for Data byte 3 enable
86	BE2N	I	Byte Enable 2 Not, Active-low for Data byte 2 enable
87	BE1N	I	Byte Enable 1 Not, Active-low for Data byte 1 enable
88	BE0N	I	Byte Enable 0 Not, Active-low for Data byte 0 enable
89	D31	I/O	Data 31
90	DGND	GND	Digital core ground
91	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (pin 24) through external Ferrite bead and capacitor.
92	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	D30	I/O	Data 30
94	D29	I/O	Data 29
95	D28	I/O	Data 28
96	D27	I/O	Data 27
97	D26	I/O	Data 26
98	D25	I/O	Data 25
99	D24	I/O	Data 24
100	D23	I/O	Data 23
101	D22	I/O	Data 22
102	D21	I/O	Data 21

TABLE 2-2: PIN DESCRIPTION FOR KSZ8841-32 CHIP (32-BIT) (CONTINUED)

Pin Number	Pin Name	Type	Description
103	D20	I/O	Data 20
104	D19	I/O	Data 19
105	D18	I/O	Data 18
106	D17	I/O	Data 17
107	DGND	GND	Digital IO ground
108	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
109	D16	I/O	Data 16
110	D15	I/O	Data 15
111	D14	I/O	Data 14
112	D13	I/O	Data 13
113	D12	I/O	Data 12
114	D11	I/O	Data 11
115	D10	I/O	Data 10
116	D9	I/O	Data 9
117	D8	I/O	Data 8
118	D7	I/O	Data 7
119	D6	I/O	Data 6
120	D5	I/O	Data 5
121	D4	I/O	Data 4
122	D3	I/O	Data 3
123	DGND	GND	Digital IO ground
124	DGND	GND	Digital core ground
125	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
126	D2	I/O	Data 2
127	D1	I/O	Data 1
128	D0	I/O	Data 0

Legend:

P = Power supply, GND = Ground
I/O = Bi-directional, I = Input, O = Output.
IPD = Input with internal pull-down.
IPU = Input with internal pull-up.
OPD = Output with internal pull-down.
OPU = Output with internal pull-up.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8862M contains two 10/100 physical layer transceivers (PHYs), two MAC units, and a DMA channel integrated with a Layer-2 switch.

The KSZ8862M contains a bus interface unit (BIU) that controls the KSZ8862M via an 8-, 16-, or 32-bit host interface.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption.

3.1 Functional Overview: Physical Layer Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function (port 2 only) performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external1% 3.01 kΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function (port 2 only) performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side begins with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based upon comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.1.4 100BASE-FX OPERATION

100BASE-FX operation is supported on port 1 and similar to 100BASE-TX operation with the differences being that the scrambler/descrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In addition, auto-negotiation is bypassed and auto MDI/MDI-X is disabled.

3.1.5 100BASE-FX SIGNAL DETECTION

In 100BASE-FX operation, FXSD1 (fiber signal detect), input pin 44, is usually connected to the fiber transceiver SD (signal detect) output pin. 100BASE-FX mode is activated when the FXSD1 input pin is greater than 1V. When FXSD1 is between 1V and 1.8V, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD1 is over 2.2V, the fiber signal is detected. Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD1 input pin is tied high to force 100BASE-FX mode.

The 100BASE-FX signal detection is summarized as below:

When FXSD1 input voltage is less than 0.2V, this is not a fiber mode or there is no fiber connection.

When FXSD1 input voltage is greater than 1.0V but less than 1.8V, this is a FX mode but no signal detected and far-end fault generated.

When FXSD1 input voltage is greater than 2.2V, this is a FX mode with signal detected.

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD1 pin's input voltage threshold.

3.1.6 100BASE-FX FAR-END-FAULT (FEF)

A far-end-fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8862M detects a FEF when its FXSD1 input on port 1 is between 1V and 1.8V. When a FEF is detected, the KSZ8862M signals its fiber link partner that a FEF has occurred by sending 84 1's followed by a zero in the idle period between frames.

By default, FEF is enabled. FEF can be disabled through register setting at P1MBCR (bit2) or P1CR4 (bit12).

3.1.7 100BASE-SX OPERATION

100BASE-SX operation is supported on port 1 only. It conforms to the TIA/EIA-785 Standard for 100BASE-SX fiber operation. Fiber Link Negotiation Pulse (FLNP) Bursts are used to advertise link capabilities to the link partner during fiber auto-negotiation. FLNP Bursts are equivalent to the Fast Link Pulse (FLP) Bursts used in 10BASE-T and 100BASE-TX auto-negotiation defined by clause 28 of the IEEE802.3 Standard. Refer to respective Standard for details.

3.1.7.1 Physical Interface

For 100BASE-SX operation, port 1 interfaces with an external fiber module to drive 850 nm fiber optic links up to a maximum distance of 300m. The interface connections between the KSZ8862M and fiber module are single-ended (common mode). 100BASE-SX signal transmission and reception are done on TXM1 (pin 49) and RXM1 (pin 46), respectively. Refer to Microchip reference schematic for recommended interface circuit and termination.

3.1.7.2 Enabling 100BASE-SX Mode

To enable 100BASE-SX mode, tie FXSD1 (pin 44) to high (+3.3V) and 100FX/10FL (pin 41) to ground.

3.1.7.3 Enabling Fiber Forced Mode

In 100BASE-SX mode, the KSZ8862M supports forced mode only.

For forced mode, port 1 has auto-negotiation disabled, is forced to 100Mbps for the speed, and is set to either half or full duplex. Optionally, flow control can be enabled to send out PAUSE frames in full duplex mode.

Forced mode and auto-negotiation disabled mode settings for 100BASE-SX fiber use the same registers (P1MBCR, P1CR4). These registers are summarized in the Register Map: MAC and PHY section.

3.1.8 10BASE-FL OPERATION

10BASE-FL operation is supported on port 1 only. It conforms to clause 15 and 18 of the IEEE802.3 Standard for 10BASE-FL fiber operation. Fiber Link Negotiation Pulse (FLNP) Bursts are used to advertise link capabilities to the link partner during fiber auto-negotiation. FLNP Bursts are equivalent to the Fast Link Pulse (FLP) Bursts used in 10BASE-T and 100BASE-TX auto-negotiation defined by clause 28 of the IEEE802.3 Standard. Refer to respective Standard for details.

3.1.8.1 Physical Interface

For 10BASE-FL operation, port 1 interfaces with an external fiber module to drive 850 nm fiber optic links up to a maximum distance of 2 km. The interface connections between the KSZ8862M and fiber module are single-ended (common mode). 10BASE-FL signal transmission and reception are done on TXM1 (pin 49) and RXM1 (pin 46), respectively. Refer to Micrel reference schematic for recommended interface circuit and termination.

3.1.8.2 Enabling 10BASE-FL Mode.

To enable 10BASE-FL mode, tie FXSD1 (pin 44) to high (+3.3V) and 100FX/10FL (pin 41) to ground 2.

3.1.8.3 Enabling Fiber Forced Mode

In 10BASE-FL mode, the KSZ8862M supports forced mode only.

For forced mode, port 1 has auto-negotiation disabled, is forced to 10 Mbps for the speed, and is set to either half or full duplex. Optionally, flow control can be enabled to send out PAUSE frames in full duplex mode.

Forced mode and auto-negotiation disabled mode settings for 10BASE-FL fiber use the same registers (P1MBCR, P1CR4). These registers are summarized in the Register Map section.

3.1.9 10BASE-T TRANSMIT

The 10BASE-T driver (port 2 only) is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typically 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all ones Manchester-encoded signal.

3.1.10 10BASE-T RECEIVE

On the receive side (port 2 only), input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8862M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.11 LED DRIVER

The device provides a current mode fiber LED driver (port 1 only). The edge-enhanced current mode does not require any output wave shaping. The drive current of the LED driver can be programmed through ATCR0 [7:6] register in Bank 44.

3.1.12 POST AMPLIFIER

The chip also includes a post amplifier (port 1 only). The post amplifier is intended for interfacing the output of the pre-amplifier of the PIN diode module. The minimum sensitivity of the amplifier is 2.5 mV(rms) for 10BASE-FL receive on pin RXM1 or 16 mV(rms) for 100BASE-SX receive on pin RXM1.

3.1.13 POWER MANAGEMENT

The KSZ8862M features per port power-down mode. To save power, the user can power-down the port that is not in use by setting bit 11 in either P1CR4 or P1MBCR register for port 1 and setting bit 11 in either P2CR4 or P2MBCR register for port 2. To bring the port back up, reset bit 11 in these registers.

In addition, there is a full switch power-down mode. This mode shuts the entire switch down, when the PWRDN (pin 36) is pulled down to low.

3.1.14 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8862M supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover on port 2. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8862M device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in Table 3-1.

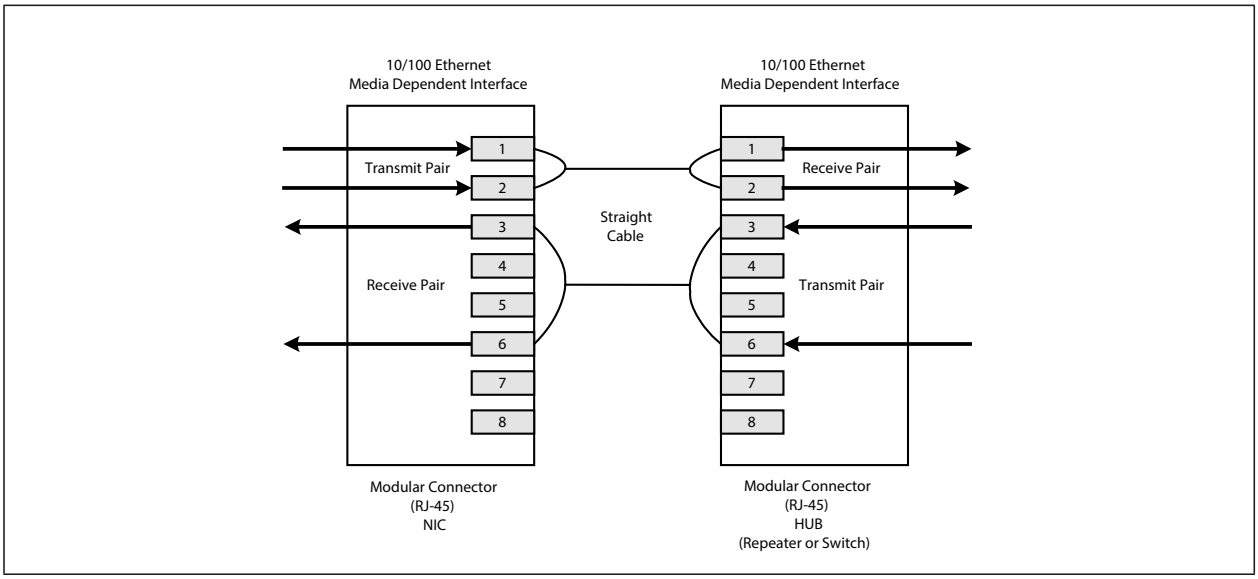
TABLE 3-1: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.1.14.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a NIC card (MDI) and a switch or hub (MDI-X).

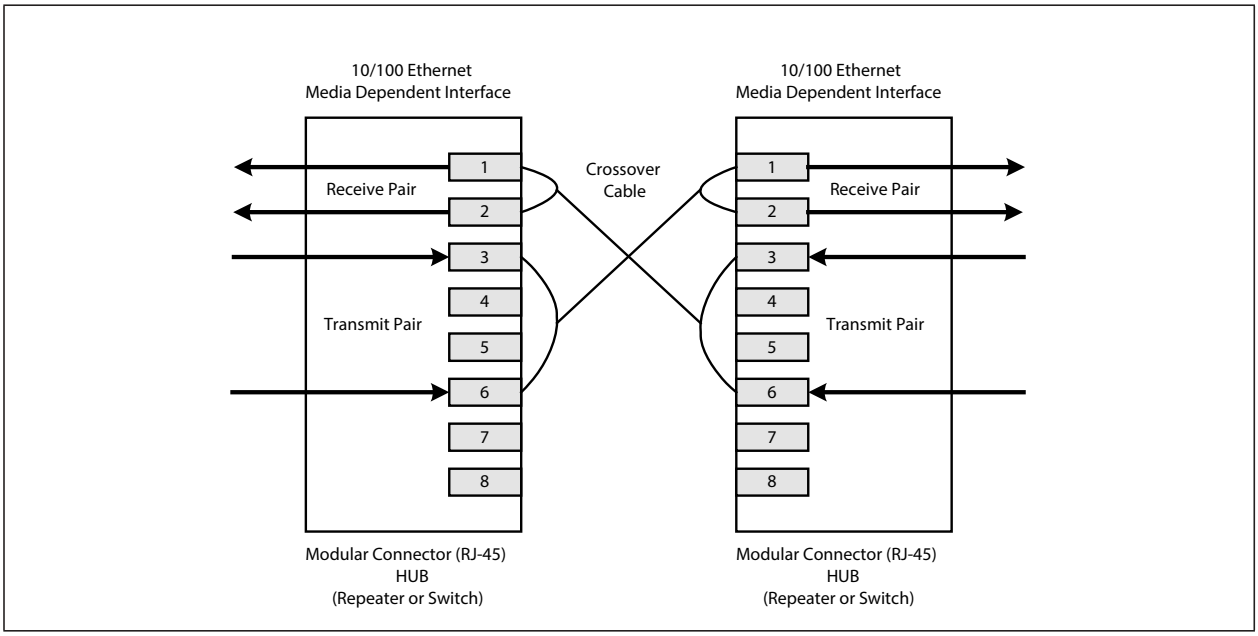
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.1.14.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



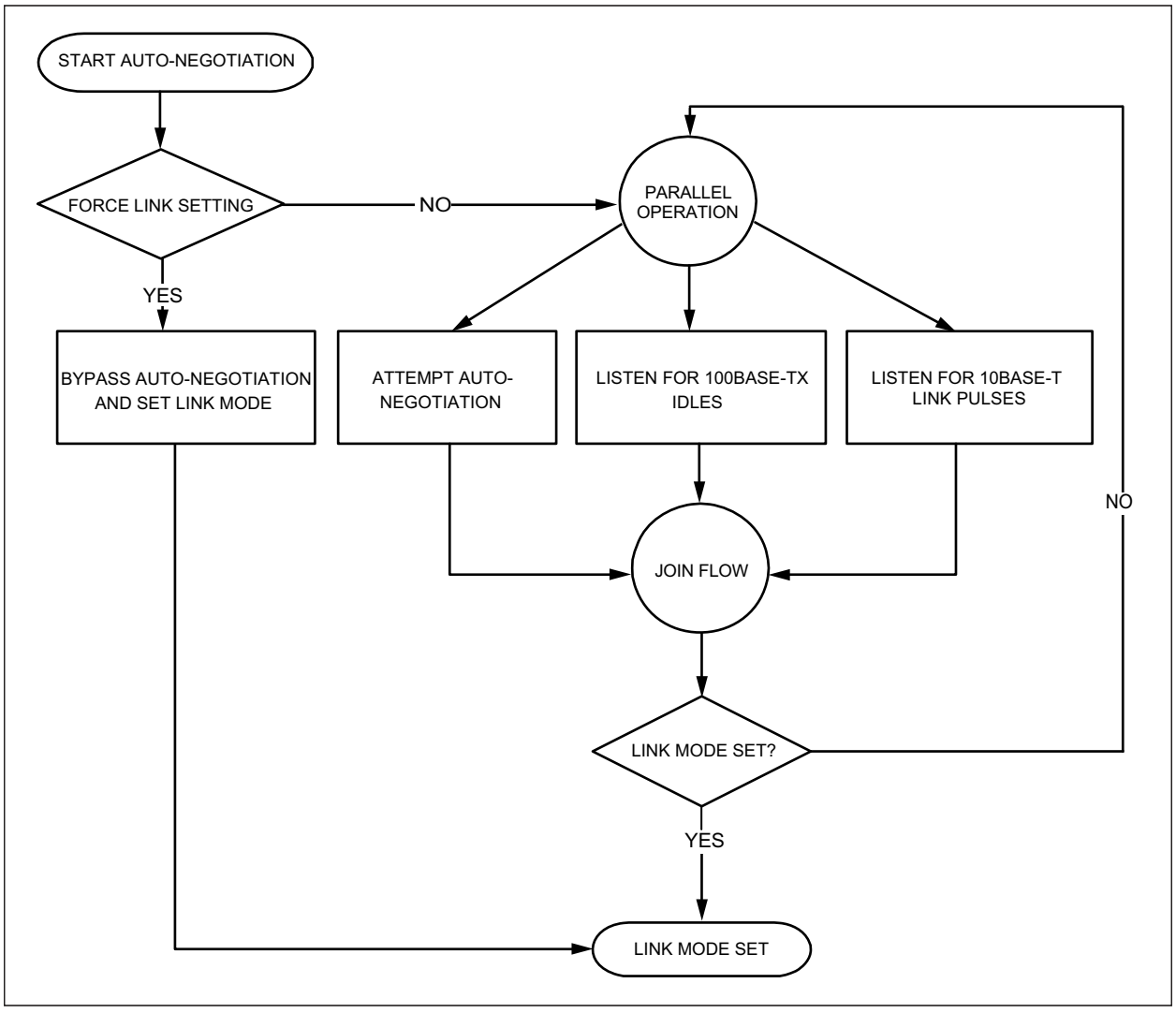
3.1.15 AUTO-NEGOTIATION

The KSZ8862M conforms to the auto negotiation protocol as described by the 802.3 committee to allow the channel to operate at 10BASE-T or 100BASE-TX on port 2 only.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8862M is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.1.16 LINKMD® CABLE DIAGNOSTICS

The KSZ8862M LinkMD® uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format in register P1VCT[8:0].

Note that cable diagnostics are only valid for copper connections. Fiber-optic operation is not supported.

3.1.16.1 Access

LinkMD is initiated by accessing register P2VCT, the LinkMD Control/Status register, in conjunction with register P2CR4, the 100BASE-TX PHY Controller register.

3.1.16.2 Usage

LinkMD can be run at any time by ensuring that Auto-MDIX has been disabled. To disable Auto-MDIX, write a ‘1’ to P2CR4[10] for port 2 to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P2VCT[15] for port 2, is set to ‘1’ to start the test on this pair.

When bit P1VCT[15] returns to ‘0’, the test is complete. The test result is returned in bits P2VCT[14:13] and the distance is returned in bits P2VCT[8:0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

If P2VCT[14:13] =11, this indicates an invalid test, and occurs when the KSZ8862M is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8862M to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by the following formula:

P2VCT[8:0] x 0.4m for port 2 cable distance

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.2 Functional Overview: MAC and Switch

3.2.1 ADDRESS LOOKUP

The internal lookup engine updates its table with a new entry if the following conditions are met:

The KSZ8862M is guaranteed to learn 1K addresses and distinguishes itself from hash-based look-up tables, which depending upon the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.2.2 LEARNING

The internal lookup engine updates its table with a new entry if the following conditions are met:

- The received packet's Source Address (SA) does not exist in the lookup table.
- The received packet is good without receiving errors; the packet size is legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, then the last entry of the table is deleted to make room for the new entry.

3.2.3 MIGRATION

The internal look-up engine also monitors whether a station has moved. If a station has moved, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good without receiving errors; the packet size is legal length.

The lookup engine updates the existing record in the table with the new source port information.

3.2.4 AGING

The look-up engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine removes the record from the table. The look-up engine constantly performs the aging process and continuously removes aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through Global Register SGCR1 [10].

3.2.5 FORWARDING

The KSZ8862M forwards packets using the algorithm that is depicted in the following flowcharts. Figure 3-4 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 3-5. The packet is sent to PTF2.

FIGURE 3-4: DESTINATION ADDRESS LOOKUP FLOW CHART IN STAGE ONE

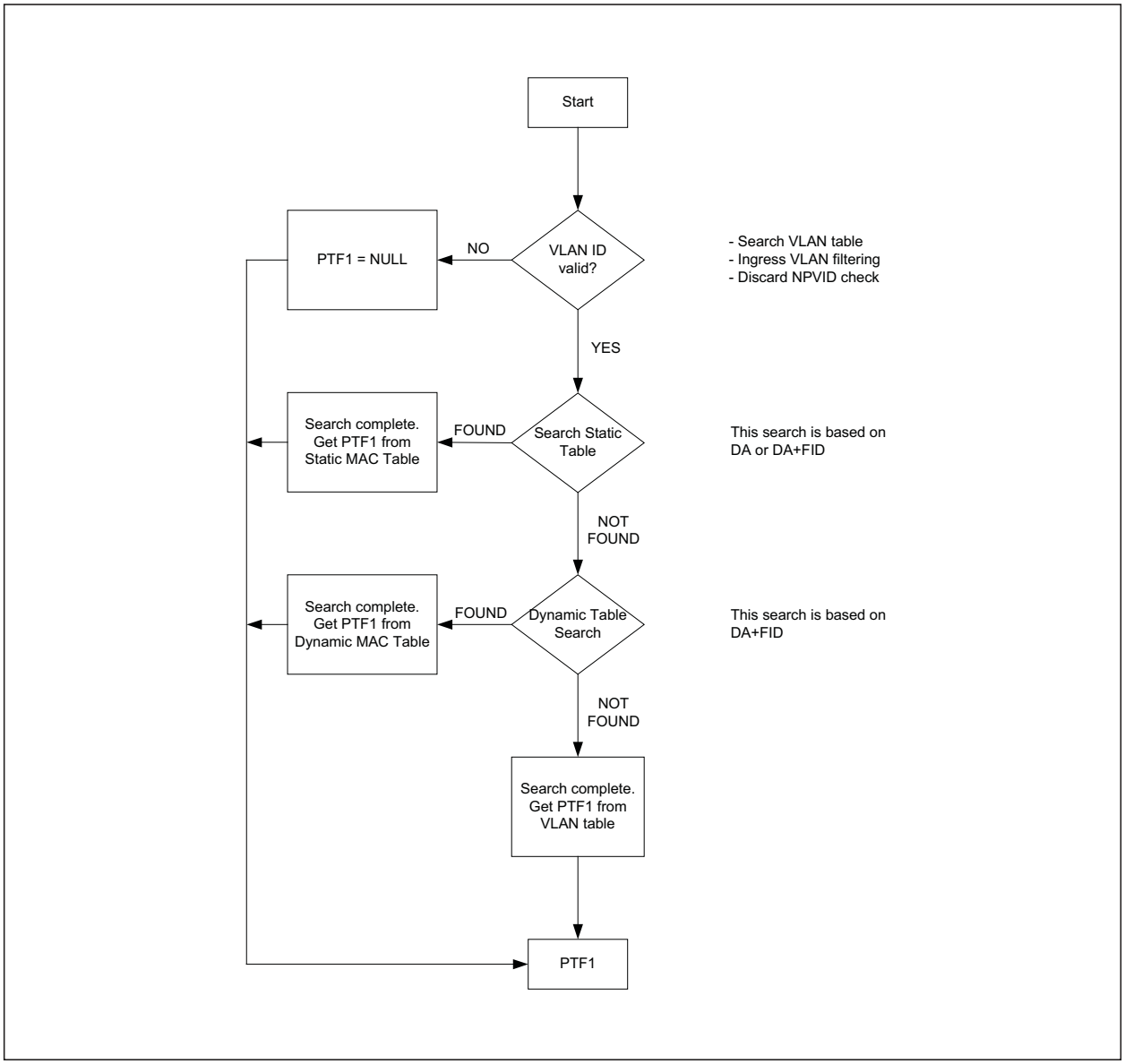
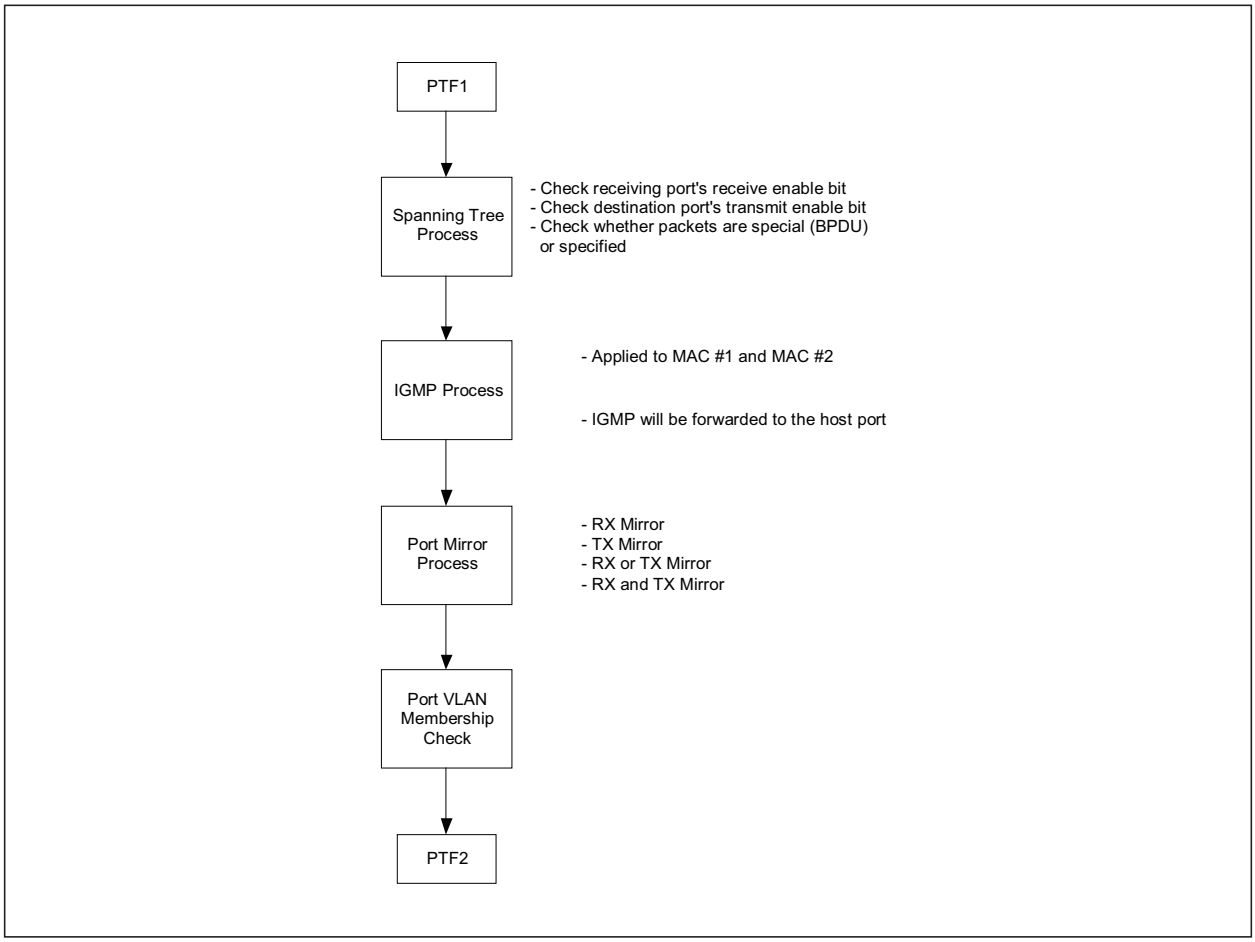


FIGURE 3-5: DESTINATION ADDRESS RESOLUTION FLOW CHART IN STAGE TWO



The KSZ8862M will not forward the following packets:

• Error packets.

These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.

• 802.3x pause frames.

The KSZ8862M intercepts these packets and performs the flow control.

• Local packets.

Based on destination address (DA) look-up. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as local.

3.2.6 SWITCHING ENGINE

The KSZ8862M features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The switching engine has a 32 KB internal frame buffer. This resource is shared between all the ports. There are a total of 256 buffers available. Each buffer is sized at 128B.

3.2.7 MAC OPERATION

The KSZ8862M strictly abides by IEEE 802.3 standards to maximize compatibility. Additionally, there is an added MAC filtering function to filter unicast packets. The MAC filtering function is useful in applications such as VoIP where restricting certain packets reduces congestion and thus improves performance.

3.2.8 INTER PACKET GAP (IPG)

If a frame is successfully transmitted, the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, then the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

3.2.9 BACK-OFF ALGORITHM

The KSZ8862M implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode, and optional aggressive mode back-off. After 16 collisions, the packet is optionally dropped depending upon the switch configuration in SGCR1 [8].

3.2.10 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, then the packet is dropped.

3.2.11 LEGAL PACKET SIZE

The KSZ8862M discards packets less than 64 bytes and can be programmed to accept packet size up to 1536 bytes in SGCR2 [1]. The KSZ8862M can also be programmed for special applications to accept packet size up to 1916 bytes in SGCR2 [2].

3.2.12 FLOW CONTROL

The KSZ8862M supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8862M receives a pause control frame, the KSZ8862M will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8862M are transmitted.

On the transmit side, the KSZ8862M has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues, and available receive queues.

The KSZ8862M will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8862M issues a flow control frame (Xoff), containing the maximum pause time as defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8862M then sends out the other flow control frame (Xon) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

The KSZ8862M flow controls all ports if the receive queue becomes full.

3.2.13 HALF-DUPLEX BACKPRESSURE

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same in full-duplex mode. If backpressure is required, then the KSZ8862M sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8862M discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, then the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, then the carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, then the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive back off (bit 8 in SGCR1)
- No excessive collision drop (bit 3 in SGCR2)

Note: These bits are not set in default, since this is not the IEEE standard.

3.2.14 BROADCAST STORM PROTECTION

The KSZ8862M has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8862M has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis in P1CR1 [7] and P2CR1 [7]. The rate is based on a 67ms interval for 100BT and a 670ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in SGCR3 [2:0] [15:8]. The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec x 67 ms/interval x 1% = 99 frames/interval (approx.) = 0 x 63

Note: 148,800 frames/sec is based on 64-byte block of packets in 100BASE-T with 12 bytes of IPG and 8 bytes of preamble between two packets.

3.2.15 CLOCK GENERATOR

The X1 and X2 pins are connected to a 25 MHz crystal. X1 can also serve as the connector to a 3.3V, 25 MHz oscillator (as described in the Pin Description and Configuration section).

The bus interface unit (BIU) uses BCLK (Bus Clock) for synchronous accesses. The maximum host port frequency is 50 MHz for VLBus-like and burst mode (32-bit interface only).

3.3 Bus Interface Unit (BIU)

The host interface of the BIU is designed to communicate with embedded processors. The host interface of the KSZ8862M is a generic bus interface. Some glue logic may be required when the interface talks to various buses and processors.

In terms of transfer type, the BIU can support two transfers: asynchronous transfer and synchronous transfer. To support these transfers (asynchronous and synchronous), the BIU provides three groups of signals:

- Synchronous signals
- Asynchronous signals
- Common signals used for both synchronous and asynchronous transfers

Since both synchronous and asynchronous signals are independent of each other, synchronous burst transfer and asynchronous transfer can be mixed or interleaved but cannot be overlapped (due to the sharing of the common signals).

In terms of physical data bus size, the KSZ8862M supports 8-, 16-, and 32 bit host/industrial standard data bus sizes. Given a physical data bus size, the KSZ8862M supports 8-, 16-, or 32-bit data transfers depending upon the size of the physical data bus. For example, for a 32-bit system/host data bus, it allows 8-, 16-, and 32-bit data transfers (KSZ8862-32MQL); for a 16-bit system/host data bus, it allows 8- and 16-bit data transfers (KSZ8862-16MQL); and for 8-bit system/host data bus, it only allows 8-bit data transfers (KSZ8862-16MQL).

Note that KSZ8862M does not support internal data byte-swap but it does support internal data word-swap. This means that the system/host data bus HD [7:0] has to connect to both D [7:0] and D [15:8] for 8-bit data bus interfaces. However, the system/host data bus HD [15:8] and HD [7:0] just connects to D [15:8] and D [7:0], respectively, for 16-bit data bus interface; there is no need to connect HD [31:24] and HD [23:16] to D [31:24] and D [23:16].

Table 3-2 describes the BIU signal grouping.

TABLE 3-2: BUS INTERFACE UNIT SIGNAL GROUPING

Signal	Type	Function
Common Signals		
A[15:1]	I	Address
AEN	I	Address Enable Address Enable asserted indicates memory address on the bus for DMA access and because the device is an I/O device, address decoding is only enabled when AEN is Low.

TABLE 3-2: BUS INTERFACE UNIT SIGNAL GROUPING (CONTINUED)

<table>
<tr><th>Signal</th><th>Type</th><th>Function</th></tr>
<tr><td rowspan="11">BE3N,
BE2N,
BE1N,
BE0N</td><td rowspan="11">I</td><td>Byte Enable
<table><tr><th>BE0N</th><th>BE1N</th><th>BE2N</th><th>BE3N</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>32-bit access (32-bit bus only)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Lower 16-bit (D[15:0]) access</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Higher 16-bit (D[31:16]) access</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 0 (D[7:0]) access</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Byte 1 (D[15:8]) access</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Byte 2 (D[23:16]) access (32-bit bus only)</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Byte 3 (D[31:24]) access (32-bit bus only)</td></tr></table></td></tr>
<tr><td>Note 1: BE3N, BE2N, BE1N, and BE0N are ignored when DATACSN is low because 32-bit transfers are assumed.
Note 2: BE2N and BE3N are valid only for the KSZ8862-32 mode, and are No Connect for the KSZ88621-16 mode.</td></tr>
<tr><td>D[31:16]</td><td>I/O</td><td>Data
For KSZ8862M-32 mode only.</td></tr>
<tr><td>D[15:0]</td><td>I/O</td><td>Data
For both KSZ8862-32 and KSZ8862-16 modes</td></tr>
<tr><td>ADSN</td><td>I</td><td>Address Strobe
The rising edge of ADSN is used to latch A[15:1], AEN, BE3N, BE2N, BE1N, and BE0N.</td></tr>
<tr><td>LDEVN</td><td>O</td><td>Local Device
This signal is a combinatorial decode of AEN and A[15:4]. This A[15:4] is used to compare against the Base Address Register.</td></tr>
<tr><td>DATACSN</td><td>I</td><td>Data Register Chip Select (For KSZ8862-32 Mode only)
This signal is used for central decoding architecture (mostly for embedded application). When asserted, the device’s local decoding logic is ignored and the 32-bit access to QMU Data Register is assumed.</td></tr>
<tr><td>INTRN</td><td>O</td><td>Interrupt</td></tr>
<tr><td colspan="3">Synchronous Transfer Signals</td></tr>
<tr><td>VLBUSN</td><td>I</td><td>VLBUS
VLBUSN = 0, VLBus-like cycle.
VLBUSN = 1, burst cycle (both host/system and KSZ8862M can insert wait state)</td></tr>
<tr><td>CYCLEN</td><td>I</td><td>CYCLEN
For VLBus-like access: used to sample SWR when asserted.
For burst access: used to connect to IOWC# bus signal to indicate burst write.</td></tr>
<tr><td>SWR</td><td>I</td><td>Write/Read
For VLBus-like access: used to indicate write (High) or read (Low) transfer.
For burst access: used to connect to IORC# bus signal to indicate burst read.</td></tr>
<tr><td>SRDYN</td><td>O</td><td>Synchronous Ready
For VLBus-like access: exactly the same signal definition of nSRDY in VLBus.
For burst access: insert wait state by KSZ8862M whenever necessary during the Data Register access.</td></tr>
<tr><td>RDYRTNN</td><td>I</td><td>Ready Return
For VLBus-like access: exactly like RDYRTNN signal in VLBus to end the cycle.
For burst access: exactly like EXRDY signal in EISA to insert wait states. Note that the wait states are inserted by system logic (memory) not by KSZ8862M.</td></tr>
<tr><td>BCLK</td><td>I</td><td>Bus Clock</td></tr>
<tr><td colspan="3">Asynchronous Transfer Signals</td></tr>
<tr><td>RDN</td><td>I</td><td>Asynchronous Read</td></tr>
<tr><td>WRN</td><td>I</td><td>Asynchronous Write</td></tr>
</table>

TABLE 3-2: BUS INTERFACE UNIT SIGNAL GROUPING (CONTINUED)

Signal	Type	Function
ARDY	O	Asynchronous Ready This signal is asserted (Low) to insert wait states.

Note 3-1 I = Input. O = Output. I/O = Bi-directional.

Regardless of whether the transfer is synchronous or asynchronous, if the address latch is required, use the rising edge of ADSN to latch the incoming signals A[15:1], AEN, BE3N, BE2N, BE1N, and BE0N.

Note that if the local device decoder is used in either synchronous or asynchronous transfers, LDEVN will be asserted to indicate that the KSZ8862M is successfully targeted. The signal LDEVN is a combinatorial decode of AEN and A[15:4].

3.3.1 ASYNCHRONOUS INTERFACE

For asynchronous transfers, the asynchronous dedicated signals RDN (for read) or WRN (for write) toggle, but the synchronous dedicated signals CYCLEN, SWR, and RDYRTNN are de-asserted and stay at the same logic level throughout the entire asynchronous transfer.

There is no data burst support for asynchronous transfer. All asynchronous transfers are single-data transfers. The BIU, however, provides flexible asynchronous interfacing to communicate with various applications and architectures. Three major ways of interfacing with the system (host) are.

- Interfacing with the system/host relying on local device decoding and having stable address throughout the whole transfer: The typical example for this application is ISA-like bus interface using latched address signals as shown in Figure 13. No additional address latch is required, therefore ADSN should be connected Low. The BIU decodes A[15:4] and qualifies with AEN (Address Enable) to determine if the KSZ8862M device is the intended target. The host utilizes the rising edge of RDN to latch read data and the BIU will use rising edge of WRN to latch write data.
- Interfacing with the system/host relying on local device decoding but not having stable address throughout the entire transfer: The typical example for this application is EISA-like bus (non-burst) interface as shown in Figure 14. This type of interface requires ADSN to latch the address on the rising edge. The BIU decodes latched A[15:4] and qualifies with AEN to determine if the KSZ8862M device is the intended target. The data transfer is the same as the first case.
- Interfacing with the system/host relying on central decoding (KSZ8862-32 mode only): The typical example for this application is for an embedded processor having a central decoder on the system board or within the processor. Connecting the chip select (CS) from system/host to DATACSN bypasses the local device decoder. When the DATACSN is asserted, it only allows access to the Data Register in 32 bits and BE3N, BE2N, BE1N, and BE0N are ignored as shown in Figure 7-2. No other registers can be accessed by asserting DATACSN. The data transfer is the same as in the first case. Independent of the type of asynchronous interface used. To insert a wait state, the BIU will assert ARDY to prolong the cycle.

3.3.2 SYNCHRONOUS INTERFACE

For synchronous transfers, the synchronous dedicated signals CYCLEN, SWR, and RDYRTNN will toggle but the asynchronous dedicated signals RDN and WRN are de-asserted and stay at the same logic level throughout the entire synchronous transfer.

The synchronous interface mainly supports two applications, one for VLBus-like and the other for EISA-like (DMA type C) burst transfers. The VLBus-like interface supports only single-data transfer. The pin option VLBUSN determines if it is a VLBus-like or EISA-like burst transfer. If VLBUSN = 0, the interface is for VLBus-like transfer; if VLBUSN = 1, the interface is for EISA-like burst transfer.

For VLBus-like transfer interface (VLBUSN = 0):

This interface is used in an architecture in which the device's local decoder is utilized; that is, the BIU decodes latched A[15:4] and qualifies with AEN (Address Enable) to determine if the KSZ8862M device is the intended target. No burst is supported in this application. The M/nIO signal connection in VLBus is routed to AEN. The CYCLEN in this application is used to sample the SWR signal when it is asserted. Usually, CYCLEN is one clock delay of ADSN. There is a handshaking process to end the cycle of VLBus-like transfers. When the KSZ8862M is ready to finish the cycle, it asserts SRDYN. The system/host acknowledges SRDYN by asserting RDYRTNN after the system/host has latched the read data. The KSZ8862M holds the read data until RDYRTNN is asserted. The timing waveform is shown in Figure 7-6 and Figure 7-7.

For EISA-like burst transfer interface (VLBUSN = 1):

The SWR is connected to IORC# in EISA to indicate the burst read and CYCLEN is connected to IOWC# in EISA to indicate the burst write. Note that in this application, both the system/host/memory and KSZ8862M are capable of inserting wait states. For system/host/memory to insert a wait state, assert the RDYRTNN signal; for the KSZ8862M to insert the wait state, assert the SRDYN signal. The timing waveform is shown in Figure 7-4 and Figure 7-5.

3.3.2.1 BIU Summation

Figure 3-6 shows the mapping from ISA-like, EISA-like and VLBus-like transactions to the chip's BIU.

Figure 3-7 shows the connection for different data bus sizes.

Note: For the 8-bit data bus mode, the internal inverter is enabled and connected between BE0N and BE1N, so an even address will enable the BE0N and an odd address will enable the BE1N.

FIGURE 3-6: MAPPING FROM THE ISA, EISA, AND VLBUS TO THE KSZ8862M BUS INTERFACE

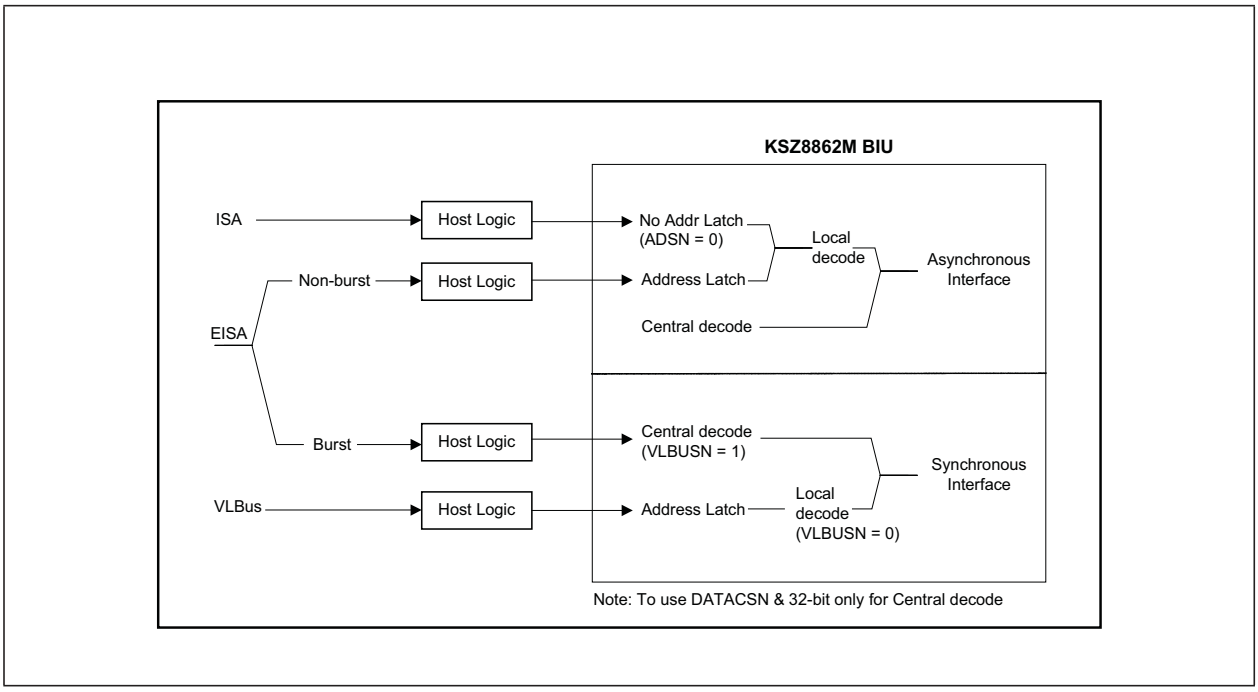
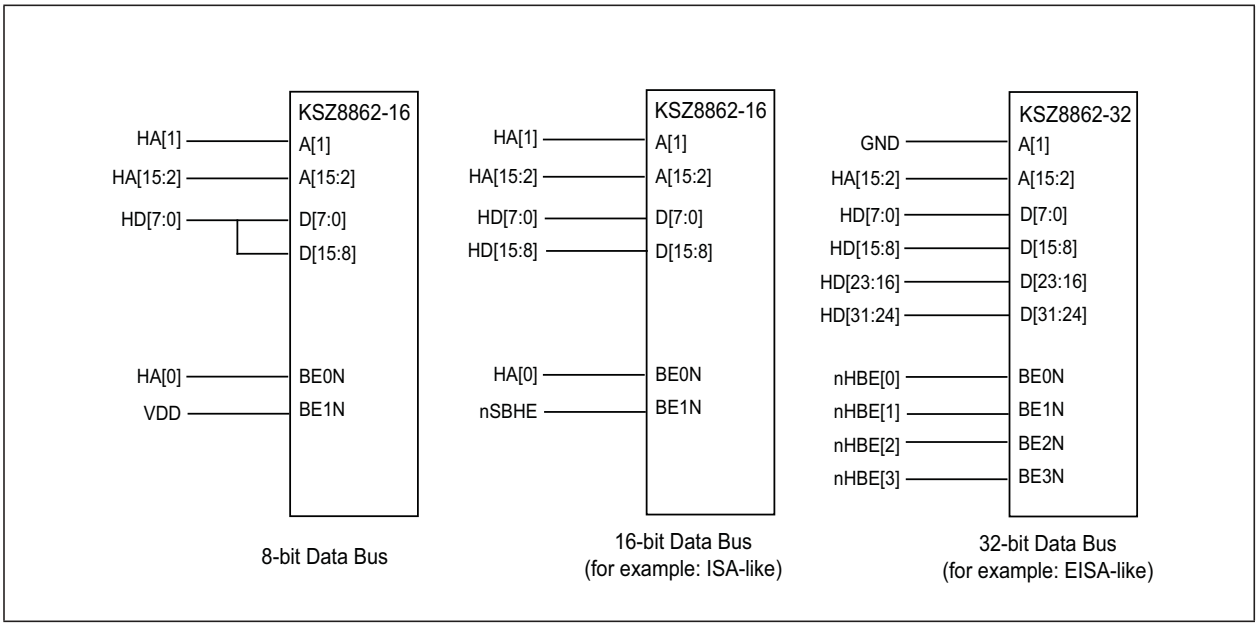


FIGURE 3-7: KSZ8862M 8-BIT, 16-BIT, AND 32-BIT DATA BUS CONNECTIONS



3.3.3 BIU IMPLEMENTATION PRINCIPLES

Because KSZ8862M is an I/O device with 16 addressable locations, address decoding is based on the values of A15-A4 and AEN. Whenever DATACSN is asserted, the address decoder is disabled and a 32-bit transfer to Data Register is assumed (BE3N – BE0N are ignored).

If address latching is required, the address is latched on the rising edge of ADSN and is transparent when ADSN = 0.

- Byte, word, and double word data buses and accesses (transfers) are supported.
- Internal byte swapping is not implemented and word swapping is supported internally. Refer to Figure 3-7 for the appropriate 8-bit, 16-bit, and 32-bit data bus connection.
- Because independent sets of synchronous and asynchronous signals are provided, synchronous and asynchronous cycles can be mixed or interleaved as long as they are not active simultaneously.
- The asynchronous interface uses RDN and WRN signal strobes for data latching. If necessary, ARDY is de-asserted on the leading edge of the strobe.
- The VLBUS-like synchronous interface uses BCLK, ADSN, and SWR and CYCLEN to control read and write operations and generate SRDYN to insert the wait state, if necessary, when VLBUSN = 0. For read, the data must be held until RDYRTNN is asserted.

The EISA-like burst transfer is supported using synchronous interface signals and DATACSN when I/O signal VLBUSN = 1. Both the system/host/memory and KSZ8862M are capable of inserting wait states. To set the system/host/memory to insert a wait state, assert RDYRTNN signal. To set the KSZ8862M to insert a wait state, assert SRDYN signal.

3.4 Queue Management Unit (QMU)

The Queue Management Unit (QMU) manages packet traffic between the MAC/PHY interface and the system host. It has built-in packet memory for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue). Each queue contains 4 KB of memory for back-to-back, non-blocking frame transfer performance. It provides a group of control registers for system control, frame status registers for current packet transmit/receive status, and interrupts to inform the host of the real time TX/RX status.

3.4.1 TRANSMIT QUEUE (TXQ) FRAME FORMAT

The frame format for the transmit queue is shown in Table 3-3. The first word contains the control information for the frame to transmit. The second word is used to specify the total number of bytes of the frame. The packet data follows. The packet data area holds the frame itself. It may or may not include the CRC checksum depending upon whether hardware CRC checksum generation is enabled.

Multiple frames can be pipelined in both the transmit queue and receive queue as long as there is enough queue memory, thus avoiding overrun. For each transmitted frame, the transmit status information for the frame is located in the TXSR register.

TABLE 3-3: FRAME FORMAT FOR TRANSMIT QUEUE

Packet Memory Address Offset	Bit 15 2nd Byte	Bit 0 1st Byte
0	Control Word	
2	Byte Count	
4 and up	Transmit Packet Data (maximum size is 1916)	

Because multiple packets can be pipelined into the TX packet memory for transmit, the transmit status reflects the status of the packet that is currently being transferred on the MAC interface, which may or may not be the last queued packet in the TX queue.

The transmit control word is the first 16-bit word in the TX packet memory, followed by a 16-bit byte count. It must be word aligned. Each control word corresponds to one TX packet. Table 3-4 gives the transmit control word bit fields.

TABLE 3-4: TRANSMIT CONTROL WORD BIT FIELDS

Bit	Description
15	TXIC Transmit Interrupt on Completion When this bit is set, the KSZ8862M sets the transmit interrupt after the present frame has been transmitted.
14 - 10	Reserved.
9 - 8	TXDPN Transmit Destination Port Number When bit is set, this field indicates the destination port(s) where the packet is forwarded from host system. Set bit 8 to indicate that port 1 is the destination port. Set bit 9 to indicate that port 2 is the destination port. Setting all ports to 1 causes the switch engine to broadcast the packet to both ports. Setting all bits to 0 has no effect. The internal switch engine forwards the packets according to the switching algorithm in its MAC lookup table.
7 - 6	Reserved.
5 - 0	TXFID Transmit Frame ID This field specifies the frame ID that is used to identify the frame and its associated status information in the transmit status register TXSR[5:0].

The transmit Byte Count specifies the total number of bytes to be transmitted from the TXQ. Its format is given in Table 3-5.

TABLE 3-5: TRANSMIT BYTE COUNT FORMAT

Bit	Description
15 - 11	Reserved.
10 - 0	TXBC Transmit Byte Count Transmit Byte Count. Hardware uses the byte count information to conserve the TX buffer memory for better utilization of the packet memory. Note: The hardware behavior is unknown if an incorrect byte count information is written to this field. Writing a 0 value to this field is not permitted.

The data area contains six bytes of Destination Address (DA) followed by six bytes of Source Address (SA), followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The KSZ8862M does not insert its own SA. The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the KSZ8862M. It is treated transparently as data both for transmit operations.

3.4.2 RECEIVE QUEUE (RXQ) FRAME FORMAT

The frame format for the receive queue is shown in Table 3-6. The first word contains the status information for the frame received. The second word is the total number of bytes of the RX frame. Following that is the packet data area. The packet data area holds the frame itself. It may or may not include the CRC checksum depending on whether hardware CRC stripping is enabled.

TABLE 3-6: FRAME FORMAT FOR RECEIVE QUEUE

Packet Memory Address Offset	Bit 15 2nd Byte — Bit 0 1st Byte
0	Status Word
2	Byte Count
4 and up	Receive Packet Data (maximum size is 1916)

For receive, the packet receive status always reflects the receive status of the packet received in the current RX packet memory (see Table 3-7). The RXSR register indicates the status of the current received frame.

TABLE 3-7: FRXQ RECEIVE PACKET STATUS

Bit	Description
15	RXFV Receive Frame Valid When set, this field indicates that the present frame in the receive packet memory is valid. The status information currently in this location is also valid. When bit is reset, indicates that there is either no pending receive frame or current frame is still in the process of receiving and has not completed yet.
14 - 10	Reserved.
9 - 8	RXSPN Receive Source Port Number When bit is set, this field indicates the source port where the packet was received. (Setting bit 9 = 0 and bit 8 = 1 indicates the packet was received from port 1. Setting bit 9 = 1 and bit 8 = 0 indicates that the packet was received from port 2. Valid port is either port 1 or port 2.
7	RXBF Receive Broadcast Frame When set, it indicates that this frame has a broadcast address.
6	RXMF Receive Multicast Frame When set, it indicates that this frame has a multicast address (including the broadcast address).
5	RXUF Receive Unicast Frame When set, it indicates that this frame has a unicast address.
4	Reserved.
3	RXFT Receive Frame Type When set, it indicates that the frame is an Ethernet-type frame (frame length is greater than 1500 bytes). When clear, it indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames.
2	RXTL Receive Frame Too Long When set, it indicates that the frame length exceeds the maximum size of 1518 bytes. Frames that are too long are passed to the host only if the pass bad frame bit is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.
1	RXRF Receive Runt Frame When set, it indicates that a frame was damaged by a collision or had a premature termination before the collision window passed. Runt frames are passed to the host only if the pass bad frame bit is set.
0	RXCE Receive CRC Error When set, it indicates that a CRC error has occurred on the current received frame. CRC error frames are passed to the host only if the pass bad frame bit is set.

Table 3-8 gives the format of the RX byte count field.

TABLE 3-8: FRXQ RX BYTE COUNT FIELD

Bit	Description
15 - 11	Reserved.
10 - 0	RXBC Receive Byte Count Receive Byte Count.

3.5 Advanced Switch Functions

3.5.1 SPANNING TREE SUPPORT

To support spanning tree, the host port is the designated port for the processor.

The other ports can be configured in one of the five spanning tree states via “transmit enable”, “receive enable” and “learning disable” register settings in registers P1CR2 and P2CR2 for ports 1 and 2, respectively. Table 3-9 shows the port setting and software actions taken for each of the five spanning tree states.

TABLE 3-9: SPANNING TREE STATES

State	Port Setting	Software Action
Disable State: The port should not forward or receive any packets. Learning is disabled.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “1”	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the Static MAC Address Table with “overriding bit” set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State: Only packets to the processor are forwarded.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “1”	The processor should not send any packets to the port(s) in this state. The processor should program the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State: Only packets to and from the processor are forwarded. Learning is disabled.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “1”	The processor should program the Static MAC Address TableStatic MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is disabled on the port in this state.
Learning State: Only packets to and from the processor are forwarded. Learning is enabled.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “0”	The processor should program the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is enabled on the port in this state.
Forwarding State Packets are forwarded and received normally. Learning is enabled.	Transmit enable = “1”, Receive enable = “1”, Learning disable = “0”	The processor programs the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. Address learning is enabled on the port in this state.

3.5.2 IGMP SUPPORT

For Internet Group Management Protocol (IGMP) support in Layer 2, the KSZ8862M provides two components:

3.5.2.1 "IGMP" Snooping

The KSZ8862M traps IGMP packets and forwards them only to the processor (host port). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

3.5.2.2 "Multicast Address Insertion" in the Static MAC Table

Once the multicast address is programmed in the Static MAC Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

3.5.2.3 IPv6 MLD Snooping

The KSZ8862M traps IPv6 Multicast Listener Discovery (MLD) packets and forwards them only to the processor (host port). MLD snooping is controlled by SGCR2 [13] (MLD snooping enable) and SGCR2 [12] (MLD option).

Setting SGCR2 [13] causes the KSZ8862M to trap packets that meet all of the following conditions:

- IPv6 multicast packets
- Hop count limit = 1
- IPv6 next header = 1 or 58 (or = 0 with hop-by-hop next header = 1 or 58)
- If SGCR2[12] = 1, IPv6 next header = 43, 44, 50, 51, or 60 (or = 0 with hop-by-hop next header = 43, 44, 50, 51, or 60)

3.5.3 PORT MIRRORING SUPPORT

KSZ8862M supports "Port Mirroring" comprehensively as:

3.5.3.1 "Receive Only" Mirror on a Port

All the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "receive sniff" and the host port is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8862M forwards the packet to both port 2 and the host port. The KSZ8862M can optionally even forward "bad" received packets to the "sniffer port".

3.5.3.2 "Transmit Only" Mirror on a Port

All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "transmit sniff" and the host port is programmed to be the "sniffer port". A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8862M forwards the packet to both port 1 and the host port.

3.5.3.3 "Receive and Transmit Only" Mirror on a Port

All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the "AND" feature, set register SGCR2, bit 8 to "1". For example, port 1 is programmed to be "receive sniff", port 2 is programmed to be "transmit sniff", and the host port is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8862M forwards the packet to both port 2 and the host port.

Multiple ports can be selected as "receive sniff" or "transmit sniff". In addition, any port can be selected as the "sniffer port". All these per port features can be selected through registers P1CR2, P2CR2, and P3CR2 for ports 1, 2, and the host port, respectively.

3.6 IEEE 802.1Q VLAN Support

The KSZ8862M supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8862M provides a 16-entry VLAN table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning (see Table 3-10 and Table 3-11).

TABLE 3-10: FID + DA LOOKUP IN VLAN MODE

DA Found in Static MAC Table	Use FID Flag	FID Match	DA+FID Found in Dynamic MAC Table	Action
No	Don't Care	Don't Care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
No	Don't Care	Don't Care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	0	Don't Care	Don't Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	1	Yes	Don't Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]

TABLE 3-11: FID + SA LOOKUP IN VLAN MODE

FID+SA Found in Dynamic MAC Table	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

3.7 QoS Priority Support

The KSZ8862M provides Quality of Service (QoS) for applications such as VoIP and video conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues: Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. Bit 0 of registers P1CR1, P2CR1, and P3CR1 is used to enable split transmit queues for ports 1, 2, and the host port, respectively.

3.7.1 PORT-BASED PRIORITY

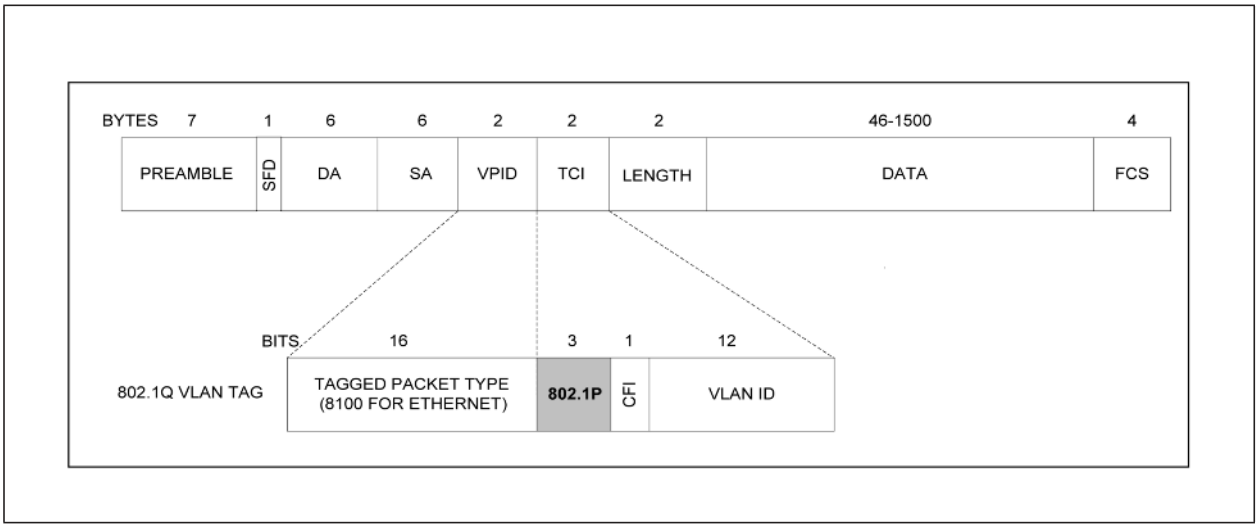
With port-based priority, each ingress port is individually classified as a specific priority level. All packets received at the high-priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits[4:3] of registers P1CR1, P2CR1, and P3CR1 is used to enable port-based priority for Ports 1, 2, and the host port, respectively.

3.7.2 802.1P-BASED PRIORITY

For 802.1p-based priority, the KSZ8862 examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and used to look up the "priority mapping" value, as specified by the register SGCR6. The "priority mapping" value is programmable.

Figure 3-8 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 3-8: 802.1P PRIORITY FIELD FORMAT



802.1p based priority is enabled by bit[5]of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively.

The KSZ8862M provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN protocol ID (VPID) and the 2 bytes tag control information field (TCI), is also referred to as the 802.1Q VLAN tag.

Tag insertion is enabled by bit [2] of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively. At the egress port, untagged packets are tagged with the ingress port's default tag. The default tags are programmed in register sets P1VIDCR, P2VIDCR, and P3VIDCR for Ports 1, 2, and the host port, respectively. The KSZ8862 does not add tags to already tagged packets.

Tag removal is enabled by bit [1] of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8862 will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

3.7.3 PRIORITY FIELD RE-MAPPING

This is a QoS feature that allows the KSZ8862M to set the "user priority ceiling" at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field. The "user priority ceiling" is enabled by bit[3] of registers P1CR2, P2CR2, and P3CR2 for Ports 1, 2, and the host port, respectively.

3.7.4 DIFFSERV-BASED PRIORITY

DiffServ-based priority uses the ToS registers shown in the Type-of-Service (ToS) Priority Control Registers section. The ToS priority control registers implement a fully-decoded, 128-bit differentiated services code point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

3.8 Rate-Limiting Support

The KSZ8862M supports hardware rate limiting from 64 Kbps to 99 Mbps, independently on the "receive side" and on the "transmit side" as per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up ingress rate control registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up egress rate control registers. The size of each frame has options to include minimum inter-frame gap (IFG) or preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8862M provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8862M counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the “leaky bucket” algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

3.8.1 MAC FILTERING FUNCTION

Use the static table to assign a dedicated MAC address to a specific port. When a unicast MAC address is not recorded in the static table, it is also not learned in the dynamic MAC table. The KSZ8862M includes an option that can filter or forward unicast packets for an unknown MAC address. This option is enabled by SGCR7 [7].

The unicast MAC address filtering function is useful in preventing the broadcast of unicast packets that could degrade the quality of this port in applications such as voice over Internet Protocol (VoIP).

3.8.2 CONFIGURATION INTERFACE

The KSZ8862M operates only as a managed switch.

3.8.3 EEPROM INTERFACE

It is optional in the KSZ8862M to use an external EEPROM. In the case that an EEPROM is not used, the EEEN pin must be tied Low or floating.

The external serial EEPROM with a standard microwire bus interface is used for non-volatile storage of information such as the host MAC address, base address, and default configuration settings. The KSZ8862M can detect if the EEPROM is a 1KB (93C46) or 4KB (93C66) EEPROM device (the 93C46 and the 93C66 are typical EEPROM devices). The EEPROM is organized as 16-bit mode.

If the EEEN pin is pulled high, the KSZ8862M performs an automatic read of the external EEPROM words 0H to 6H after the de-assertion of Reset. The EEPROM values are placed in certain host-accessible registers. EEPROM read/write functions can also be performed by software read/writes to the EEPCR registers.

The KSZ8862M EEPROM format is shown in Table 3-12.

TABLE 3-12: EEPROM FORMAT

Word	15:8	7:0
0h	Base Address	
1h	Host MAC Address Byte 2	Host MAC Address Byte 1
2h	Host MAC Address Byte 4	Host MAC Address Byte 3
3h	Host MAC Address Byte 6	Host MAC Address Byte 5
4h	Reserved	
5h	Reserved	
6h	ConfigParam (see Table 3-13)	
7h-3 fh	Not used for KSZ8862M (available for user to use)	

The format for ConfigParam is shown in Table 3-13.

TABLE 3-13: CONFIGPARAM WORD IN EEPROM FORMAT

Bit	Bit Name	Description
15 - 2	Reserved	Reserved
1	Clock Rate	Internal clock rate selection 0: 125 MHz 1: 25 MHz Note: At power up, this chip operates on 125 MHz clock. The internal frequency can be dropped to 25 MHz via the external EEPROM.
0	ASYN 8-bit	Async 8-bit or 16-bit bus select 1= bus is configured for 16-bit width 0= bus is configured for 8-bit width (32-bit width, KSZ8862-32, don't care this bit setting)

3.9 Loopback Support

The KSZ8862M provides loopback support for remote diagnostic of failure. In loopback mode, the speed at both PHY ports will be set to 100BASE-TX full-duplex mode. Two types of loopback are supported: Far-end Loopback and Near-end (Remote) Loopback.

3.9.1 NEAR-END (REMOTE) LOOPBACK

Near-end (Remote) loopback is conducted at PHY port 1 of the KSZ8862M. The loopback path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXPx/TXMx).

Bit [1] of registers P1PHYCTRL and P2PHYCTRL is used to enable near-end loopback for ports 1 and 2, respectively. Alternatively, Bit [9] of registers P1SCSLMD and P2SCSLMD can also be used to enable near-end loopback. The both ports 1 and 2 near-end loopback paths are illustrated Figure 3-9.

3.9.2 Far-End Loopback

Far-end loopback is conducted between the KSZ8862M's two PHY ports. The loopback path starts at the "Originating." PHY port's receive inputs (RXP/RXM), wraps around at the "loopback" PHY port's PMD/PMA, and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

Bit [8] of registers P1CR4 and P2CR4 is used to enable far-end loopback for ports 1 and 2, respectively. Alternatively, Bit [14] of registers P1MBCR and P2MBCR can also be used to enable far-end loopback. The port 2 far-end loopback path is illustrated in Figure 3-10.

FIGURE 3-9: PORT 1 AND PORT 2 NEAR-END (REMOTE) LOOPBACK PATH

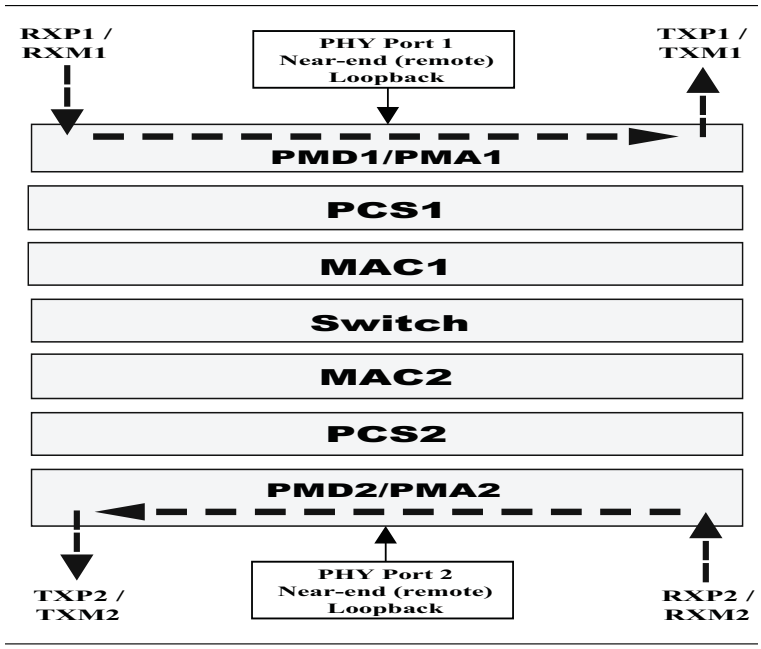
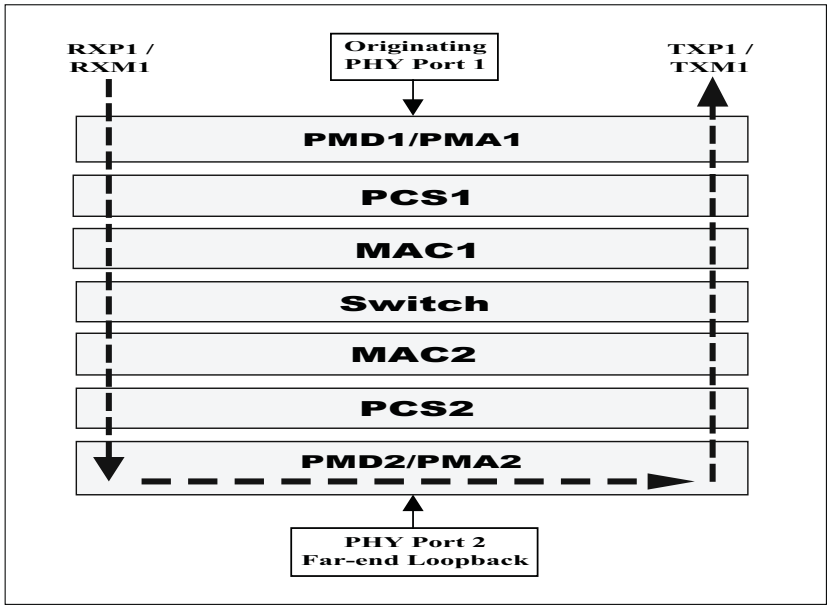


FIGURE 3-10: PORT 2 FAR-END LOOPBACK PATH



4.0 REGISTER DESCRIPTIONS

4.1 CPU Interface I/O Registers

The KSZ8862M provides an EISA-like, ISA-like, or VLBUS-like bus interface for the CPU to access its internal I/O registers. I/O registers serve as the address that the microprocessor uses when communicating with the device. This is used for configuring operational settings, reading or writing control, status information, and transferring packets by reading and writing through the packet data registers.

4.1.1 I/O REGISTERS

Input/Output (I/O) registers are limited to 16 locations as required by most ISA bus-based systems; therefore, registers are assigned to different banks. The last word of the I/O register locations (0xE - 0xF) is shared by all banks and can be used to change the bank in use.

The following I/O Space Mapping Tables apply to 8-, 16-, or 32-bit bus products. Depending upon the bus interface used and byte enable signals (BE[3:0]N control byte access), each I/O access can be performed as an 8-bit, 16-bit, or 32-bit operation. The KSZ8862M is not limited to 8/16-bit performance and 32-bit read/write are also supported.

TABLE 4-1: INTERNAL I/O SPACE MAPPING - BANK 0 TO BANK 7

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 0**	**Bank 1**	**Bank 2**	**Bank 3**	**Bank 4**	**Bank 5**	**Bank 6**	**Bank 7**
0x0 to 0x3	0x0 to 0x1	0x0	Base Address [7:0]	Reserved	Host MAC Address Low [7:0]	On-Chip Bus Control [7:0]	Reserved			
		0x1	Base Address [15:8]		Host MAC Address Low [15:8]	On-Chip Bus Control [15:8]				
	0x2 to 0x3	0x2	Reserved	Reserved	Host MAC Address Mid [7:0]	EEPROM Control [7:0]	Reserved			
		0x3			Host MAC Address Mid [15:8]	EEPROM Control [15:8]				
0x4 to 0x7	0x4 to 0x5	0x4	QMU RX Flow Control Watermark [7:0]	Reserved	Host MAC Address High [7:0]	Memory BIST Info [7:0]	Reserved			
		0x5	QMU RX Flow Control Watermark [15:8]		Host MAC Address High [15:8]	Memory BIST Info [15:8]				
	0x6 to 0x7	0x6	Bus Error Status [7:0]	Reserved	Reserved	Global Reset [7:0]	Reserved			
		0x7	Bus Error Status [15:8]			Global Reset [15:8]				
0x8 to 0xB	0x8 to 0x9	0x8	Bus Burst Length [7:0]	Reserved	Reserved	Power Management Capabilities [7:0]	Reserved			
		0x9	Bus Burst Length [15:8]			Power Management Capabilities [15:8]				
	0xA to 0xB	0xA	Reserved							
		0xB								
0xC to 0xF	0xC to 0xD	0xC	Reserved							
		0xD								
	0xE to 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

TABLE 4-2: INTERNAL I/O SPACE MAPPING - BANK 8 TO BANK 15

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 8	Bank 9	Bank 10	Bank 11	Bank 12	Bank 13	Bank 14	Bank 15
0x0 to 0x3	0x0 to 0x1	0x0	Reserved							
		0x1								
	0x2 to 0x3	0x2								
		0x3								
0x4 to 0x7	0x4 to 0x5	0x4								
		0x5								
	0x6 to 0x7	0x6								
		0x7								
0x8 to 0xB	0x8 to 0x9	0x8								
		0x9								
	0xA to 0xB	0xA								
		0xB								
0xC to 0xF	0xC to 0xD	0xC	Bank Select [7:0]							
		0xD								
	0xE to 0xF	0xE	Bank Select [15:8]							
		0xF								

TABLE 4-3: INTERNAL I/O SPACE MAPPING - BANK 16 TO BANK 23

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 16	Bank 17	Bank 18	Bank 19	Bank 20	Bank 21	Bank 22	Bank 23
0x0 to 0x3	0x0 to 0x1	0x0	Transmit Control [7:0]	TXQ Command [7:0]	Interrupt Enable [7:0]	Multicast Table 0 [7:0]	Reserved			
		0x1	Transmit Control [15:8]	TXQ Command [15:8]	Interrupt Enable [15:8]	Multicast Table 0 [15:8]				
	0x2 to 0x3	0x2	Transmit Status [7:0]	RXQ Command [7:0]	Interrupt Status [7:0]	Multicast Table 1 [7:0]	Reserved			
		0x3	Transmit Status [15:8]	RXQ Command [15:8]	Interrupt Status [15:8]	Multicast Table 1 [15:8]				
0x4 to 0x7	0x4 to 0x5	0x4	Receive Control [7:0]	TX Frame Data Pointer [7:0]	Receive Status [7:0]	Multicast Table 2 [7:0]	Reserved			
		0x5	Receive Control [15:8]	TX Frame Data Pointer [15:8]	Receive Status [15:8]	Multicast Table 2 [15:8]				
	0x6 to 0x7	0x6	Reserved	RX Frame Data Pointer [7:0]	Receive Byte Counter [7:0]	Multicast Table 3 [7:0]	Reserved			
		0x7		RX Frame Data Pointer [15:8]	Receive Byte Counter [15:8]	Multicast Table 3 [15:8]				

TABLE 4-3: INTERNAL I/O SPACE MAPPING - BANK 16 TO BANK 23 (CONTINUED)

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 16**	**Bank 17**	**Bank 18**	**Bank 19**	**Bank 20**	**Bank 21**	**Bank 22**	**Bank 23**
0x8 to 0xB	0x8 to 0x9	0x8	TXQ Memory Information [7:0]	QMU Data Low [7:0]	Early Transmit [7:0]	Power Management Control/Status [7:0]	Reserved			
		0x9	TXQ Memory Information [15:8]	QMU Data Low [15:8]	Early Transmit [15:8]	Power Management Control/Status [15:8]				
	0xA to 0xB	0xA	RXQ Memory Information [7:0]	QMU Data High [7:0]	Early Receive [7:0]	Reserved				
		0xB	RXQ Memory Information [15:8]	QMU Data High [15:8]	Early Receive [15:8]					
0xC to 0xF	0xC to 0xD	0xC	Reserved							
		0xD								
	0xE to 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

TABLE 4-4: INTERNAL I/O SPACE MAPPING - BANK 24 TO BANK 31

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 24	Bank 25	Bank 26	Bank 27	Bank 28	Bank 29	Bank 30	Bank 31
0x0 to 0x3	0x0 to 0x1	0x0	Reserved							
		0x1								
	0x2 to 0x3	0x2	Reserved							
		0x3								
0x4 to 0x7	0x4 to 0x5	0x4	Reserved							
		0x5								
	0x6 to 0x7	0x6	Reserved							
		0x7								
0x8 to 0xB	0x8 to 0x9	0x8	Reserved							
		0x9								
	0xA to 0xB	0xA	Reserved							
		0xB								
0xC to 0xF	0xC to 0xD	0xC	Bank Select [7:0]							
		0xD								
	0xE to 0xF	0xE	Bank Select [15:8]							
		0xF								

TABLE 4-5: INTERNAL I/O SPACE MAPPING - BANK 32 TO BANK 39

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 32	Bank 33	Bank 34	Bank 35	Bank 36	Bank 37	Bank 38	Bank 39
0x0 to 0x3	0x0 to 0x1	0x0	Switch ID and Enable [7:0]	Switch Global Control 6 [7:0]	Reserved					MAC Address 1 [7:0]
		0x1	Switch ID and Enable [15:8]	Switch Global Control 6 [15:8]						MAC Address 1 [15:8]
	0x2 to 0x3	0x2	Switch Global Control 1 [7:0]	Switch Global Control 7 [7:0]	Reserved					MAC Address 2 [7:0]
		0x3	Switch Global Control 1 [15:8]	Switch Global Control 7 [15:8]						MAC Address 2 [15:8]
0x4 to 0x7	0x4 to 0x5	0x4	Switch Global Control 2 [7:0]	Reserved						MAC Address 3 [7:0]
		0x5	Switch Global Control 2 [15:8]							MAC Address 3 [15:8]
	0x6 to 0x7	0x6	Switch Global Control 3 [7:0]	Reserved						
		0x7	Switch Global Control 3 [15:8]							

TABLE 4-5: INTERNAL I/O SPACE MAPPING - BANK 32 TO BANK 39 (CONTINUED)

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 32	Bank 33	Bank 34	Bank 35	Bank 36	Bank 37	Bank 38	Bank 39
0x8 to 0xB	0x8 to 0x9	0x8	Switch Global Control 4 [7:0]	Reserved						
		0x9	Switch Global Control 4 [15:8]							
	0xA to 0xB	0xA	Switch Global Control 5 [7:0]	Reserved						
		0xB	Switch Global Control 5 [15:8]							
0xC to 0xF	0xC to 0xD	0xC	Reserved							
		0xD								
	0xE to 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

TABLE 4-6: INTERNAL I/O SPACE MAPPING - BANK 40 TO BANK 47

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 40	Bank 41	Bank 42	Bank 43	Bank 44	Bank 45	Bank 46	Bank 47
0x0 to 0x3	0x0 to 0x1	0x0	TOS Priority Control 1 [7:0]	TOS Priority Control 7 [7:0]	Indirect Access Control. [7:0]	Reserved	Digital Test Status [7:0]	PHY1 MII-Register Basic Control [7:0]	PHY2 MII-Register Basic Control [7:0]	Reserved
		0x1	TOS Priority Control 1 [15:8]	TOS Priority Control 7 [15:8]	Indirect Access Control. [15:8]		Digital Test Status [15:8]	PHY1 MII-Register Basic Control [15:8]	PHY2 MII-Register Basic Control [15:8]	
	0x2 to 0x3	0x2	TOS Priority Control 2 [7:0]	TOS Priority Control 8 [7:0]	Indirect Access Data 1 [7:0]	Reserved	Analog Test Status [7:0]	PHY1 MII-Register Basic Status [7:0]	PHY2 MII-Register Basic Status [7:0]	PHY1 Special Control/ Status [7:0]
		0x3	TOS Priority Control 2 [15:8]	TOS Priority Control 8 [15:8]	Indirect Access Data 1 [15:8]		Analog Test Status [15:8]	PHY1 MII-Register Basic Status [15:8]	PHY2 MII-Register Basic Status [15:8]	PHY1 Special Control/ Status [15:8]
0x4 to 0x7	0x4 to 0x5	0x4	TOS Priority Control 3 [7:0]	Reserved	Indirect Access Data 2 [7:0]	Reserved	Digital Test Control [7:0]	PHY1 PHYID Low [7:0]	PHY2 PHYID Low [7:0]	PHY2 LinkMD® Control/ Status [7:0]
		0x5	TOS Priority Control 3 [15:8]		Indirect Access Data 2 [15:8]		Digital Test Control [15:8]	PHY1 PHYID Low [15:8]	PHY2 PHYID Low [15:8]	PHY2 LinkMD® Control/ Status [15:8]
	0x6 to 0x7	0x6	TOS Priority Control 4 [7:0]	Reserved	Indirect Access Data 3 [7:0]	Reserved	Analog Test Control 0 [7:0]	PHY1 PHYID High [7:0]	PHY2 PHYID High [7:0]	PHY2 Control/Status [7:0]
		0x7	TOS Priority Control 4 [15:8]		Indirect Access Data 3 [15:8]		Analog Test Control 0 [15:8]	PHY1 PHYID High [15:8]	PHY2-PHYID High [15:8]	PHY2 Control/Status [15:8]

TABLE 4-6: INTERNAL I/O SPACE MAPPING - BANK 40 TO BANK 47 (CONTINUED)

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 40	Bank 41	Bank 42	Bank 43	Bank 44	Bank 45	Bank 46	Bank 47
0x8 to 0xB	0x8 to 0x9	0x8	TOS Priority Control 5 [7:0]	Reserved	Indirect Access Data 4 [7:0]	Reserved	Analog Test Control 1 [7:0]	PHY1 A.N. Advertisement [7:0]	PHY2 A.N. Advertisement [7:0]	Reserved
		0x9	TOS Priority Control 5 [15:8]		Indirect Access Data 4 [15:8]		Analog Test Control 1 [15:8]	PHY1 A.N. Advertisement [15:8]	PHY2 A.N. Advertisement [15:8]	
	0xA to 0xB	0xA	TOS Priority Control 6 [7:0]	Reserved	Indirect Access Data 5 [7:0]	Reserved	Analog Test Control 2 [7:0]	PHY1 A.N. Link Partner Ability [7:0]	PHY2 A.N. Link Partner Ability [7:0]	Reserved
		0xB	TOS Priority Control 6 [15:8]		Indirect Access Data 5 [15:8]		Analog Test Control 2 [15:8]	PHY1 A.N. Link Partner Ability [15:8]	PHY2 A.N. Link Partner Ability [15:8]	
0xC to 0xF	0xC to 0xD	0xC	Reserved							
		0xD								
	0xE to 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

TABLE 4-7: INTERNAL I/O SPACE MAPPING - BANK 48 TO BANK 55

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 48	Bank 49	Bank 50	Bank 51	Bank 52	Bank 53	Bank 54	Bank 55
0x0 to 0x3	0x0 to 0x1	0x0	Port 1 Control 1 [7:0]	Port 1 PHY Special Control/ Status, LinkMD [7:0]	Port 2 Control 1 [7:0]	Port 2 PHY Special Control/ Status, LinkMD [7:0]	Host Port Control 1 [7:0]	Reserved		
		0x1	Port 1 Control 1 [15:8]	Port 1 PHY Special Control/ Status, LinkMD [15:8]	Port 2 Control 1 [15:8]	Port 2 PHY Special Control/ Status, LinkMD [15:8]	Host Port Control 1 [15:8]			
	0x2 to 0x3	0x2	Port 1 Control 2 [7:0]	Port 1 Control 4 [7:0]	Port 2 Control 2 [7:0]	Port 2 Control 4 [7:0]	Host Port Control 2 [7:0]	Reserved		
		0x3	Port 1 Control 2 [15:8]	Port 1 Control 4 [15:8]	Port 2 Control 2 [15:8]	Port 2 Control 4 [15:8]	Host Port Control 2 [15:8]			
0x4 to 0x7	0x4 to 0x5	0x4	Port 1 VID Control [7:0]	Port 1 Status [7:0]	Port 2 VID Control [7:0]	Port 2 Status [7:0]	Host Port VID Control [7:0]	Reserved		
		0x5	Port 1 VID Control [15:8]	Port 1 Status [15:8]	Port 2 VID Control [15:8]	Port 2 Status [15:8]	Host Port VID Control [15:8]			
	0x6 to 0x7	0x6	Port 1 Control 3 [7:0]	Reserved	Port 2 Control 3 [7:0]	Reserved	Host Port Control 3 [7:0]	Reserved		
		0x7	Port 1 Control 3 [15:8]		Port 2 Control 3 [15:8]		Host Port Control 3 [15:8]			

TABLE 4-7: INTERNAL I/O SPACE MAPPING - BANK 48 TO BANK 55 (CONTINUED)

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 48	Bank 49	Bank 50	Bank 51	Bank 52	Bank 53	Bank 54	Bank 55
0x8 to 0xB	0x8 to 0x9	0x8	Port 1 Ingress Rate Control [7:0]	Reserved	Port 2 Ingress Rate Control [7:0]	Reserved	Host Port Ingress Rate Control [7:0]	Reserved		
		0x9	Port 1 Ingress Rate Control [15:8]		Port 2 Ingress Rate Control [15:8]		Host Port Ingress Rate Control [15:8]			
	0xA to 0xB	0xA	Port 1 Egress Rate Control [7:0]	Reserved	Port 2 Egress Rate Control [7:0]	Reserved	Host Port Egress Rate Control [7:0]	Reserved		
		0xB	Port 1 Egress Rate Control [15:8]		Port 2 Egress Rate Control [15:8]		Host Port Egress Rate Control [15:8]			
0xC to 0xF	0xC to 0xD	0xC	Reserved							
		0xD								
	0xE to 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

TABLE 4-8: INTERNAL I/O SPACE MAPPING - BANK 56 TO BANK 63

I/O Register Location			Bank Location							
32-Bit	16-Bit	8-Bit	Bank 56	Bank 57	Bank 58	Bank 59	Bank 60	Bank 61	Bank 62	Bank 63
0x0 to 0x3	0x0 to 0x1	0x0	Reserved							
		0x1								
	0x2 to 0x3	0x2	Reserved							
		0x3								
0x4 to 0x7	0x4 to 0x5	0x4	Reserved							
		0x5								
	0x6 to 0x7	0x6	Reserved							
		0x7								
0x8 to 0xB	0x8 to 0x9	0x8	Reserved							
		0x9								
	0xA to 0xB	0xA	Reserved							
		0xB								
0xC to 0xF	0xC to 0xD	0xC	Reserved							
		0xD								
	0xE to 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

4.2 Register Map: MAC and PHY

Do not write to bit values or to registers defined as Reserved. Manipulating reserved bits or registers causes unpredictable and often fatal results. If the user wants to write to these reserved bits, the user has to read back these reserved bits (RO or RW) first, then “OR” with the read value of the reserved bits and write back to these reserved bits.

Bit Type Definitions

- RO = Read only.
- RW = Read/Write.
- W1C = Write 1 to Clear (writing a one to this bit clears it).

Bank 0-63 Bank Select Register (0x0E): BSR (Same Location in all Banks)

The bank select register is used to select or to switch between different sets of register banks for I/O access. There are a total of 64 banks available to select, including the built-in switch engine registers.

TABLE 4-9: BANK 0-63 BANK SELECT REGISTER (0X0E)

Bit	Default Value	R/W	Description
15 - 6	0x000	RO	Reserved
5 - 0	0x00	R/W	**BSA Bank Select Address Bits** BSA bits select the I/O register bank in use. This register is always accessible regardless of the register bank currently selected. Notes: The bank select register can be accessed as a doubleword (32-bit) at offset 0xC, as a word (16-bit) at offset 0xE, or as a byte (8-bit) at offset 0xE. A doubleword write to offset 0xC writes to the BANK Select Register but does not write to registers 0xC and 0xD; it only writes to register 0xE.

Bank 0 Base Address Register (0x00): BAR

This register holds the base address for decoding a device access. Its value is loaded from the external EEPROM (0x0H) upon a power-on reset if the EEPROM Enable (EEEN) pin is tied to High. Its value can also be modified after reset. Writing to this register does not store the value into the EEPROM. When the EEEN pin is tied to Low, the default base address is 0x300.

TABLE 4-10: BANK 0 BASE ADDRESS REGISTER (0X00)

Bit	Default Value	R/W	Description
15 - 8	0x03 if EEEN is Low or the value from EEPROM if EEEN is High	R/W	**BARH Base Address High** These bits are compared against the address on the bus ADDR[15:8] to determine the BASE for the KSZ8862M registers.
7 - 5	0x00 if EEEN is Low or the value from EEPROM if EEEN is High	R/W	**BARL Base Address Low** These bits are compared against the address on the bus ADDR[7:5] to determine the BASE for the KSZ8862M registers.
4 - 0	0x00	RO	Reserved

Bank 0 QMU RX Flow Control High Watermark Configuration Register (0x04): QRFCR

This register contains the user defined QMU RX Queue high watermark configuration bit as below.

TABLE 4-11: BANK 0 QMU RX FLOW CONTROL HIGH WATERMARK CONFIGURATION REGISTER (0X04)

Bit	Default Value	R/W	Description
15 - 13	0x0	RO	Reserved
12	0	R/W	**QMU RX Flow Control High Watermark Configuration** 0 = 3 KBytes 1 = 2 KBytes
11 - 0	0x000	RO	Reserved

Bank 0 Bus Error Status Register (0x06): BESR

This register flags the different kinds of errors on the host bus.

TABLE 4-12: BANK 0 BUS ERROR STATUS REGISTER (0X06)

Bit	Default Value	R/W	Description
15	0	RO	**IBEC Illegal Byte Enable Combination** 1 = Illegal byte enable combination occurs. The illegal combination value can be found from bit 14 to bit 11. 0 = Legal byte enable combination. Write 1 to clear.
14 - 11	—	RO	**IBECV Illegal Byte Enable Combination Value** Bit 14 = Byte enable 3. Bit 13 = Byte enable 2. Bit 12 = Byte enable 1. Bit 11 = Byte enable 0. This value is valid only when bit 15 is set to 1.
10	0	RO	**SSAXFER Simultaneous Synchronous and Asnychronous Transfers** 1 = Synchronous and Asnychronous Transfers occur simultaneously. 0 = Normal. Write 1 to clear.
9 - 0	0x000	RO	Reserved

Bank 0 Bus Burst Length Register (0x08): BBLR

Before the burst can be sent, the burst length needs to be programmed.

TABLE 4-13: BANK 0 BUS BURST LENGTH REGISTER (0X08)

Bit	Default Value	R/W	Description
15	0	RO	Reserved
14 - 12	0x0	R/W	**BRL Burst Length (for burst read and write)** 000: single. 011: fixed burst read length of 4. 101: fixed burst read length of 8. 111: fixed burst read length of 16.
11 - 0	0x000	RO	Reserved

Bank 1: Reserved

Except Bank Select Register (0xE).

Bank 2 Host MAC Address Register Low (0x00): MARL

This register along with the other two Host MAC address registers are loaded starting at word location 0x1 of the EEPROM upon hardware reset. The software driver can modify the register, but it will not modify the original Host MAC address value in the EEPROM. These six bytes of Host MAC address in external EEPROM are loaded to these three registers as mapping below:

- MARL[15:0] = EEPROM 0x1(MAC Byte 2 and 1)
- MARM[15:0] = EEPROM 0x2(MAC Byte 4 and 3)
- MARH[15:0] = EEPROM 0x3(MAC Byte 6 and 5)

The Host MAC address is used to define the individual destination address that the KSZ8841M responds to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received from right to left (LSB to MSB). For example, the actual transmitted and received bits are on the order of 10000000 11000100 10100010 11100110 10010001 11010101. These three registers value for Host MAC address 01:23:45:67:89:AB will be held as below:

- MARL[15:0] = 0x89AB
- MARM[15:0] = 0x4567
- MARH[15:0] = 0x0123

The following table shows the register bit fields:

TABLE 4-14: BANK 2 HOST MAC ADDRESS REGISTER LOW (0X00)

Bit	Default Value	R/W	Description
15 - 0	—	R/W	**MARL MAC Address Low** The least significant word of the MAC address.

Bank 2 Host MAC Address Register Middle (0x02): MARM

The following table shows the register bit fields for middle word of Host MAC address.

TABLE 4-15: BANK 2 HOST MAC ADDRESS REGISTER MIDDLE (0X02)

Bit	Default Value	R/W	Description
15 - 0	—	R/W	**MARM MAC Address Middle** The middle word of the MAC address.

Bank 2 Host MAC Address Register High (0x04): MARH

The following table shows the register bit fields for high word of Host MAC address.

TABLE 4-16: BANK 2 HOST MAC ADDRESS REGISTER HIGH (0X04)

Bit	Default Value	R/W	Description
15 - 0	—	R/W	**MARH MAC Address High** The Most significant word of the MAC address.

Bank 3 On-Chip Bus Control Register (0x00): OBCR

This register controls the on-chip bus speed for the KSZ8862M. It is used for power management when the external host CPU is running at a slow frequency. The default of the on-chip bus speed is 125 MHz without EEPROM. When the external host CPU is running at a higher clock rate, the on-chip bus should be adjusted for the best performance.

TABLE 4-17: BANK 3 ON-CHIP BUS CONTROL REGISTER (0X00)

Bit	Default Value	R/W	Description
15 - 2	—	RO	Reserved
1 - 0	0x0	R/W	**OBSC On-Chip Bus Speed Control** 00 = 125 MHz. 01 = 62.5 MHz. 10 = 41.66 MHz. 11 = 25 MHz. Note: When external EEPROM is enabled, the bit 1 in Configparm word (0x6H) is used to control this speed as below: Bit 1 = 0, this value will be 00 for 125 MHz. Bit 1 = 1, this value will be 11 for 25 MHz. (User still can write these two bits to change speed after EEPROM data loaded)

Bank 3 EEPROM Control Register (0x02): EEPCR

To support an external EEPROM, tie the EEPROM Enable (EEEN) pin to High; otherwise, tie it to Low. If an external EEPROM is not used, the default chip Base Address (0x300), and the software programs the host MAC address. If an EEPROM is used in the design (EEPROM Enable pin to High), the chip Base Address and host MAC address are loaded from the EEPROM immediately after reset. The KSZ8841M allows the software to access (read and write) the EEPROM directly; that is, the EEPROM access timing can be fully controlled by the software if the EEPROM Software Access bit is set.

TABLE 4-18: BANK 3 EEPROM CONTROL REGISTER (0X02)

Bit	Default Value	R/W	Description
15 - 5	—	RO	Reserved
4	0	R/W	**EESA EEPROM Software Access** 1 = Enable software to access EEPROM through bit 3 to bit 0. 0 = Disable software to access EEPROM.
3	—	RO	**EECB EEPROM Status Bit** Data Receive from EEPROM. This bit directly reads the EEDI pin.
2 - 0	0x0	R/W	**EECB EEPROM Control Bits** Bit 2 = Data Transmit to EEPROM. This bit directly controls the device's EEDO pin. Bit 1 = Serial Clock. This bit directly controls the device's EESK pin. Bit 0 = Chip Select for EEPROM. This bit directly controls the device's EECS pin.

Bank 3 Memory BIST Info Register (0x04): MBIR

TABLE 4-19: BANK 3 MEMORY BIST INFO REGISTER (0X04)

Bit	Default Value	R/W	Description
15 - 13	0x0	RO	Reserved
12	—	RO	**TXMBF TX Memory BIST Finish** When set, it indicates the Memory Built In Self Test completion for the TX Memory.
11	—	RO	**TXMBFA TX Memory BIST Fail** When set, it indicates the Memory Built In Self Test has failed.
10 - 5	—	RO	Reserved
4	—	RO	**RXMBF RX Memory BIST Finish** When set, it indicates the Memory Built In Self Test completion for the RX Memory.
3	—	RO	**RXMBFA RX Memory BIST Fail** When set, it indicates the Memory Built In Self Test has failed.
2 - 0	—	RO	Reserved

Bank 3 Global Reset Register (0x06): GRR

This register controls the global reset function with information programmed by the CPU.

TABLE 4-20: BANK 3 GLOBAL RESET REGISTER (0X06)

Bit	Default Value	R/W	Description
15 - 1	0x0000	RO	Reserved
0	0	R/W	**Global Soft Reset** 1 = Software reset is active. 0 = Software reset is inactive. Software reset will affect PHY, MAC, QMU, DMA, and the switch core, only the BIU (base address registers) remains unaffected by a software reset.

Bank 3 Bus Configuration Register (0x08): BCFG

This register is a read-only register. The bit 0 is automatically downloaded from bit 0 Configparm word of EEPROM, if pin EEEN is high (enabled EEPROM).

TABLE 4-21: BUS CONFIGURATION REGISTER (0X08)

Bit	Default Value	R/W	Description
15 - 1	0x0000	RO	Reserved
0	—	RO	**Bus Configuration (only for KSZ8862-16 device)** 1 = Bus width is 16 bits. 0 = Bus width is 8 bits. (this bit is only available when EEPROM is enabled)

Banks 4 - 15: Reserved

Except Bank Select Register (0xE).

Bank 16 Transmit Control Register (0x00): TXCR

This register holds control information programmed by the CPU to control the QMU transmit module function.

TABLE 4-22: BANK 16 TRANSMIT CONTROL REGISTER (0X00)

Bit	Default Value	R/W	Description
15	—	RO	Reserved
14	0x0	RO	Reserved
13	0x0	RO	Reserved
12 - 4	—	RO	Reserved
3	0x0	R/W	**TXFCE Transmit Flow Control Enable** When this bit is set, the QMU sends flow control pause frames from the host port if the RX FIFO has reached its threshold. Note: the SGCR3[5] in Bank 32 also needs to be enabled.
2	0x0	R/W	**TXPE Transmit Padding Enable** When this bit is set, the KSZ8862M automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit requires enabling the add CRC feature to avoid CRC errors for the transmit packet.
1	0x0	R/W	**TXCE Transmit CRC Enable** When this bit is set, the KSZ8862M automatically adds a CRC checksum field to the end of a transmit frame.
0	0x0	R/W	**TXE Transmit Enable** When this bit is set, the transmit module is enabled and placed in a running state. When reset, the transmit process is placed in the stopped state after the transmission of the current frame is completed.

Bank 16 Transmit Status Register (0x02): TXSR

This register keeps the status of the last transmitted frame.

TABLE 4-23: BANK 16 TRANSMIT STATUS REGISTER (0X02)

Bit	Default Value	R/W	Description
15 - 6	0x000	RO	Reserved
5 - 0	—	RO	**TXFID Transmit Frame ID** This field identifies the transmitted frame. All of the transmit status information in this register belongs to the frame with this ID.

Bank 16 Receive Control Register (0x04): RXCR

This register holds control information programmed by the CPU to control the receive function.

TABLE 4-24: BANK 16 RECEIVE CONTROL REGISTER (0X04)

Bit	Default Value	R/W	Description
15 - 11	—	RO	Reserved
10	0x0	R/W	**RXFCE Receive Flow Control Enable** When this bit is set, the KSZ8862M will acknowledge a PAUSE frame from the receive interface; i.e., the outgoing packets are pending in the transmit buffer until the PAUSE frame control timer expires. When this bit is cleared, flow control is not enabled.
9	0x0	R/W	**RXEFE Receive Error Frame Enable** When this bit is set, CRC error frames are allowed to be received into the RX queue. When this bit is cleared, all CRC error frames are discarded.
8	—	RO	Reserved
7	0x0	R/W	**RXBE Receive Broadcast Enable** When this bit is set, the RX module receives all the broadcast frames.
6	0x0	R/W	**RXME Receive Multicast Enable** When this bit is set, the RX module receives all the multicast frames (including broadcast frames).
5	0x0	R/W	**RXUE Receive Unicast** When this bit is set, the RX module receives unicast frames that match the 48-bit Station MAC address of the module.
4	0x0	R/W	**RXRA Receive All** When this bit is set, the KSZ8862M receives all incoming frames, regardless of the frame's destination address.
3	0x0	R/W	**RXSCE Receive Strip CRC** When this bit is set, the KSZ8862M strips the CRC on the received frames. Once cleared, the CRC is stored in memory following the packet.
2	0x0	R/W	**QMU Receive Multicast Hash-Table Enable** When this bit is set, this bit enables the RX function to receive multicast frames that pass the CRC Hash filtering mechanism.
1	—	RO	Reserved
0	0x0	R/W	**RXE Receive Enable** When this bit is set, the RX block is enabled and placed in a running state. When reset, the receive process is placed in the stopped state upon completing reception of the current frame.

Bank 16 TXQ Memory Information Register (0x08): TXMIR

This register indicates the amount of free memory available in the TXQ of the QMU module.

TABLE 4-25: BANK 16 TXQ MEMORY INFORMATION REGISTER (0X08)

Bit	Default Value	R/W	Description
15 - 13	—	RO	Reserved
12 - 0	—	RO	**TXMA Transmit Memory Available** The amount of memory available is represented in units of byte. The TXQ memory is used for both frame payload, control word. Note: Software must be written to ensure that there is enough memory for the next transmit frame including control information before transmit data is written to the TXQ.

Bank 16 RXQ Memory Information Register (0x0A): RXMIR

This register indicates the amount of receive data available in the RXQ of the QMU module.

TABLE 4-26: BANK 16 RXQ MEMORY INFORMATION REGISTER (0X0A)

Bit	Default Value	R/W	Description
15 - 13	—	RO	Reserved
12 - 0	—	RO	**RXMA Receive Packet Data Available** The amount of Receive packet data available is represented in units of byte. The RXQ memory is used for both frame payload, status word. There is total 4096 bytes in RXQ. This counter will update after a complete packet is received and also issues an interrupt when receive interrupt enable IER[13] in Bank 18 is set. Note: Software must be written to empty the RXQ memory to allow for the new RX frame. If this is not done, the frame may be discarded as a result of insufficient RXQ memory.

Bank 17 TXQ Command Register (0x00): TXQCR

This register is programmed by the Host CPU to issue a transmit command to the TXQ. The present transmit frame in the TXQ memory is queued for transmit.

TABLE 4-27: BANK 17 TXQ COMMAND REGISTER (0X00)

Bit	Default Value	R/W	Description
15 - 1	—	RO	Reserved
0	0x0	R/W	**TXETF Enqueue TX Frame** When this bit is written as 1, the current TX frame prepared in the TX buffer is queued for transmit. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before setting up another new TX frame.

Bank 17 RXQ Command Register (0x02): RXQCR

This register is programmed by the Host CPU to issue release command to the RXQ. The current frame in the RXQ frame buffer is read only by the host and the memory space is released.

TABLE 4-28: BANK 17 RXQ COMMAND REGISTER (0X02)

Bit	Default Value	R/W	Description
15 - 1	—	RO	Reserved
0	0x0	R/W	**RXRRF Release RX Frame** When this bit is written as 1, the current RX frame buffer is released. Note: This bit is self-clearing after the frame memory is released. The software should wait for the bit to be cleared before processing new RX frame.

Bank 17 TX Frame Data Pointer Register (0x04): TXFDPR

The value of this register determines the address to be accessed within the TXQ frame buffer. When the AUTO increment is set, It will automatically increment the pointer value on Write accesses to the data register.

The counter is incremented by one for every byte access, by two for every word access, and by four for every double word access.

TABLE 4-29: BANK 17 TX FRAME DATA POINTER REGISTER (0X04)

Bit	Default Value	R/W	Description
15	—	RO	Reserved
14	0x0	R/W	**TXFPAI TX Frame Data Pointer Auto Increment** When this bit is set, the TX Frame data pointer register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every doubleword access. When this bit is reset, the TX frame data pointer is manually controlled by user to access the TX frame location.
13 - 11	—	RO	Reserved
10 - 0	0x0	R/W	**TXFP TX Frame Pointer** TX Frame Pointer index to the Frame Data register for access. This field reset to next available TX frame location when the TX Frame Data has been enqueued through the TXQ command register.

Bank 17 RX Frame Data Pointer Register (0x06): RXFDPR

The value of this register determines the address to be accessed within the RXQ frame buffer. When the Auto Increment is set, it will automatically increment the RXQ Pointer on read accesses to the data register.

The counter is incremented is by one for every byte access, by two for every word access, and by four for every double word access.

TABLE 4-30: BANK 17 RX FRAME DATA POINTER REGISTER (0X06)

Bit	Default Value	R/W	Description
15	—	RO	Reserved
14	0x0	R/W	**RXFPAI RX Frame Pointer Auto Increment** When this bit is set, the RXQ Address register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every double word access. When this bit is reset, the RX frame data pointer is manually controlled by user to access the RX frame location.
13 - 11	—	RO	Reserved
10 - 0	0x000	R/W	**RXFP RX Frame Pointer** RX Frame data pointer index to the Data register for access. This field reset to next available RX frame location when RX Frame release command is issued (through the RXQ command register).

Bank 17 QMU Data Register Low (0x08): QDRL

This register QDRL(0x08-0x09) contains the Low data word presently addressed by the pointer register. Reading maps from the RXQ, and writing maps to the TXQ.

TABLE 4-31: BANK 17 QMU DATA REGISTER LOW (0X08)

Bit	Default Value	R/W	Description
15 - 0	—	R/W	**QDRL Queue Data Register Low** This register is mapped into two uni-directional buffers for 16-bit buses, and one uni-directional buffer for 32-bit buses, (TXQ when Write, RXQ when Read) that allow moving words to and from the KSZ8862M regardless of whether the pointer is even, odd, or Dword aligned. Byte, word, and Dword access can be mixed on the fly in any order. This register along with DQRH is mapped into two consecutive word locations for 16-bit buses, or one word location for 32-bit buses, to facilitate Dword move operations.

Bank 17 QMU Data Register High (0x0A): QDRH

This register QDRH(0x0A-0x0B) contains the High data word presently addressed by the pointer register. Reading maps from the RXQ, and writing maps to the TXQ.

TABLE 4-32: BANK 17 QMU DATA REGISTER HIGH (0X0A)

Bit	Default Value	R/W	Description
15 - 0	—	R/W	**QDRL Queue Data Register High** This register is mapped into two uni-directional buffers for 16-bit buses, and one uni-directional buffer for 32-bit buses, (TXQ when Write, RXQ when Read) that allow moving words to and from the KSZ8862M regardless of whether the pointer is even, odd, or Dword aligned. Byte, word, and Dword access can be mixed on the fly in any order. This register along with DQRL is mapped into two consecutive word locations for 16-bit buses, or one word location for 32-bit buses, to facilitate Dword move operations.

Bank 18 Interrupt Enable Register (0x00): IER

This register enables the interrupts from the QMU and other sources.

TABLE 4-33: BANK 18 INTERRUPT ENABLE REGISTER (0X00)

Bit	Default Value	R/W	Description
15	0x0	R/W	**LCIE Link Change Interrupt Enable** When this bit is set, the link change interrupt is enabled. When this bit is reset, the link change interrupt is disabled.
14	0x0	R/W	**TXIE Transmit Interrupt Enable** When this bit is set, the transmit interrupt is enabled. When this bit is reset, the transmit interrupt is disabled.
13	0x0	R/W	**RXIE Receive Interrupt Enable** When this bit is set, the receive interrupt is enabled. When this bit is reset, the receive interrupt is disabled.
12	0x0	R/W	Reserved
11	0x0	R/W	**RXOIE Receive Overrun Interrupt Enable** When this bit is set, the Receive Overrun interrupt is enabled. When this bit is reset, the Receive Overrun interrupt is disabled.
10	0x0	R/W	Reserved
9	0x0	R/W	**TXPSIE Transmit Process Stopped Interrupt Enable** When this bit is set, the Transmit Process Stopped interrupt is enabled. When this bit is reset, the Transmit Process Stopped interrupt is disabled.
8	0x0	R/W	**RXPSIE Receive Process Stopped Interrupt Enable** When this bit is set, the Receive Process Stopped interrupt is enabled. When this bit is reset, the Receive Process Stopped interrupt is disabled.
7	0x0	R/W	**RXEFIE Receive Error Frame Interrupt Enable** When this bit is set, the Receive error frame interrupt is enabled. When this bit is reset, the Receive error frame interrupt is disabled.
6 - 0	—	RO	Reserved

Bank 18 Interrupt Status Register (0x02): ISR

This register contains the status bits for all QMU and other interrupt sources.

When the corresponding enable bit is set, it causes the interrupt pin to be asserted.

This register is usually read by the host CPU and device drivers during interrupt service routine or polling. The register bits are not cleared when read. The user has to write “1” to clear.

TABLE 4-34: BANK 18 INTERRUPT STATUS REGISTER (0X02)

Bit	Default Value	R/W	Description
15	0x0	RO (W1C)	**LCIS Link Change Interrupt Status** When this bit is set, it indicates that the link status has changed from link up to link down, or link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
14	0x0	RO (W1C)	**TXIS Transmit Status** When this bit is set, it indicates that the TXQ MAC has transmitted at least a frame on the MAC interface and the QMU TXQ is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.

TABLE 4-34: BANK 18 INTERRUPT STATUS REGISTER (0X02) (CONTINUED)

Bit	Default Value	R/W	Description
13	0x0	RO (W1C)	**RXIS Receive Interrupt Status** When this bit is set, it indicates that the QMU RXQ has received a frame from the MAC interface and the frame is ready for the host CPU to process. This edge-triggered interrupt status is cleared by writing 1 to this bit.
12	0x0	RO	Reserved
11	0x0	RO (W1C)	**RXOIS Receive Overrun Interrupt Status** When this bit is set, it indicates that the Receive Overrun status has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
10	0x0	RO	Reserved
9	0x1	RO (W1C)	**TXPSIE Transmit Process Stopped Status** When this bit is set, it indicates that the Transmit Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
8	0x1	RO (W1C)	**RXPSIE Receive Process Stopped Status** When this bit is set, it indicates that the Receive Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
7	0x0	RO (W1C)	RXEFIE Receive Error Frame Interrupt Status When this bit is set, it indicates that the Receive error frame status has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
6 - 0	—	RO	Reserved

Bank 18 Receive Status Register (0x04): RXSR

This register indicates the status of the current received frame and mirrors the Receive Status word of the Receive Frame in the RXQ.

TABLE 4-35: BANK 18 RECEIVE STATUS REGISTER (0X04)

Bit	Default Value	R/W	Description
15	—	RO	**RXFV Receive Frame Valid** When set, it indicates that the present frame in the receive packet memory is valid. The status information currently in this location is also valid. When clear, it indicates that there is either no pending receive frame or that the current frame is still in the process of receiving.
14 - 10	—	RO	Reserved
9 - 8	—	RO	**RXSPN Receive Source Port Number** When bit is set, this field indicates the source port where the packet was received. (Setting bit 9 = 0 and bit 8 = 1 indicates the packet was received from port 1. Setting bit 9 = 1 and bit 8 = 0 indicates that the packet was received from port 2. Valid port is either port 1 or port 2.
7	—	RO	**RXBF Receive Broadcast Frame** When set, it indicates that this frame has a broadcast address.
6	—	RO	**RXMF Receive Multicast Frame** When set, it indicates that this frame has a multicast address (including the broadcast address).
5	—	RO	**RXUF Receive Unicast Frame** When set, it indicates that this frame has a unicast address.
4	—	RO	Reserved

TABLE 4-35: BANK 18 RECEIVE STATUS REGISTER (0X04) (CONTINUED)

Bit	Default Value	R/W	Description
3	—	RO	**RXFT Receive Frame Type** When set, it indicates that the frame is an Ethernet-type frame (frame length is greater than 1500 bytes). When clear, it indicate that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames.
2	—	RO	**RXTL Receive Frame Too Long** When set, it indicates that the frame length exceeds the maximum size of 1916 bytes. Frames that are too long are passed to the host only if the pass bad frame bit is set (bit 9 in RXCR register). Note: Frame too long is only a frame length indication and does not cause any frame truncation.
1	—	RO	**RXRF Receive Runt Frame** When set, it indicates that a frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed to the host only if the pass bad frame bit is set (bit 9 in RXCR register).
0	—	RO	**RXCE Receive CRC Error** When set, it indicates that a CRC error has occurred on the current received frame. A CRC error frame is passed to the host only if the pass bad frame bit is set (bit 9 in RXCR register)

Bank 18 Receive Byte Count Register (0x06): RXBC

This register indicates the status of the current received frame and mirrors the Receive Byte Count word of the Receive Frame in the RXQ.

TABLE 4-36: BANK 18 RECEIVE BYTE COUNT REGISTER (0X06)

Bit	Default Value	R/W	Description
15 - 11	—	RO	Reserved
10 - 0	—	RO	RXBC Receive Byte Count Receive byte count.

Bank 19 Multicast Table Register 0 (0x00): MTR0

The 64-bit multicast table is used for group address filtering. This value is defined as the six most significant bits from CRC circuit calculation result that is based on 48-bit of DA input. The two most significant bits select one of the four registers to be used, while the others determine which bit within the register.

TABLE 4-37: BANK 19 MULTICAST TABLE REGISTER 0 (0X00)

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	**MTR0 Multicast Table 0** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Bank 19 Multicast Table Register 1 (0x02): MTR1

TABLE 4-38: BANK 19 MULTICAST TABLE REGISTER 1 (0X02)

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	**MTR0 Multicast** Table 3-1 When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Bank 19 Multicast Table Register 2 (0x04): MTR2

TABLE 4-39: BANK 19 MULTICAST TABLE REGISTER 2 (0X04)

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	**MTR0 Multicast** Table 3-2 When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Bank 19 Multicast Table Register 3 (0x06): MTR3

TABLE 4-40: BANK 19 MULTICAST TABLE REGISTER 3 (0X06)

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	**MTR0 Multicast** Table 3-3 When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Banks 20 – 31: Reserved

Except Bank Select Register (0xE).

Bank 32 Switch ID and Enable Register (0x00): SIDER

This register contains the chip ID and the chip enable bit.

TABLE 4-41: BANK 32 CHIP ID AND ENABLE REGISTER (0X00)

Bit	Default Value	R/W	Description
15 - 8	0x88	RO	**Family ID** Chip family ID
7 - 4	0x8	RO	**Chip ID** 0x8 is assigned to KSZ8862M
3 - 1	0x1	RO	Revision ID
0	0	R/W	**Start Switch** 1 = start the chip. 0 = switch is disabled.

Bank 32 Switch Global Control Register 1 (0x02): SGCR1

This register contains global control bits for the switch function.

TABLE 4-42: SWITCH GLOBAL CONTROL REGISTER 1 (0X02): SGCR1

Bit	Default	R/W	Description
15	0	RW	**Pass All Frames** 1 = Switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with Sniffer mode only.
14	0	RW	Reserved
13	1	RW	**IEEE 802.3x Transmit Direction Flow Control Enable** 1 = Enables transmit direction flow control feature. 0 = Disable transmit direction flow control feature. The switch will not generate any flow control packets.
12	1	RW	**IEEE 802.3x Receive Direction Flow Control Enable** 1 = Enables receive direction flow control feature. 0 = Disable receive direction flow control feature. The switch will not react to any received flow control packets.
11	0	RW	**Frame Length Field Check** 1 = Enable checking frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500).
10	1	RW	**Aging Enable** 1 = Enable aging function in the chip. 0 = Disable aging function in the chip.
9	0	RW	**Fast Age Enable** 1 = Turn on fast aging (800 µs).
8	0	RW	**Aggressive Back-Off Enable** 1 = Enable more aggressive back-off algorithm in half-duplex mode to enhance performance. This is not an IEEE standard.
7-4	—	RW	Reserved
3	0	RW	**Enable Flow Control when Exceeding Ingress Limit** 1 = Flow control frame will be sent to link partner when exceeding the ingress rate limit. 0 = Frame will be dropped when exceeding the ingress rate limit.
4	1	RW	**Receive 2K Byte Packets Enable** 1 = Enable packet length up to 2K bytes. While set, SGCR2 bits[2,1] will have no effect. 0 = Discard packet if packet length is greater than 2000 bytes.
3	0x0	RW	**Pass Flow Control Packet** 1 = Switch will not filter 802.1x “flow control” packets.
2-1	—	RW	Reserved
0	0	RW	**Link Change Age** 1 = Link change from “link” to “no link” will cause fast aging (<800 µs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 + 75 seconds). Note: If any port is unplugged, all addresses will be automatically aged out.

Bank 32 Switch Global Control Register 2 (0x04): SGCR2

This register contains global control bits for the switch function.

TABLE 4-43: SWITCH GLOBAL CONTROL REGISTER 2 (0X004 - 0X005): SGCR2

Bit	Default	R/W	Description
15	0	RW	**802.1Q VLAN Enable** 1 = 802.1Q VLAN mode is turned on. VLAN table must be set up before the operation. 0 = 802.1Q VLAN is disabled.
14	0	RW	**IGMP Snoop Enable On Switch Host Port** 1 = IGMP snoop is enabled. All the IGMP packets are forwarded to the switch host port. 0 = IGMP snoop is disabled.
13	0	RW	**IPv6 MLD Snooping Enable** 1 = Enable IPv6 MLD snooping.
12	0	RW	**IPv6 MLD Snooping Option** 1 = Enable IPv6 MLD snooping option.
11	0	RW	**Priority Scheme Select** 0 = always TX higher priority packets first. 1 = Weighted Fair Queueing enabled. When all four queues have packets waiting to transmit, the bandwidth allocation is q3:q2:q1:a0 = 8:4:2:1. If any queues are empty, the highest non-empty queue gets one more weighting. For example, if q2 is empty, q3:q1:q0 becomes (8+1): 0:2:1.
10 - 9	0x0	RW	Reserved
8	0	RW	**Sniff Mode Select** 1 = Performs RX and TX sniff (both the source port and destination port need to match). 0 = Performs RX or TX sniff (either the source port or destination port needs to match). This is the mode used to implement RX only sniff.
7	1	RW	**Unicast Port-VLAN Mismatch Discard** 1 = No packets can cross the VLAN boundary. 0 = Unicast packets (excluding unknown/multicast/broadcast) can cross the VLAN boundary.
6	1	RW	**Multicast Storm Protection Disable** 1 = “Broadcast Storm Protection” does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets are regulated. 0 = “Broadcast Storm Protection” includes DA = FF-FF-FF-FF-FF-FF and DA[40] = “1” packets.
5	1	RW	**Back Pressure Mode** 1 = Carrier sense-based back pressure is selected. 0 = Collision-based back pressure is selected.
4	1	RW	**Flow Control and Back Pressure Fair Mode** 1 = Fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This prevents the flow control port from being flow controlled for an extended period of time. 0 = In this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port is flow controlled. This may not be “fair” to the flow control port.
3	0	RW	**No Excessive Collision Drop** 1 = The switch does not drop packets when 16 or more collisions occur. 0 = The switch drops packets when 16 or more collisions occur.

TABLE 4-43: SWITCH GLOBAL CONTROL REGISTER 2 (0X004 - 0X005): SGCR2

Bit	Default	R/W	Description
2	0	RW	**Huge Packet Support** 1 = Accepts packet sizes up to 1916 bytes (inclusive). This bit setting overrides setting from bit 1 of the same register. 0 = The max packet size is determined by bit [1] of this register.
1	0	RW	**Legal Maximum Packet Size Check Enable** 1 = 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value are dropped. 0 = Accepts packet sizes up to 1536 bytes (inclusive).
0	0	RW	**Priority Buffer Reserve** 1 = Each port is pre-allocated 48 buffers, used exclusively for high priority (q3, q2, and q1) packets. Effective only when the multiple queue feature is turned on. 0 = Each port is pre-allocated 48 buffers used for all priority packets (q3, q2, q1, and q0).

Switch Global Control Register 3 (0x06): SGCR3

This register contains global control bits for the switch function.

TABLE 4-44: SWITCH GLOBAL CONTROL REGISTER 3 (0X06): SGCR3

Bit	Default	R/W	Description
15 - 8	0x63	RW	**Broadcast Storm Protection Rate Bit [7:0]** These bits, along with SGCR3[2:0], determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 670 ms for 10BT. The default is 1%.
7	0	RO	Reserved
6	0	RW	**Switch Host Port in Half-Duplex Mode** 1 = Enable host port interface half-duplex mode. 0 = Enable host port interface full-duplex mode.
5	1	RW	**Switch Host Port Flow Control Enable** 1 = Enable full-duplex flow control on Switch Host port. 0 = Disable full-duplex flow control on Switch Host port.
4	0	RW	Reserved
3	0	RW	**Null VID Replacement** 1 = Replaces NULL VID with port VID (12 bits). 0 = No replacement for NULL VID.
2 - 0	000	RW	**Broadcast Storm Protection Rate Bit [10:8]** These bits, along with SGCR3[15:8] determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 670 ms for 10BT. The default is 1%.

Rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx.) = 0x63.

Switch Global Control Register 4 (0x08): SGCR4

This register contains global control bits for the switch function.

TABLE 4-45: SWITCH GLOBAL CONTROL REGISTER 4 (0X08): SGCR4

Bit	Default	R/W	Description
15 - 0	0x2400	RW	Reserved

Bank 32 Switch Global Control Register 5 (0x0A): SGCR5

This register contains the global control for the chip function.

TABLE 4-46: BANK 32 CHIP GLOBAL CONTROL REGISTER (0X0A)

Bit	Default Value	R/W	Description
15	0	R/W	**LEDSEL1** See description in bit 9.
14 - 12	0	R/W	Reserved
11 - 10	0x2	R/W	Reserved
9	0	R/W	**LEDSEL0** These two bits, LEDSEL1 and LEDSEL0, are used to select LED mode. Port n LED indicators, (where n = 1 for port 1 and n =2 for port 2) defined as below:

	[LEDSEL1, LEDSEL0]	
	[0, 0]	**[0, 1]**
P1LED3	—	—
P1LED2	Link/Activity	100Link/Activity
P1LED1	Full-Duplex/Col	10Link/Activity
P1LED0	Speed	Full-Duplex

	[LEDSEL1, LEDSEL0]	
	[1, 0]	**[1, 1]**
P1LED3	Activity	—
P1LED2	Link	—
P1LED1	Full-Duplex/Col	—
P1LED0	Speed	—

8	0	RO	Reserved
7 - 0	0x35	RO	Reserved

Switch Global Control Register 6 (0x00): SGCR6

This register contains global control bits for the switch function.

TABLE 4-47: SWITCH GLOBAL CONTROL REGISTER 6 (0X00): SGCR6

Bit	Default	R/W	Description
15 - 14	0x3	R/W	**Tag_0x7** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x7.
13 - 12	0x3	R/W	**Tag_0x6** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x6.
11 - 10	0x2	R/W	**Tag_0x5** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x5.
9 - 8	0x2	R/W	**Tag_0x4** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x4.
7 - 6	0x1	R/W	**Tag_0x3** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x3.

TABLE 4-47: SWITCH GLOBAL CONTROL REGISTER 6 (0X00): SGCR6

Bit	Default	R/W	Description
5 - 4	0x1	R/W	**Tag_0x2** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x2.
3 - 2	0x0	R/W	**Tag_0x1** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x1.
1 - 0	0x0	R/W	**Tag_0x0** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x0.

Switch Global Control Register 7 (0x02): SGCR7

This register contains global control bits for the switch function.

TABLE 4-48: SWITCH GLOBAL CONTROL REGISTER 6 (0X00): SGCR6

Bit	Default	R/W	Description
15 - 8	0x00	R/W	Reserved
7	0	R/W	**Unknown Default Port Enable** Send packets with unknown destination address to specified ports in bits [2:0]. 1 = enable to send unknown DA packet.
6 - 3	—	R/W	Reserved
2 - 0	0x7	R/W	**Unknown Packet Default Port(s)** Specify which ports to send packets with unknown destination addresses. Feature is enabled by bit [7]. Bit 2 for the host port, bit 1 for port 2, and bit 0 for port 1.

Banks 34 – 38: Reserved

Except Bank Select Register (0xE)

Bank 39 MAC Address Register 1 (0x00): MACAR1

This register contains the MAC address for the switch function. This MAC address is used for sending PAUSE frame.

TABLE 4-49: MAC ADDRESS REGISTER 1 (0X00): MACAR1

Bit	Default	R/W	Description
15 - 0	0x0010	RW	**MACA[47:32]** Specifies MAC address 1. This value has to be same as MARH in Bank2.

Bank 39 MAC Address Register 2 (0x02): MACAR2

This register contains the MAC address for the switch function. This MAC address is used for sending PAUSE frame.

TABLE 4-50: MAC ADDRESS REGISTER 2 (0X02): MACAR2

Bit	Default	R/W	Description
15 - 0	0xA1FF	RW	**MACA[31:16]** Specifies MAC address 2. This value has to be same as MARL in Bank2.

Bank 39 MAC Address Register 3 (0x04): MACAR3

This register contains the MAC address for the switch function. This MAC address is used for sending PAUSE frame.

TABLE 4-51: MAC ADDRESS REGISTER 3 (0X014 - 0X015): MACAR3

Bit	Default	R/W	Description
15 - 0	0xFFFF	RW	**MACA[15:0]** Specifies MAC address 3. This value has to be same as MARL in Bank2.

4.3 Type-of-Service (TOS) Priority Control Registers

Bank 40 TOS Priority Control Register 1 (0x00): TOSR1

The Ipv4/Ipv6 ToS priority control registers implement a fully decoded,128-bit DSCP (Differentiated Services Code Point) register used to determine priority from the 6-bit ToS (Type of Service) field in the IP header. The most significant 6 bits of the ToS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bits in the DSCP register to determine the priority.

This register contains the TOS priority control bits for the switch function.

TABLE 4-52: TOS PRIORITY CONTROL REGISTER 1 (0X00): TOSR1

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[15:14]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x1c.
13−12	0	R/W	**DSCP[13:12]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x18.
11−10	0	R/W	**DSCP[11:10]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x14.
9−8	0	R/W	**DSCP[9:8]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x10.
7−6	0	R/W	**DSCP[7:6**] The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x0c.
5−4	0	R/W	**DSCP[5:4]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x08.
3−2	0	R/W	**DSCP[3:2]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x04.
1−0	0	R/W	**DSCP[1:0]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x00.

Bank 40 TOS Priority Control Register 2 (0x02): TOSR2

This register contains the TOS priority control bits for the switch function.

TABLE 4-53: TOS PRIORITY CONTROL REGISTER 2 (0X02): TOSR2

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[31:30]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x3c.
13−12	0	R/W	**DSCP[29:28]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x38.
11−10	0	R/W	**DSCP[27:26]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x34.
9−8	0	R/W	**DSCP[25:24]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x30.
7−6	0	R/W	**DSCP[23:22**] The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x2c.
5−4	0	R/W	**DSCP[21:20]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x28.
3−2	0	R/W	**DSCP[19:18]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x24.
1−0	0	R/W	**DSCP[17:16]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x20.

Bank 40 TOS Priority Control Register 3 (0x04): TOSR3

This register contains the TOS priority control bits for the switch function.

TABLE 4-54: TOS PRIORITY CONTROL REGISTER 3 (0X04): TOSR3

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[47:46]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x5c.
13−12	0	R/W	**DSCP[45:44]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x58.
11−10	0	R/W	**DSCP[43:42]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x54.
9−8	0	R/W	**DSCP[41:40]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x50.
7−6	0	R/W	**DSCP[39:38]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x4c.
5−4	0	R/W	**DSCP[37:36]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x48.
3−2	0	R/W	**DSCP[35:34]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x44.
1−0	0	R/W	**DSCP[33:32]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x40.

Bank 40 TOS Priority Control Register 4 (0x06): TOSR4

This register contains the TOS priority control bits for the switch function.

TABLE 4-55: TOS PRIORITY CONTROL REGISTER 4 (0X06): TOSR4

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[63:62]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x7c.
13−12	00	R/W	**DSCP[61:60]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x78.
11−10	00	R/W	**DSCP[59:58]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x74.
9−8	00	R/W	**DSCP[57:56]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x70.
7−6	00	R/W	**DSCP[55:54]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x6c.
5−4	00	R/W	**DSCP[53:52]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x68.
3−2	00	R/W	**DSCP[51:50]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x64.
1−0	00	R/W	**DSCP[49:48]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x60.

Bank 40 TOS Priority Control Register 5 (0x08): TOSR5

This register contains the TOS priority control bits for the switch function.

TABLE 4-56: TOS PRIORITY CONTROL REGISTER 5 (0X05): TOSR5

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[79:78]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x9c.
13−12	00	R/W	**DSCP[77:76]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x98.
11−10	00	R/W	**DSCP[75:74]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x94.
9−8	00	R/W	**DSCP[73:72]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x90.
7−6	00	R/W	**DSCP[71:70]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x8c.
5−4	00	R/W	**DSCP[69:68]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x88.
3−2	00	R/W	**DSCP[67:66]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x84.
1−0	00	R/W	**DSCP[65:64]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x80.

Bank 40 TOS Priority Control Register 6 (0x0A): TOSR6

This register contains the TOS priority control bits for the switch function.

TABLE 4-57: TOS PRIORITY CONTROL REGISTER 6 (0X0A): TOSR6

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[95:94]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value is 0xbc.
13−12	00	R/W	**DSCP[93:92]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb8.
11−10	00	R/W	**DSCP[91:90]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb4.
9−8	00	R/W	**DSCP[89:88]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb0.
7−6	00	R/W	**DSCP[87:86]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xac.
5−4	00	R/W	**DSCP[85:84]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa8.
3−2	00	R/W	**DSCP[83:82]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa4.
1−0	00	R/W	**DSCP[81:80]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa0.

Bank 41 TOS Priority Control Register 7 (0x00): TOSR7

This register contains the TOS priority control bits for the switch function.

TABLE 4-58: TOS PRIORITY CONTROL REGISTER 7 (0X00): TOSR7

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[111:110]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xdc.
13−12	00	R/W	**DSCP[109:108]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd8.
11−10	00	R/W	**DSCP[107:106]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd4.
9−8	00	R/W	**DSCP[105:104]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd0.
7−6	00	R/W	**DSCP[103:102]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xcc.
5−4	00	R/W	**DSCP[101:100]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc8.
3−2	00	R/W	**DSCP[99:98]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc4.
1−0	00	R/W	**DSCP[97:96]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc0.

Bank 41 TOS Priority Control Register 8 (0x02): TOSR8

This register contains the TOS priority control bits for the switch function.

TABLE 4-59: TOS PRIORITY CONTROL REGISTER 7 (0X02): TOSR8

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[127:126]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xfc.
13−12	00	R/W	**DSCP[125:124]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf8.
11−10	00	R/W	**DSCP[123:122]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf4.
9−8	00	R/W	**DSCP[121:120]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf0.
7−6	00	R/W	**DSCP[119:118]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xec.
5−4	00	R/W	**DSCP[117:116]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe8.
3−2	00	R/W	**DSCP[115:114]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe4.
1−0	00	R/W	**DSCP[113:112]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe0.

Bank 42 Indirect Access Control Register (0x00): IACR

This register contains the indirect control for the switch function.

TABLE 4-60: BANK 42 INDIRECT ACCESS CONTROL REGISTER (0X00)

Bit	Default Value	R/W	Description
15 - 13	0x0	RO	Reserved
12	0	R/W	**Read High. Write Low** 1 = Read cycle. 0 = Write cycle.
11 - 10	0x0	R/W	**Table Select** 00 = Static MAC address table selected. 01 = VLAN table selected. 10 = Dynamic address table selected. 11 = MIB counter selected.
9 - 0	0x000	R/W	**Indirect Address** Bit 9-0 of indirect address.

Note: Write IACR triggers a command. Read or write access is determined by Register bit 12.

Bank 42 Indirect Access Data Register 1 (0x02): IADR1

This register contains the indirect data for the chip function.

TABLE 4-61: BANK 42 INDIRECT ACCESS DATA REGISTER 1 (0X02)

Bit	Default Value	R/W	Description
15 - 8	0x00	RO	Reserved
7	0	RO	**CPU Read Status** Only for dynamic and statistics counter reads. 1 = Read is still in progress. 0 = Read has completed.
6 - 3	0x0	RO	Reserved
2 - 0	0x0	RO	**Indirect Data [66:64]** Bits [66:64] of indirect data.

Bank 42 Indirect Access Data Register 2 (0x04): IADR2

This register contains the indirect data for the switch function.

TABLE 4-62: BANK 42 INDIRECT ACCESS DATA REGISTER 2 (0X04)

Bit	Default Value	R/W	Description
15 - 0	0x0000	RW	**Indirect Data** Bit 47-32 of indirect data.

Bank 42 Indirect Access Data Register 3 (0x06): IADR3

This register contains the indirect data for the chip function.

TABLE 4-63: BANK 42 INDIRECT ACCESS DATA REGISTER 3 (0X06)

Bit	Default Value	R/W	Description
15 - 0	0x0000	RW	**Indirect Data** Bit 63-48 of indirect data.

Bank 42 Indirect Access Data Register 4 (0x08): IADR4

This register contains the indirect data for the chip function.

TABLE 4-64: BANK 42 INDIRECT ACCESS DATA REGISTER 4 (0X08)

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	**Indirect Data** Bit 15-0 of indirect data.

Bank 42 Indirect Access Data Register 5 (0x0A): IADR5

This register contains the indirect data for the chip function.

TABLE 4-65: BANK 42 INDIRECT ACCESS DATA REGISTER 5 (0X0A)

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	**Indirect Data** Bit 31-16 of indirect data.

Bank 43: Reserved

Except Bank Select Register (0xE)

Bank 44 Digital Testing Status Register (0x00): DTSR

This register contains the user defined register for the switch function.

TABLE 4-66: BANK 44 DIGITAL TESTING STATUS REGISTER (0X00)

Bit	Default Value	R/W	Description
15 - 3	0x0000	RO	Reserved
2 - 0	0x0	RO	Reserved

Bank 44 Analog Testing Status Register (0x02): ATSR

This register contains the user defined register for the switch function.

TABLE 4-67: BANK 44 ANALOG TESTING STATUS REGISTER (0X02)

Bit	Default Value	R/W	Description
15 - 8	0x00	RO	Reserved
7 - 0	0x00	RO	Reserved

Bank 44 Digital Testing Control Register (0x04): DTCR

This register contains the user defined register for the switch function.

TABLE 4-68: BANK 44 DIGITAL TESTING CONTROL REGISTER (0X04)

Bit	Default Value	R/W	Description
15 - 8	0x00	RO	Reserved
7 - 0	0x00	RO	Reserved

Bank 44 Analog Testing Control Register (0x06): ATCR0

This register contains the user defined register for the switch function.

TABLE 4-69: BANK 44 ANALOG TESTING STATUS REGISTER (0X06)

Bit	Default Value	R/W	Description
15 - 8	0x00	RO	Reserved
7 - 6	0x00	RW	**LED Driver Current Set** 00 = 60 mA 01 = 80 mA 10 = 97 mA 11 = 40 mA
5 - 0	0x00	RO	Reserved

Bank 44 Analog Testing Control Register 1 (0x08): ATCR1

This register contains the user defined register for the switch function.

TABLE 4-70: BANK 44 ANALOG TESTING CONTROL REGISTER 1 (0X08)

Bit	Default Value	R/W	Description
15 - 0	0x00	RO	Reserved

Bank 44 Analog Testing Control Register 2 (0x0A): ATCR2

This register contains the user defined register for the switch function.

TABLE 4-71: BANK 44 ANALOG TESTING CONTROL REGISTER 1 (0X0A)

Bit	Default Value	R/W	Description
15 - 0	0x0000	RO	Reserved

Bank 45 PHY 1 MII-Register Basic Control Register (0x00): P1MBCR

This register contains Media Independent Interface (MII) register for port 1 as defined in the IEEE 802.3 specification.

TABLE 4-72: BANK 45 PHY 1 MII-REGISTER BASIC CONTROL REGISTER (0X00)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	**Soft Reset** Not supported.	—
14	0	R/W	**Far-End Loopback** 1 = Perform loopback as follows: Start: RXP2/RXM2 (Port 2) Loop back: PMD/PMA of Port 1's PHY End: TXP2/TXM2 (Port 2) 0 = Normal operation.	Bank 49 0x02 bit 8
13	0	R/W	**Force 100** 1 = Force 100 Mbps if AN is disabled (bit 12) 0 = Force 10 Mbps if AN is disabled (bit 12)	Bank 49 0x2 bit6
12	1	R/W	**AN Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	Bank 49 0x2 bit7
11	0	R/W	**Power-Down** 1 = Power-down. 0 = Normal operation.	Bank 49 0x2 bit11
10	0	RO	**Isolate** Not supported.	—
9	0	R/W	**Restart AN** Note 1 1 = Restart auto-negotiation. 0 = Normal operation.	Bank 49 0x2 bit13
8	0	R/W	**Force Full Duplex** 1 = Force full-duplex 0 = Force half-duplex. If AN is disabled (bit 12) or AN is enabled but failed.	Bank 49 0x2 bit5
7	0	RO	**Collision test** Not supported.	—
6	0	RO	Reserved	—
5	1	R/W	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Microchip Auto MDI-X mode.	Bank 49 0x4 bit15
4	0	R/W	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.	Bank 49 0x2 bit9
3	0	R/W	**Disable MDI-X** 1 = Disable auto MDI-X. 0 = Normal operation.	Bank 49 0x2 bit10
2	0	R/W	**Disable Far-End-Fault** 1 = disable far-end-fault detection. 0 = normal operation.	Bank 49 0x2 bit12

TABLE 4-72: BANK 45 PHY 1 MII-REGISTER BASIC CONTROL REGISTER (0X00) (CONTINUED)

Bit	Default Value	R/W	Description	Bit Same As
1	0	R/W	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.	Bank 49 0x2 bit14
0	0	R/W	**Disable LED** 1 = Disable LED. 0 = Normal operation.	Bank 49 0x2 bit15

Note 1: Auto Negotiation is not supporting on port 1.

Bank 45 PHY 1 MII-Register Basic Status Register (0x02): P1MBSR

This register contains the MII register status for the chip function.

TABLE 4-73: BANK 45 PHY 1 MII-REGISTER BASIC STATUS REGISTER (0X02)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	**T4 Capable** 1 = 100BASE-T4 capable. 0 = not 100BASE-T4 capable.	—
14	1	RO	**100 Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex.capable.	—
13	1	RO	**100 Half Capable** 1= 100BASE-TX half-duplex capable. 0= Not 100BASE-TX half-duplex capable.	—
12	1	RO	**10 Full Capable** 1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	—
11	1	RO	**10 Half Capable** 1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	—
10 - 7	0	RO	Reserved	—
6	0	RO	**Preamble suppressed** Not supported.	—
5	0	RO	**AN Complete** 1 = Auto-negotiation complete. 0 = Auto-negotiation not completed.	Bank 49 0x4 bit6
4	0	RO	**Far-End-Fault** 1 = Far-end-fault detected. 0 = No far-end-fault detected.	Bank 49 0x4 bit8
3	1	RO	**AN Capable** 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	—
2	0	RO	**Link Status** 1 = Link is up. 0 = Link is down.	Bank 49 0x4 bit5
1	0	RO	**Jabber test** Not supported.	—
0	0	RO	**Extended Capable** 1 = Extended register capable. 0 = Not extended register capable.	—

Bank 45 PHY 1 PHYID Low Register (0x04): PHY1ILR

This register contains the PHY ID (low) for the switch port 1 function.

TABLE 4-74: BANK 45 PHY 1 PHYID LOW REGISTER (0X04)

Bit	Default Value	R/W	Description
15 - 0	0x1430	RO	**PHYID Low** Low order PHYID bits.

Bank 45 PHY 1 PHYID High Register (0x06): PHY1IHR

This register contains the PHY ID (high) for the switch port 1 function.

TABLE 4-75: BANK 45 PHY 1 PHYID HIGH REGISTER (0X06)

Bit	Default Value	R/W	Description
15 - 0	0x0022	RO	**PHYID High** High order PHYID bits.

Bank 45 PHY 1 Auto-Negotiation Advertisement Register (0x08): P1ANAR

This register contains the auto-negotiation advertisement for the switch port function.

TABLE 4-76: BANK 45 PHY 1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0X08)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	Reserved	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0	RO	Reserved	—
10	1	R/W	**Pause (flow control capability)** 1 = Advertise pause capability. 0 = Do not advertise pause capability.	Bank 49 0x2 bit4
9	0	R/W	Reserved	—
8	1	R/W	**Adv 100 Full** 1 = Advertise 100 full-duplex capability. 0 = Do not advertise 100 full-duplex capability	Bank 49 0x2 bit3
7	1	R/W	**Adv 100 Half** 1= Advertise 100 half-duplex capability. 0 = Do not advertise 100 half-duplex capability.	Bank 49 0x2 bit2
6	1	R/W	**Adv 10 Full** 1 = Advertise 10 full-duplex capability. 0 = Do not advertise 10 full-duplex capability.	Bank 49 0x2 bit1
5	1	R/W	**Adv 10 Half** 1 = Advertise 10 half-duplex capability. 0 = Do not advertise 10 half-duplex capability.	Bank 49 0x2 bit0
4 - 0	0x01	RO	**Selector Field** 802.3	—

Bank 45 PHY 1 Auto-Negotiation Link Partner Ability Register (0x0A): P1ANLPR

This register contains the auto-negotiation link partner ability for switch port 1 function.

TABLE 4-77: BANK 45 PHY 1 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (0X0A)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**LP ACK** Not supported.	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0	RO	Reserved	—
10	0	RO	**Pause** Link partner pause capability.	Bank49 0x4 bit4
9	0	RO	Reserved	—
8	0	RO	**Adv 100 Full** Link partner 100 full capability.	Bank49 0x4 bit3
7	0	RO	**Adv 100 Half** **Link partner 100 half capability.**	Bank49 0x4 bit2
6	0	RO	**Adv 10 Full** **Link partner 10 full capability.**	Bank49 0x4 bit1
5	0	RO	**Adv 10 Half** Link partner 10 half capability.	Bank49 0x4 bit0
4 - 0	0x01	RO	Reserved	—

Bank 46 PHY 2 MII-Register Basic Control Register (0x00): P2MBCR

This register contains Media Independent Interface (MII) register for port 1 as defined in the IEEE 802.3 specification.

TABLE 4-78: BANK 45 PHY 1 MII-REGISTER BASIC CONTROL REGISTER (0X00)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	Soft reset Not supported.	—
14	0	R/W	**Far-End Loopback** 1 = Perform loopback as follows: Start: RXP2/RXM2 (Port 1) Loop back: PMD/PMA of Port 2's PHY End: TXP1/TXM1 (Port 1) 0 = Normal operation.	Bank 51 0x02 bit 8
13	0	R/W	**Force 100** 1 = Force 100 Mbps. 0 = Force 10 Mbps.	Bank 51 0x2 bit6
12	1	R/W	**AN Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	Bank 51 0x2 bit7
11	0	R/W	**Power-Down** 1 = Power-down. 0 = Normal operation.	Bank 51 0x2 bit11
10	0	RO	**Isolate** Not supported.	—
9	0	R/W	**Restart AN** 1 = Restart auto-negotiation. 0 = Normal operation.	Bank 51 0x2 bit13

TABLE 4-78: BANK 45 PHY 1 MII-REGISTER BASIC CONTROL REGISTER (0X00) (CONTINUED)

Bit	Default Value	R/W	Description	Bit Same As
8	0	R/W	**Force Full Duplex** 1 = Force full-duplex 0 = Force half-duplex.	Bank 51 0x2 bit5
7	0	RO	**Collision test** Not supported.	—
6	0	RO	Reserved	—
5	1	R/W	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Microchip Auto MDI-X mode.	Bank 51 0x4 bit15
4	0	R/W	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.	Bank 51 0x2 bit9
3	0	R/W	**Disable MDI-X** 1 = Disable auto MDI-X. 0 = Normal operation.	Bank 51 0x2 bit10
2	0	R/W	**Disable Far-End-Fault** 1 = Disable far-end-fault detection. 0 = Normal operation.	Bank 51 0x2 bit12
1	0	R/W	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.	Bank 51 0x2 bit14
0	0	R/W	**Disable LED** 1 = Disable LED. 0 = Normal operation.	Bank 51 0x2 bit15

Bank 46 PHY 2 MII-Register Basic Status Register (0x02): P2MBSR

This register contains the MII register status for the switch port 2 function.

TABLE 4-79: BANK 46 PHY 2 MII-REGISTER BASIC STATUS REGISTER (0X02)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	**T4 Capable** 0 = not 100BASE-T4 capable.	—
14	1	RO	**100 Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex.capable.	—
13	1	RO	**100 Half Capable** 1= 100BASE-TX half-duplex capable. 0= Not 100BASE-TX half-duplex capable.	—
12	1	RO	**10 Full Capable** 1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	—
11	1	RO	**10 Half Capable** 1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	—
10 - 7	0	RO	Reserved	—
6	0	RO	**Preamble suppressed** Not supported.	—
5	0	RO	**AN Complete** 1 = Auto-negotiation complete. 0 = Auto-negotiation not completed.	Bank 51 0x4 bit6

TABLE 4-79: BANK 46 PHY 2 MII-REGISTER BASIC STATUS REGISTER (0X02) (CONTINUED)

Bit	Default Value	R/W	Description	Bit Same As
4	0	RO	Reserved	Bank 51 0x4 bit8
3	1	RO	**AN Capable** 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	—
2	0	RO	**Link Status** 1 = Link is up. 0 = Link is down.	Bank 51 0x4 bit5
1	0	RO	**Jabber test** Not supported.	—
0	0	RO	**Extended Capable** 1 = Extended register capable. 0 = Not extended register capable.	—

Bank 46 PHY 2 PHYID Low Register (0x04): PHY2ILR

This register contains the PHY ID (low) for the switch port 2 function.

TABLE 4-80: BANK 46 PHY 2 PHYID LOW REGISTER (0X04)

Bit	Default Value	R/W	Description
15 - 0	0x1430	RO	**PHYID Low** Low order PHYID bits.

Bank 46 PHY 2 PHYID High Register (0x06): PHY2IHR

This register contains the PHY ID (high) for the switch port 2 function.

TABLE 4-81: BANK 46 PHY 2 PHYID HIGH REGISTER (0X06)

Bit	Default Value	R/W	Description
15 - 0	0x0022	RO	**PHYID High** High order PHYID bits.

Bank 46 PHY 2 Auto-Negotiation Advertisement Register (0x08): P2ANAR

This register contains the auto-negotiation advertisement for the switch port 2 function.

TABLE 4-82: BANK 46 PHY 2 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0X08)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	Reserved	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0	RO	Reserved	—
10	1	R/W	**Pause (flow control capability)** 1 = Advertise pause capability. 0 = Do not advertise pause capability.	Bank 51 0x2 bit4
9	0	RO	Reserved	—
8	1	R/W	**Adv 100 Full** 1 = Advertise 100 full-duplex capability. 0 = Do not advertise 100 full-duplex capability	Bank 51 0x2 bit3

TABLE 4-82: BANK 46 PHY 2 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0X08)

Bit	Default Value	R/W	Description	Bit Same As
7	1	R/W	**Adv 100 Half** 1= Advertise 100 half-duplex capability. 0 = Do not advertise 100 half-duplex capability.	Bank 51 0x2 bit2
6	1	R/W	**Adv 10 Full** 1 = Advertise 10 full-duplex capability. 0 = Do not advertise 10 full-duplex capability.	Bank 51 0x2 bit1
5	1	R/W	**Adv 10 Half** 1 = Advertise 10 half-duplex capability. 0 = Do not advertise 10 half-duplex capability.	Bank 51 0x2 bit0
4 - 0	0x01	RO	**Selector Field** 802.3	—

Bank 46 PHY 2 Auto-Negotiation Link Partner Ability Register (0x0A): P2ANLPR

This register contains the auto-negotiation link partner ability for switch port 2 function.

TABLE 4-83: BANK 46 PHY 2 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (0X0A)

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**LP ACK** Not supported.	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0	RO	Reserved	—
10	0	RO	**Pause** Link partner pause capability.	Bank 51 0x4 bit4
9	0	RO	Reserved	—
8	0	RO	**Adv 100 Full** Link partner 100 full capability.	Bank 51 0x4 bit3
7	0	RO	**Adv 100 Half** Link partner 100 half capability.	Bank 51 0x4 bit2
6	0	RO	**Adv 10 Full** Link partner 10 full capability.	Bank 51 0x4 bit1
5	0	RO	**Adv 10 Half** Link partner 10 half capability.	Bank 51 0x4 bit0
4 - 0	0x01	RO	Reserved	—

Bank 47 PHY1 Special Control/Status Register (0x02): P1PHYCTRL

This register contains the control and status information of PHY1.

TABLE 4-84: BANK 47 PHY1 SPECIAL CONTROL/STATUS REGISTER (0X02): P1PHYCTRL

Bit	Default Value	R/W	Description	Bit Same As
15 - 6	0x000	RO	Reserved	—
5	0	RO	**Polarity Reverse (polrvs)** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bank 49 0x04 bit 13
4	0	RO	**MDIX Status (mdix_st)** 1 = MDI 0 = MDIX	Bank 49 0x04 bit 7
3	0	R/W	**Force Link (force_lnk)** 1 = Force link pass. 0 = Normal operation.	Bank 49 0x00 bit 11
2	1	R/W	**Power Saving (pwrsave)** 1 = Disable power saving. 0 = Enable power saving.	Bank 49 0x00 bit 10
1	0	R/W	**Remote (Near-end) Loopback (rlb)** 1 = Perform remote loopback at PHY (RXP1/RXM1 -> TXP1/TXM1, (see Figure 7-2) 0 = Normal operation	Bank 49 0x00 bit 9
0	0	RO	Reserved	—

Bank 47 PHY2 LinkMD Control/Status (0x04): P2VCT

This register contains the LinkMD control and status information of PHY 2.

TABLE 4-85: BANK 47 PHY2 LINKMD CONTROL/STATUS (0X04): P2VCT

Bit	Default Value	R/W	Description	Bit Same As
15	0	R/W (Self-Clear)	**Vct_enable** 1 = Cable diagnostic test is enabled. It is self-cleared after the VCT test is done. 0 = Indicates that the cable diagnostic test is completed and the status information is valid for read.	Bank 51 0x00 bit 12
14 - 13	0x0	RO	**Vct_result** [00] = Normal condition. [01] = Open condition detected in the cable. [10] = Short condition detected in the cable. [11] = Cable diagnostic test failed.	Bank 51 0x00 bit 14 - 13
12	—	RO	**Vct 10M Short** 1 = Less than 10m short.	Bank 51 0x00 bit 15
11 - 9	0x0	RO	Reserved	—
8 - 0	0x000	RO	**Vct_fault_count** Distance to the fault. The distance is approximately 0.4m*vct_fault_count.	Bank 51 0x00 bit 8 - 0

Bank 47 PHY2 Special Control/Status Register (0x06): P2PHYCTRL

This register contains the control and status information of PHY2.

TABLE 4-86: BANK 47 PHY1 SPECIAL CONTROL/STATUS REGISTER (0X02): P1PHYCTRL

Bit	Default Value	R/W	Description	Bit Same As
15 - 6	0x000	RO	Reserved	—
5	0	RO	**Polarity Reverse (polrvs)** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bank 51 0x04 bit 13
4	0	RO	**MDIX Status (mdix_st)** 1 = MDI 0 = MDIX	Bank 51 0x04 bit 7
3	0	R/W	**Force Link (force_lnk)** 1 = Force link pass. 0 = Normal operation.	Bank 51 0x00 bit 11
2	1	R/W	**Power Saving (pwrsave)** 1 = Disable power saving. 0 = Enable power saving.	Bank 51 0x00 bit 10
1	0	R/W	**Remote (Near-end) Loopback (rlb)** 1 = Perform remote loopback at Port 2's (RXP2/RXM2 -> TXP2/TXM2, (see Figure 7-2) 0 = Normal operation	Bank 51 0x00 bit 9
0	0	RO	Reserved	—

Bank 48 Port 1 Control Register 1 (0x00): P1CR1

This register contains control bits for the switch Port 1 function.

TABLE 4-87: PORT 1 CONTROL REGISTER 1 (0X00): P1CR1

Bit	Default	R/W	Description
15 - 8	0x00	RO	Reserved
7	0	R/W	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress packets on Port 1. 0 = Disable broadcast storm protection.
6	0	R/W	**Diffserv Priority Classification Enable** 1 = Enable DiffServ priority classification for ingress packets on Port 1. 0 = Disable DiffServ function.
5	0	R/W	**802.1p Priority Classification Enable** 1 = Enable 802.1p priority classification for ingress packets on Port 1. 0 = Disable 802.1p.
4 - 3	0x0	R/W	**Port-Based Priority Classification** 00 = Ingress packets on Port 1 are classified as priority 0 queue if "DiffServ" or "802.1p" classification is not enabled or fails to classify. 01 = Ingress packets on Port 1 are classified as priority 1 queue if "DiffServ" or "802.1p" classification is not enabled or fails to classify. 10 = Ingress packets on Port 1 are classified as priority 2 queue if "DiffServ" or "802.1p" classification is not enabled or fails to classify. 11 = Ingress packets on Port 1 are classified as priority 3 queue if "Diffserv" or "802.1p" classification is not enabled or fails to classify. Note: "DiffServ", "802.1p" and port priority can be enabled at the same time. The OR'ed result of 802.1p and DSCP overwrites the port priority.

TABLE 4-87: PORT 1 CONTROL REGISTER 1 (0X00): P1CR1 (CONTINUED)

Bit	Default	R/W	Description
2	0	RW	**Tag Insertion** 1 = When packets are output on Port 1, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port's "port VID". 0 = Disable tag insertion.
1	0	RW	**Tag Removal** 1 = When packets are output on Port 1, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	**TX Multiple Queues Select Enable** 1 = The Port 1 output queue is split into four priority queues (q0, q1, q2 and q3). 0 = Single output queue on Port 1. There is no priority differentiation even though packets are classified into high or low priority.

Bank 48 Port 1 Control Register 2 (0x02): P1CR2

This register contains control bits for the switch function.

TABLE 4-88: PORT 1 CONTROL REGISTER 2 (0X02): P1CR2

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	**Force Flow Control** 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	**Back Pressure Enable** 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.

TABLE 4-88: PORT 1 CONTROL REGISTER 2 (0X02): P1CR2 (CONTINUED)

Bit	Default	R/W	Description
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No receive monitoring.
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No transmit monitoring.
4	0	RO	Reserved
3	0	RW	**User Priority Ceiling** 1 = If the packet’s “priority field” is greater than the “user priority field” in the port VID control register bit[15:13], replace the packet’s “priority field” with the “user priority field” in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet’s “priority field.”
2 - 0	0X7	RW	**Port VLAN Membership** Define the port’s Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A ‘1’ includes a port in the membership; a ‘0’ excludes a port from the membership.

Bank 48 Port 1 VID Control Register (0x04): P1VIDCR

This register contains the global per port control for the switch function.

TABLE 4-89: PORT 1 VID CONTROL REGISTER (0X04): P1VIDCR

Bit	Default	R/W	Description
15 - 13	0x00	RW	**Default Tag[15:13]** Port’s default tag, containing “User Priority Field” bits.
12	0	RW	**Default Tag[12]** Port’s default tag, containing the CFI bit.
11 - 0	0x001	RW	**Default Tag[11:0]** Port’s default tag, containing the VID[11:0].

Note: This VID Control register serves two purposes:

Associated with the ingress untagged packets, and used for egress tagging.

Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.

Bank 48 Port 1 Control Register 3 (0x06): P1CR3

This register contains control bits for the switch Port 1 function.

TABLE 4-90: PORT 1 CONTROL REGISTER 3 (0X06): P1CR3

Bit	Default	R/W	Description
15 - 5	0x000	RO	Reserved
4	0	RO	Reserved
3 - 2	0x0	RW	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	0	RW	**Count Inter Frame Gap** Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in ingress and egress rate calculations. 0 = IFG bytes are not counted.
0	0	RW	**Count Preamble** Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. 0 = Preamble bytes are not counted.

Bank 48 Port 1 Ingress Rate Control Register (0x08): P1IRCR

TABLE 4-91: PORT 1 INGRESS RATE CONTROL REGISTER (0X08): P1IRCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Ingress Pri3 Rate** Priority 3 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10 BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
11 - 8	0x0	RW	**Ingress Pri2 Rate** Priority 2 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited).

TABLE 4-91: PORT 1 INGRESS RATE CONTROL REGISTER (0X08): P1IRCR

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Ingress Pri1 Rate** Priority 1 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10 BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
3 - 0	0x0	RW	**Ingress Pri0 Rate** Priority 0 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10 BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).

Bank 48 Port 1 Egress Rate Control Register (0x0A): P1ERCR

TABLE 4-92: PORT 1 EGRESS RATE CONTROL REGISTER (0X0A): P1ERCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Egress Pri3 Rate** Egress data rate limit for priority 3 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
11 - 8	0x0	RW	**Egress Pri2 Rate** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

TABLE 4-92: PORT 1 EGRESS RATE CONTROL REGISTER (0X0A): P1ERCR

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Egress Pri1 Rate** Egress data rate limit for priority 1 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
3 - 0	0x0	RW	**Egress Pri0 Rate** Egress data rate limit for priority 0 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

Bank 49 Port 1 PHY Special Control/Status, LinkMD (0x00): P1SCSLMD

TABLE 4-93: PORT 1 PHY SPECIAL CONTROL/STATUS, LINKMD (0X00): P1SCSLMD

Bit	Default	R/W	Description	Bit Same As
15	0	RO	Reserved	—
14 - 13	0x0	RO	Reserved	—
12	0	RO	Reserved	—
11	0	RW	**Force_Link** Force link. 1 = Force link pass. 0 = Normal operation.	Bank 47 0x02 bit 3
10	1	RW	**pwrsave** Power-saving. 1 = disable power saving. 0 = enable power saving.	Bank 47 0x02 bit 2
9	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at Port 1's PHY (RXP1/RXM1 –> TXP1/TXM1, (see Figure 7-2) 0 = Normal operation	Bank 47 0x02 bit 1
8 - 0	0x000	RO	Reserved	—

Bank 49 Port 1 Control Register 4 (0x02): P1CR4

This register contains the global per port control for the switch function.

TABLE 4-94: PORT 1 CONTROL REGISTER 4 (0X02): P1CR4

Bit	Default	R/W	Description	Bit Same As:
15	0	RW	**LED Off** 1 = Turn off all of the port 1 LEDs (P1LED3, P1LED2, P1LED1, P1LED0). These pins are driven high if this bit is set to one. 0 = normal operation.	Bank 45 0x00 bit 0
14	0	RW	**Txids** 1 = disable the port's transmitter. 0 = normal operation.	Bank 45 0x00 bit 1
13	0	RW	Restart Auto-Negotiation (Note 1) 1 = Restart auto-negotiation. 0 = Normal operation..	Bank 45 0x00 bit 9
12	0	RW	**Disable Far-End-Fault** 1 = disable far-end-fault detection and pattern transmission. 0 = enable far end fault detection and pattern transmission.	Bank 45 0x00 bit 2
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation. No change to registers setting.	Bank 45 0x00 bit 11
10	0	RW	**Disable Auto MDI/MDI-X** 1 = Disable Auto-MDI/MDI-X function. 0 = Enable Auto-MDI/MDI-X function.	Bank 45 0x00 bit 3
9	0	RW	**Force MDI-X** 1 = If Auto-MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = Do not force PHY into MDI-X mode.	Bank 45 0x00 bit 4

TABLE 4-94: PORT 1 CONTROL REGISTER 4 (0X02): P1CR4

Bit	Default	R/W	Description	Bit Same As:
8	0	RW	**Far-End Loopback** 1 = Perform loopback, as indicated: Start: RXP2/RXM2 (Port 2). Loopback: PMD/PMA of Port 1's PHY. End: TXP2/TXM2 (Port 2). 0 = Normal operation.	Bank 45 0x00 bit 14
7	1	RW	**Auto-Negotiation Enable (Note 1)** 1 = Auto-negotiation is enabled. 0 = Disable auto-negotiation, speed, and duplex are decided by bits [6:5] of the same register.	Bank 45 0x00 bit 12
6	1	RW	**Force Speed** 1 = Force 100BT if auto-negotiation is disabled (bit [7]). 0 = Force 10BT if auto-negotiation is disabled (bit [7]).	Bank 45 0x00 bit 13
5	1	RW	**Force Duplex** 1 = Force full-duplex if auto-negotiation is disabled. 0 = Force half-duplex if auto-negotiation is disabled. This bit also determines duplex if auto-negotiation is enabled but fails. When AN is enabled, this bit should be set to zero.	Bank 45 0x00 bit 8
4	1	RW	**Advertised Flow Control Capability** 1 = Advertise flow control (pause) capability. 0 = Suppress flow control (pause) capability from transmission to link partner.	Bank 45 0x08 bit 10
3	1	RW	**Advertised 100BT Full-Duplex Capability** 1 = Advertise 100BT full-duplex capability. 0 = Suppress 100BT full-duplex capability from transmission to link partner.	Bank 45 0x08 bit 8
2	1	RW	**Advertised 100BT Half-Duplex Capability** 1 = Advertise 100BT half-duplex capability. 0 = Suppress 100BT half-duplex capability from transmission to link partner.	Bank 45 0x08 bit 7
1	1	RW	**Advertised 10BT Full-Duplex Capability** 1 = Advertise 10BT full-duplex capability. 0 = Suppress 10BT full-duplex capability from transmission to link partner.	Bank 45 0x08 bit 6
0	1	RW	**Advertised 10BT Half-Duplex Capability** 1 = Advertise 10BT half-duplex capability. 0 = Suppress 10BT half-duplex capability from transmission to link partner.	Bank 45 0x08 bit 5

Bank 49 Port 1 Status Register (0x04): P1SR

This register contains the global per port status for the switch function.

TABLE 4-95: PORT 1 STATUS REGISTER (0X04): P1SR

Bit	Default	R/W	Description	Bit Same As:
15	1	RW	**HP_MDI-X** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.	Bank 45 0x00 bit 5
14	0	RO	Reserved	—
13	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bank 47 0x02 bit 5

TABLE 4-95: PORT 1 STATUS REGISTER (0X04): P1SR (CONTINUED)

Bit	Default	R/W	Description	Bit Same As:
12	0	RO	**Receive Flow Control Enable** 1 = receive flow control feature is active. 0 = receive flow control feature is inactive.	—
11	0	RO	**Transmit Flow Control Enable** 1 = transmit flow control feature is active. 0 = transmit flow control feature is inactive.	—
10	0	RO	**Operation Speed** 1 = Link speed is 100 Mbps. 0 = Link speed is 10 Mbps.	—
9	0	RO	**Operation Duplex** 1 = Link duplex is full. 0 = Link duplex is half.	—
8	0	RO	**Far-End-Fault** 1 = far-end-fault status detected. 0 = no Far-end-fault status detected.	Bank 45 0x02 bit 4
7	0	RO	**MDI-X Status** 0 = MDI. 1 = MDI-X	Bank 47 0x02 bit 4
6	0	RO	Reserved	Bank 45 0x02 bit 5
5	0	RO	**Link Good** 1 = Link good. 0 = Link not good.	Bank 45 0x02 bit 2
4	0	RO	**Partner Flow Control Capability** 1 = Link partner flow control (pause) capable. 0 = Link partner not flow control (pause) capable.	Bank 45 0x0A bit 10
3	0	RO	**Partner 100BT Full-Duplex Capability** 1 = Link partner 100BT full-duplex capable. 0 = Link partner not 100BT full-duplex capable.	Bank 45 0x0A bit 8
2	0	RO	**Partner 100BT Half-Duplex Capability** 1 = Link partner 100BT half-duplex capable. 0 = Link partner not 100BT half-duplex capable.	Bank 45 0x0A bit 7
1	0	RO	**Partner 10BT Full-Duplex Capability** 1 = Link partner 10BT full-duplex capable. 0 = Link partner not 10BT full-duplex capable.	Bank 45 0x0A bit 6
0	0	RO	**Partner 10BT Half-Duplex Capability** 1 = Link partner 10BT half-duplex capable. 0 = Link partner not 10BT half-duplex capable.	Bank 45 0x0A bit 5

Bank 50 Port 2 Control Register 1 (0x00): P2CR1

This register contains the global per port control for the switch function. See description in P1CR1, Bank 48 (0x00)

B**ank 50 Port 2 Control Register 2 (0x02): P2CR2**

This register contains the global per port control for the switch function. See description in P1CR2, Bank 48 (0x02)

Bank 50 Port 2 VID Control Register (0x04): P2VIDCR

This register contains the global per port control for the switch function. See description in P1VIDCR, Bank 48 (0x04)

Bank 50 Port 2 Control Register 3 (0x06): P2CR3

This register contains the global per port control for the switch function. See description in P1CR3, Bank 48 (0x06)

Bank 50 Port 2 Ingress Rate Control Register (0x08): P2IRCR

This register contains per port ingress rate control. See description in P1IRCR, Bank 48 (0x08)

Bank 50 Port 2 Egress Rate Control Register (0x0A): P2ERCR

This register contains per port egress rate control. See description in P1ERCR, Bank 48 (0x0A)

Bank 51 Port 2 PHY Special Control/Status, LinkMD (0x00): P2SCSLMD

TABLE 4-96: PORT 2 PHY SPECIAL CONTROL/STATUS, LINKMD (0X00): P2SCSLMD

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**Vct_10m_Short** 1 = Less than 10 meter short.	Bank 47 0x04 bit 12
14 - 13	0x0	RO	**Vct_Result** [00] = Normal condition. [01] = Open condition has been detected in cable. [10] = Short condition has been detected in cable. [11] = Cable diagnostic test has failed.	Bank 47 0x04 bit 14-13
12	0	RW/SC	**Vct_Enable** 1 = Cable diagnostic test is enabled. It is self-cleared after the CDT test is done. 0 = Indicates that the cable diagnostic test is completed and the status information is valid for reading.	Bank 47 0x04 bit 15
11	0	RW	**Force_Link** Force link. 1 = Force link pass. 0 = Normal operation.	Bank 47 0x06 bit 3
10	1	RW	**Pwrsave** Power-saving. 1 = disable power saving. 0 = enable power saving.	Bank 47 0x06 bit 2
9	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at Port 2's PHY (RXP2/RXM2 −> TXP2/TXM2, (see Figure 7-2) 0 = Normal operation	Bank 47 0x06 bit 1
8 - 0	0x000	RO	**Vct_Fault_Count** Distance to the fault. It's approximately 0.4m*CDT-Fault_Count.	Bank 47 0x04 bit 8-0

Bank 51 Port 2 Control Register 4 (0x02): P2CR4

This register contains the global per port control for the switch function.

TABLE 4-97: PORT 2 CONTROL REGISTER 4 (0X02): P2CR4

Bit	Default	R/W	Description	Bit Same As:
15	0	RW	**LED Off** 1 = Turn off all of the port 2 LEDs (P2LED3, P2LED2, P2LED1, P2LED0). These pins are driven high if this bit is set to one. 0 = normal operation.	Bank 46 0x00 bit 0
14	0	RW	**Txids** 1 = disable the port's transmitter. 0 = normal operation.	Bank 46 0x00 bit 1
13	0	RW	**Restart Auto-Negotiation** (Note 1) 1 = Restart auto-negotiation. 0 = Normal operation.	Bank 46 0x00 bit 9
12	0	RO	Reserved	Bank 46 0x00 bit 2
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation.	Bank 46 0x00 bit 11
10	0	RW	**Disable Auto MDI/MDI-X** 1 = Disable Auto-MDI/MDI-X function. 0 = Enable Auto-MDI/MDI-X function.	Bank 46 0x00 bit 3
9	0	RW	**Force MDI-X** 1 = If Auto-MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = Do not force PHY into MDI-X mode.	Bank 46 0x00 bit 4
8	0	RW	**Far-End Loopback** 1 = Perform loopback, as indicated: Start: RXP2/RXM2 (Port 2). Loopback: PMD/PMA of Port 1's PHY. End: TXP2/TXM2 (Port 2). 0 = Normal operation.	Bank 46 0x00 bit 14
7	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation is enabled. 0 = Disable auto-negotiation, speed, and duplex are decided by bits [6:5] of the same register.	Bank 46 0x00 bit 12
6	1	RW	**Force Speed** 1 = Force 100BT if auto-negotiation is disabled (bit [7]). 0 = Force 10BT if auto-negotiation is disabled (bit [7]).	Bank 46 0x00 bit 13
5	1	RW	**Force Duplex** 1 = Force full-duplex if auto-negotiation is disabled. 0 = Force half-duplex if auto-negotiation is disabled. This bit also determines duplex if auto-negotiation is enabled but fails. When AN is enabled, this bit should be set to zero.	Bank 46 0x00 bit 8
4	1	RW	**Advertised Flow Control Capability** 1 = Advertise flow control (pause) capability. 0 = Suppress flow control (pause) capability from transmission to link partner.	Bank 46 0x08 bit 10
3	1	RW	**Advertised 100BT Full-Duplex Capability** 1 = Advertise 100BT full-duplex capability. 0 = Suppress 100BT full-duplex capability from transmission to link partner.	Bank 46 0x08 bit 8

TABLE 4-97: PORT 2 CONTROL REGISTER 4 (0X02): P2CR4

Bit	Default	R/W	Description	Bit Same As:
2	1	RW	**Advertised 100BT Half-Duplex Capability** 1 = Advertise 100BT half-duplex capability. 0 = Suppress 100BT half-duplex capability from transmission to link partner.	Bank 46 0x08 bit 7
1	1	RW	**Advertised 10BT Full-Duplex Capability** 1 = Advertise 10BT full-duplex capability. 0 = Suppress 10BT full-duplex capability from transmission to link partner.	Bank 46 0x08 bit 6
0	1	RW	**Advertised 10BT Half-Duplex Capability** 1 = Advertise 10BT half-duplex capability. 0 = Suppress 10BT half-duplex capability from transmission to link partner.	Bank 46 0x08 bit 5

Bank 51 Port 2 Status Register (0x04): P2SR

This register contains the global per port status for the chip function.

TABLE 4-98: PORT 2 STATUS REGISTER (0X04)

Bit	Default Value	R/W	Description	Same Bit As
15	1	R/W	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Microchip Auto MDI-X mode.	Bank 46 0x00 bit 5
14	0	RO	Reserved	—
13	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bank 47 0x06 bit 5
12	0	RO	**Receive Flow Control Enable** 1 = Receive flow control feature is active. 0 = Receive flow control feature is inactive.	—
11	0	RO	**Transmit Flow Control Enable** 1 = Transmit flow control feature is active. 0 = Transmit flow control feature is inactive.	—
10	0	RO	**Operation Speed** 1 = Link speed is 100 Mbps. 0 = Link speed is 10 Mbps.	—
9	0	RO	**Operation Duplex** 1 = Link duplex is full. 0 = Link duplex is half.	—
8	0	RO	Reserved	Bank 46 0x02 bit 4
7	0	RO	**MDI-X Status** 1 = MDI. 0 = MDI-X.	Bank 47 0x06 bit 4
6	0	RO	**AN Done** 1 = AN done. 0 = AN not done.	Bank 46 0x02 bit 5
5	0	RO	**Link Good** 1 = Link good. 0 = Link not good.	Bank 46 0x02 bit 2
4	0	RO	**Partner flow control capability** 1 = Link partner flow control (pause) capable. 0 = Link partner not flow control (pause) capable.	Bank 46 0x0A bit 10

TABLE 4-98: PORT 2 STATUS REGISTER (0X04) (CONTINUED)

Bit	Default Value	R/W	Description	Same Bit As
3	0	RO	**Partner 100BT full-duplex capability** 1 = Link partner 100BT full-duplex capable. 0 = Link partner not 100BT full-duplex capable.	Bank 46 0x0A bit 8
2	0	RO	**Partner 100BT half-duplex capability** 1 = Link partner 100BT half-duplex capable. 0 = Link partner not 100BT half-duplex capable.	Bank 46 0x0A bit 7
1	0	RO	**Partner 10BT full-duplex capability** 1 = Link partner 10BT full-duplex capable. 0 = Link partner not 10BT full-duplex capable.	Bank 46 0x0A bit 6
0	0	RO	**Partner 10BT half-duplex capability** 1 = Link partner 10BT half-duplex capable. 0 = Link partner not 10BT half-duplex capable.	Bank 46 0x0A bit 5

Bank 52 Host Port Control Register 1 (0x00): P3CR1

This register contains the global per port control for the switch function. See description in P1CR1, Bank 48 (0x00)

Bank 52 Host Port Control Register 1 (0x02): P3CR2

This register contains control bits for the switch Port 3 function.

TABLE 4-99: PORT 3 CONTROL REGISTER 2 (0X02): P3CR2

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RO	Reserved
11	0	RO	Reserved
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No receive monitoring.

TABLE 4-99: PORT 3 CONTROL REGISTER 2 (0X02): P3CR2 (CONTINUED)

Bit	Default	R/W	Description
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No transmit monitoring.
4	0	RO	Reserved
3	0	RW	**User Priority Ceiling** 1 = if the packet’s “user priority field” is greater than the “user priority field” in the port default tag register, replace the packet’s “user priority field” with the “user priority field” in the port default tag register. 0 = do not compare and replace the packet’s ‘user priority field.”
2 - 0	0x7	RW	**Port VLAN Membership** Define the port’s Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A ‘1’ includes a port in the membership; a ‘0’ excludes a port from the membership.

Bank 52 Host Port VID Control Register (0x04): P3VIDCR

This register contains the global per port control for the switch function. See description in P1VIDCR, Bank 48 (0x04)

Bank 52 Host Port Control Register 3 (0x06): P3CR3

This register contains the global per port control for the switch function. See description in P1CR3, Bank 48 (0x06)

Bank 52 Host Port Ingress Rate Control Register (0x08): P3IRCR

This register contains per port ingress rate control. See description in P1IRCR, Bank 48 (0x08)

Bank 52 Host Port Egress Rate Control Register (0x0A): P3ERCR

This register contains per port egress rate control. See description in P1ERCR, Bank 48 (0x0A)

Banks 53 – 63: Reserved

Except Bank Select Register (0xE)

4.4 Management Information Base (MIB) Counters

The KSZ8862M provides 34 MIB counters for each port. These counters are used to monitor the port activity for network management. The MIB counters are formatted “per port” as shown in Table 4-100 and “all ports dropped packet” as shown in Table 4-102.

TABLE 4-100: FORMAT OF PER PORT MIB COUNTERS

Bit	Name	R/W	Description	Default
31	Overflow	RO	1 = Counter overflow. 0 = No counter overflow.	0
30	Count Valid	RO	1 = Counter value is valid. 0 = Counter value is not valid.	0
29 - 0	Counter Values	RO	Counter value (read clear)	0x00000000

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for both Ethernet ports are:

Port 1, base address is 0x00 and range is from 0x00 to 0x1f.

Port 2, base address is 0x20 and range is from 0x20 to 0x3f.

Per port MIB counters are read using indirect access control register in IACR, Bank 42 (0x00) and indirect access data registers in IADR4[15:0], IADR5[31:16]. Table 4-101 shows the port 1 MIB counters address memory offset.

TABLE 4-101: PORT 1 MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets
0x1	Reserved	Reserved
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 bytes)
0x5	RxJabbers	Rx packets longer than 1536 bytes w/ either CRC errors, alignment errors, or symbol errors
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1916) bytes w/ an integral number of bytes and a bad CRC
0x8	RxAlignmentError	Rx packets within (64,1916) bytes w/ a non-integral number of bytes and a bad CRC
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in EtherType field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length

TABLE 4-101: PORT 1 MIB COUNTERS INDIRECT MEMORY OFFSETS (CONTINUED)

Offset	Counter Name	Description
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1916 octets in length
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets
0x15	Reserved	Reserved
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multicast packets)
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half-duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

TABLE 4-102: ALL PORTS DROPPED PACKET" MIB COUNTERS FORMAT

Bit	Default	R/W	Description
30 - 16	—	RO	Reserved
15 - 0	0x0000	RO	Counter value

Note: "All Ports Dropped Packet" MIB Counters do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

"All Ports Dropped Packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 4-103.

TABLE 4-103: "ALL PORTS DROPPED PACKET" MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x100	Port1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port2 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port2 RX Drop Packets	RX packets dropped due to lack of resources

Examples:

1. MIB Counter Read (read port 1 “Rx64Octets” counter at indirect address offset 0x0E)

Write to reg. IACR with 0x1C0E (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADR5 (MIB counter value 31-16) // If bit 31 = 1, there was a counter overflow

// If bit 30 = 0, restart (re-read) from this register

Read reg. IADR4 (MIB counter value 15-0)

2. MIB Counter Read (read port 2 “Rx64Octets” counter at indirect address offset 0x2E)

Write to reg. IACR with 0x1C2E (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADR5 (MIB counter value 31-16) // If bit 31 = 1, there was a counter overflow

// If bit 30 = 0, restart (re-read) from this register

Read reg. IADR4 (MIB counter value 15-0)

3. MIB Counter Read (read “Port1 TX Drop Packets” counter at indirect address offset 0x100)

Write to reg. IACR with 0x1d00 (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADR4 (MIB counter value 15-0)

4.4.1 ADDITIONAL MIB INFORMATION

Per Port MIB counters are designed as “read clear”. That is, these counters will be cleared after they are read.
All Ports Dropped Packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

4.5 Static MAC Address Table

The KSZ8862M supports both a static and a dynamic MAC address table. In response to a Destination Address (DA) look up, The KSZ8862M searches both tables to make a packet forwarding decision. In response to a Source Address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. These entries in the static table will not be aged out by the KSZ8862M.

TABLE 4-104: STATIC MAC TABLE FORMAT (8 ENTRIES)

Bit	Default Value	R/W	Description
57 - 54	0000	RW	**FID** Filter VLAN ID − identifies one of the 16 active VLANs.
53	0	R/W	**Use FID** 1 = Specifies the use of FID+MAC for static table look up. 0 = Specifies only the use of MAC for static table look up.
52	0	R/W	**Override** 1 = Overrides the port setting transmit enable = “0” or receive enable = “0” setting. 0 = Specifies no override.
51	0	R/W	**Valid** 1 = Specifies that this entry is valid, and the look up result will be used. 0 = Specifies that this entry is not valid.

TABLE 4-104: STATIC MAC TABLE FORMAT (8 ENTRIES)

Bit	Default Value	R/W	Description
50 - 48	000	R/W	**Forwarding Ports** These 3 bits control the forwarding port(s): 000 = No forward. 001 = Forward to Port 1. 010 = Forward to Port 2. 100 = Forward to Port 3. 011 = Forward to Port 1 and Port 2. 110 = Forward to Port 2 and Port 3. 101 = Forward to Port 1 and Port 3. 111 = Broadcasting (excluding the ingress port).
47 - 0	0	R/W	**MAC Address** 48−bit MAC Address

Static MAC Table Lookup Examples:

Static Address Table Read (read the second entry at indirect address offset 0x01)

Write to Reg. IACR with 0x1001 (set indirect address and trigger a read static MAC table operation)

Then:

Read Reg. IADR3 (static MAC table bits [57:48])

Read Reg. IADR2 (static MAC table bits [47:32])

Read Reg. IADR5 (static MAC table bits [31:16])

Read Reg. IADR4 (static MAC table bits [15:0])

Static Address Table Write (write the eighth entry at indirect address offset 0x07)

Write to Reg. IADR3 (static MAC table bits [57:48])

Write to Reg. IADR2 (static MAC table bits[47:32])

Write to Reg. IADR5 (static MAC table bits [31:16])

Write to Reg. IADR4 (static MAC table bits [15:0])

Write to Reg. IACR with 0x0007 (set indirect address and trigger a write static MAC table operation)

4.6 Dynamic MAC Address Table

The Dynamic MAC Address (Table 4-105) is a read-only table.

TABLE 4-105: DYNAMIC MAC ADDRESS TABLE FORMAT (1024 ENTRIES)

Bit	Default	R/W	Description
71	—	RO	**Data Not Ready** 1 = Specifies that the entry is not ready, continue retrying until bit is set to “0”. 0 = Specifies that the entry is ready.
70 - 67	—	RO	Reserved
66	1	RO	**MAC Empty** 1 = Specifies that there is no valid entry in the table 0 = Specifies that there are valid entries in the table
65 - 56	0x000	RO	**Number of Valid Entries** Indicates how many valid entries in the table. 0x3ff means 1K entries. 0x001 means 2 entries. 0x000 and bit [66] = “0” means 1 entry. 0x000 and bit [66] = “1” means 0 entry.

TABLE 4-105: DYNAMIC MAC ADDRESS TABLE FORMAT (1024 ENTRIES) (CONTINUED)

Bit	Default	R/W	Description
55 - 54	—	RO	**Timestamp** Specifies the 2−bit counter for internal aging.
53 - 52	00	RO	**Source Port** Identifies the source port where FID+MAC is learned: 00 = Port 1 01 = Port 2 10 = Port 3 (host port)
51 - 48	0x0	RO	**FID** Specifies the filter ID.
47 - 0	0x0000_0000_0000	RO	**MAC Address** Specifies the 48−bit MAC Address.

Dynamic MAC Address Lookup Example:

1. Dynamic MAC Address Table Read (read the first entry at indirect address offset 0 and retrieve the MAC table size)

Write to Reg. IACR with 0x1800 (set indirect address and trigger a read dynamic MAC table operation)

Then:

Read Reg. IADR1 (dynamic MAC table bits [71:64]) // If bit [71] = “1”, restart (re-read) from this register

Read Reg. IADR3 (dynamic MAC table bits [63:48])

Read Reg. IADR2 (dynamic MAC table bits [47:32])

Read Reg. IADR5 (dynamic MAC table bits [31:16])

Read Reg. IADR4 (dynamic MAC table bits [15:0])

4.7 VLAN Table

The KSZ8862M uses the VLAN table to perform look-ups. If 802.1Q VLAN mode is enabled (SGCR2[15]), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (Filter ID), VID (VLAN ID), and VLAN membership as described in Table 4-106:

TABLE 4-106: VLAN TABLE FORMAT (16 ENTRIES)

Bit	Default	R/W	Description
19	1	RW	**Valid** 1 = Specifies that this entry is valid, the look up result will be used. 0 = Specifies that this entry is not valid.
18 - 16	111	R/W	**Membership** Specifies which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example: “101” means Port 3 and Port 1 are in this VLAN.
15 - 12	0x0	R/W	**FID** Specifies the Filter ID. The KSZ8862 supports 16 active VLANs represented by these four bit fields. The FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.
11 - 0	0x001	R/W	**VID** Specifies the IEEE 802.1Q 12 bits VLAN ID.

If 802.1Q VLAN mode is enabled, then KSZ8862 will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, then the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, then VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, then packet will be dropped and no address learning will take place. If the VID is valid, then FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, then the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, then the FID+SA will be learned.

VLAN Table Lookup Examples:

1. VLAN Table Read (read the third entry, at the indirect address offset 0x02)

Write to Reg. IACR with 0x1402 (set indirect address and trigger a read VLAN table operation)

Then:

Read Reg. IADR5 (VLAN table bits [19:16])

Read Reg. IADR4 (VLAN table bits [15:0])

2. VLAN Table Write (write the seventh entry, at the indirect address offset 0x06)

Write to Reg. IADR5 (VLAN table bits [19:16])

Write to Reg. IADR4 (VLAN table bits [15:0])

Write to Reg. IACR with 0x1406 (set indirect address and trigger a read VLAN table operation)

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... –0.5V to +4.0V

Input Voltage (all inputs) ..... –0.5V to +5.0V

Output Voltage (all outputs) ..... –0.5V to +4.0V

Storage Temperature (T_S) ..... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than those listed in the table above may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

5.2 Operating Ratings**

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... +3.1V to +3.5V

Ambient Operating Temperature for Commercial Options (T_A) ..... 0°C to +70°C

Maximum Junction Temperature (T_J) ..... +125°C

Thermal Resistance (Note 5-1) (Θ_{JA}) ..... +37.5°C/W

**The device is not guaranteed to function outside its operating ratings. Unused inputs must always be tied to an appropriate logic voltage level (Ground to VDD).

Note 5-1 No heat spreader (HS) in this package. The Θ_{JC}/Θ_{JA} is under air velocity 0 m/s.

Note: Do not drive input signals without power supplied to the device.

6.0 ELECTRICAL CHARACTERISTICS

T_A = 25°C. Specification is for packaged product only. Single port's transformer consumes an additional 45 mA @ 3.3V for 100BASE-TX and 70 mA @ 3.3V for 10BASE-T.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
Supply Current for 100BASE-TX Operation (Single Port @ 100% Utilization)						
100BASE-TX (analog core + PLL + digital core + transceiver + digital I/O)	I_{DDXIO}	—	153	—	mA	VDDATX, VDDARX, VDDIO = 3.3V
Supply Current for 10BASE-T Operation (Single Port @ 100% Utilization)						
10BASE-T (analog core + PLL + digital core + transceiver + digital I/O)	I_{DDXIO}	—	97	—	mA	VDDATX, VDDARX, VDDIO = 3.3V
CMOS Inputs						
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input Current	I_{IN}	–10	—	10	µA	V_{IN} = GND ~ V_{DDIO}
CMOS Outputs						
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –8 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output Tri-State Leakage	$\|I_{OZ}\|$	—	—	10	µA	—
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	±0.95	—	±1.05	V	100Ω termination across differential output.
Output Voltage Imbalance	V_{IMB}	—	—	2	%	100Ω termination across differential output.
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty Cycle Distortion	—	—	—	±0.25	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of I_{SET}	V_{SET}	—	0.5	—	V	—
Output Jitter	—	—	0.7	1.4	ns	Peak-to-peak
10BASE-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	—	2.4	—	V	100Ω termination across differential output.
Output Jitter	—	—	1.8	3.5	ns	Peak-to-peak
10BASE-FL/100BASE-SX Transmit						
Transmit Output Current on Pin TXM1	I_{FO}(± 5%)	40	60	97	mA	VDDATX, VDDARX, VDDIO = 3.3V
10BASE-FL Receive on Pin RXM1						
Signal Detect Assertion Threshold	V_{10FL}	2.5	—	—	mV	RMS
100BASE-SX Receive on Pin RXM1						
Signal Detect Assertion Threshold	V_{100SX}	16	—	—	mV	RMS
10BASE-T Receive						
Squelch Threshold	V_{SQ}	—	400	—	mV	5 MHz square wave

7.0 TIMING SPECIFICATIONS

7.1 Asynchronous Timing without using Address Strobe (ADSN = 0)

FIGURE 7-1: ASYNCHRONOUS CYCLE – ADSN = 0

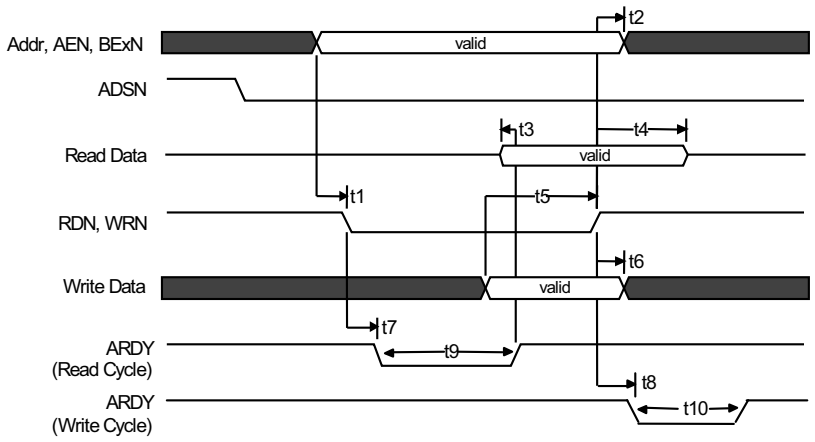


TABLE 7-1: ASYNCHRONOUS CYCLE (ADSN = 0) TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	A1-A15, AEN, BExN[3:0] valid to RDN, WRN active	0	—	—	ns
t2	A1-A15, AEN, BExN[3:0] hold after RDN inactive (assume ADSN tied Low)	0	—	—	ns
	A1-A15, AEN, BExN[3:0] hold after WRN inactive (assume ADSN tied Low)	1	—	—	
t3	Read data valid to ARDY rising	—	—	0.8	ns
t4	Read data to hold RDN inactive	4	—	—	ns
t5	Write data setup to WRN inactive	4	—	—	ns
t6	Write data hold after WRN inactive	2	—	—	ns
t7	Read active to ARDY Low	—	—	8	ns
t8	Write inactive to ARDY Low	—	—	8	ns
t9	ARDY low (wait time) in read cycle (Note 7-1) (It is 0 ns to read bank select register and 40 ns to read QMU data register in turbo mode) (Note 7-2)	0	40	—	ns
	ARDY low (wait time) in read cycle (Note 7-1) (It is 0 ns to read bank select register and 80 ns to read QMU data register in normal mode)	0	80	—	
t10	ARDY low (wait time) in write cycle (Note 7-1) (It is 0 ns to write bank select register) (It is 36 ns to write QMU data register)	0	50	—	ns

Note 7-1 When CPU finished current Read or Write operation, it can do next Read or Write operation even the ARDY is low. During Read or Write operation if the ADRY is low, the CPU has to keep the RDN/WRN low until the ARDY returns to high.

Note 7-2 In order to speed up the ARDY low time to 40 ns, user has to use the turbo software driver which is only supported in the A6 device. Please refer to the “KSZ88xx Programmer's Guide” for detail.

7.2 Asynchronous Timing using Address Strobe (ADSN)

FIGURE 7-2: ASYNCHRONOUS CYCLE – USING ADSN

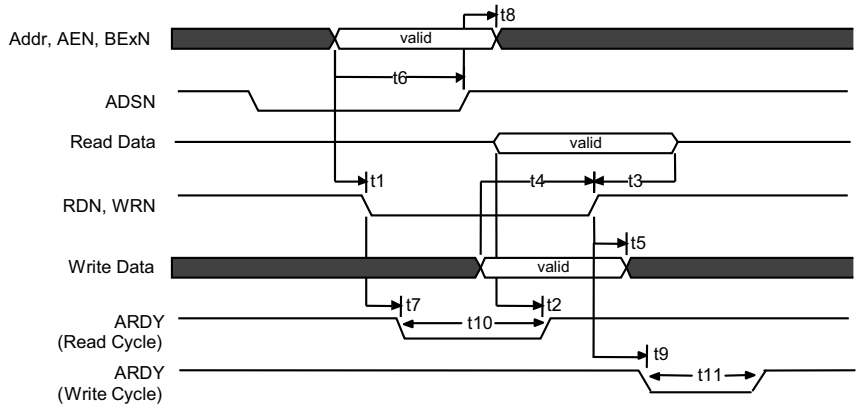


TABLE 7-2: ASYNCHRONOUS CYCLE USING ADSN TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	A1-A15, AEN, BExN[3:0] valid to RDN, WRN active	0	—	—	ns
t2	Read data valid to ARDY rising	—	—	0.8	ns
t3	Read data hold to RDN inactive	4	—	—	ns
t4	Write data setup to WRN inactive	4	—	—	ns
t5	Write data hold after WRN inactive	2	—	—	ns
t6	A1-A15, AEN, nBE[3:0] setup to ADSN rising	4	—	—	ns
t7	Read active to ARDY Low	—	—	8	ns
t8	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2	—	—	ns
t9	Write inactive to ARDY Low	—	—	8	ns
t10	ARDY low (wait time) in read cycle (Note 7-1) (It is 0 ns to read bank select register and 40 ns to read QMU data register in turbo mode) (Note 7-2)	0	40	—	ns
	ARDY low (wait time) in read cycle (Note 7-1) (It is 0 ns to read bank select register and 80 ns to read QMU data register in normal mode)	0	80	—	
t11	ARDY low (wait time) in write cycle (Note 7-1) (It is 0 ns to write bank select register) (It is 36 ns to write QMU data register)	0	50	—	ns

Note 7-1 When CPU finished current Read or Write operation, it can do next Read or Write operation even the ARDY is low. During Read or Write operation if the ADRY is low, the CPU has to keep the RDN/WRN low until the ARDY returns to high.

Note 7-2 In order to speed up the ARDY low time to 40 ns, user has to use the turbo software driver which is only supported in the A6 device. Please refer to the “KSZ88xx Programmer's Guide” for detail.

7.3 Asynchronous Timing using DATACSN

FIGURE 7-3: ASYNCHRONOUS CYCLE – USING DATACSN

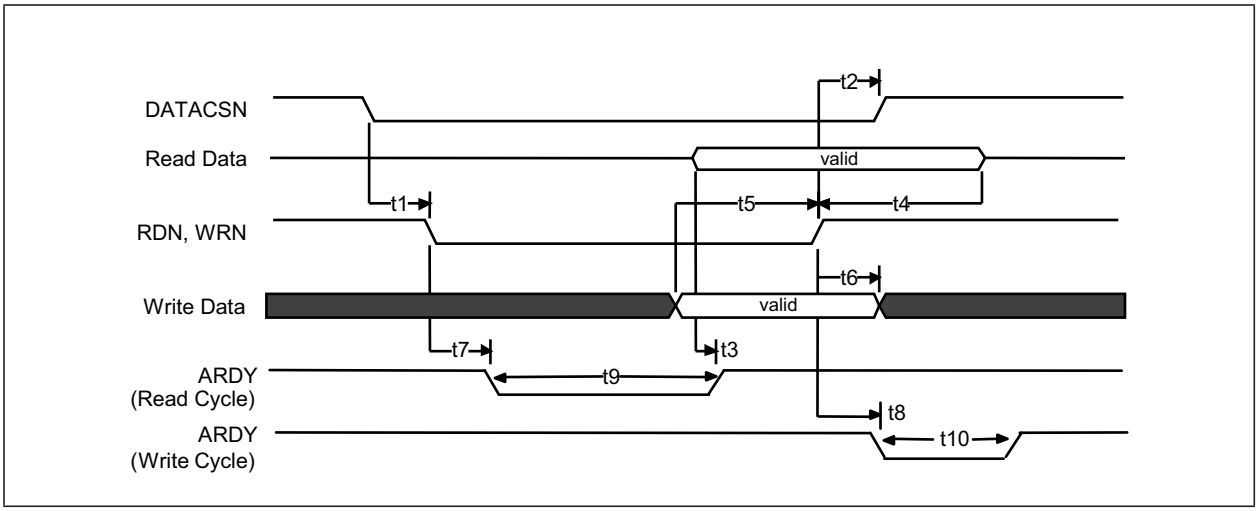


TABLE 7-3: ASYNCHRONOUS CYCLE USING DATACSN TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	DATACSN setup to RDN, WRN active	2	—	—	ns
t2	DATACSN hold after RDN, WRN inactive (assume ADSN tied Low)	0	—	—	ns
t3	Read data hold to ARDY rising	—	—	0.8	ns
t4	Read data to RDN hold	4	—	—	ns
t5	Write data setup to WRN inactive	4	—	—	ns
t6	Write data hold after WRN inactive	2	—	—	ns
t7	Read active to ARDY Low	—	—	8	ns
t8	Write inactive to ARDY Low	—	—	8	ns
t9	ARDY low (wait time) in read cycle (Note 7-1) (It is 0 ns to read bank select register and 40 ns to read QMU data register in turbo mode) (Note 7-2)	0	40	—	ns
	ARDY low (wait time) in read cycle (Note 7-1) (It is 0 ns to read bank select register and 80 ns to read QMU data register in normal mode)	0	80	—	
t10	ARDY low (wait time) in write cycle (Note 7-1) (It is 0 ns to write bank select register) (It is 36 ns to write QMU data register)	0	50	—	ns

Note 7-1 When CPU finished current Read or Write operation, it can do next Read or Write operation even the ARDY is low. During Read or Write operation if the ADRY is low, the CPU has to keep the RDN/WRN low until the ARDY returns to high.

Note 7-2 In order to speed up the ARDY low time to 40 ns, user has to use the turbo software driver which is only supported in the A6 device. Please refer to the “KSZ88xx Programmer's Guide” for detail.

7.4 Address Latching Timing for All Modes

FIGURE 7-4: ADDRESS LATCHING CYCLE FOR ALL MODES

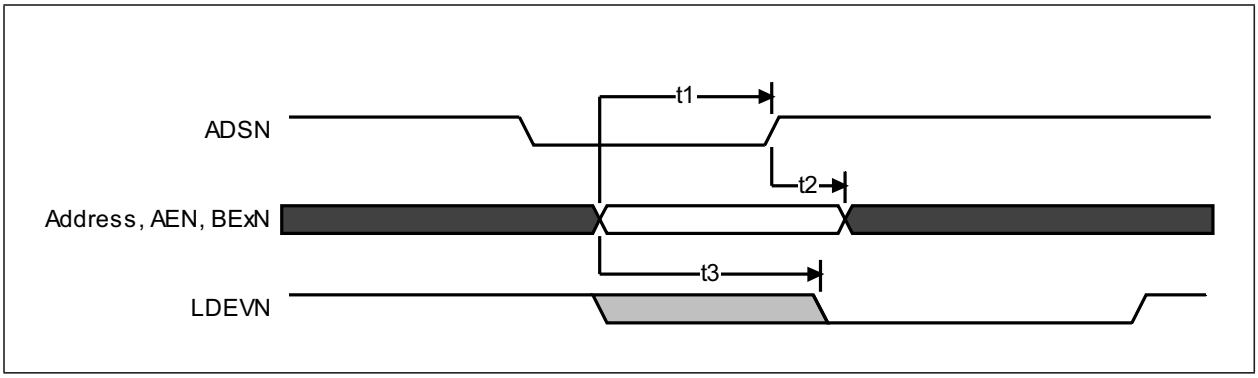


TABLE 7-4: ADDRESS LATCHING TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	A1-A15, AEN, BExN[3:0] setup to ADSN	4	—	—	ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2	—	—	ns
t3	A4-A15, AEN to LDEVN delay	—	—	5	ns

7.5 Synchronous Timing in Burst Write (VLBUSN = 1)

FIGURE 7-5: SYNCHRONOUS BURST WRITE CYCLES – VLBUSN = 1

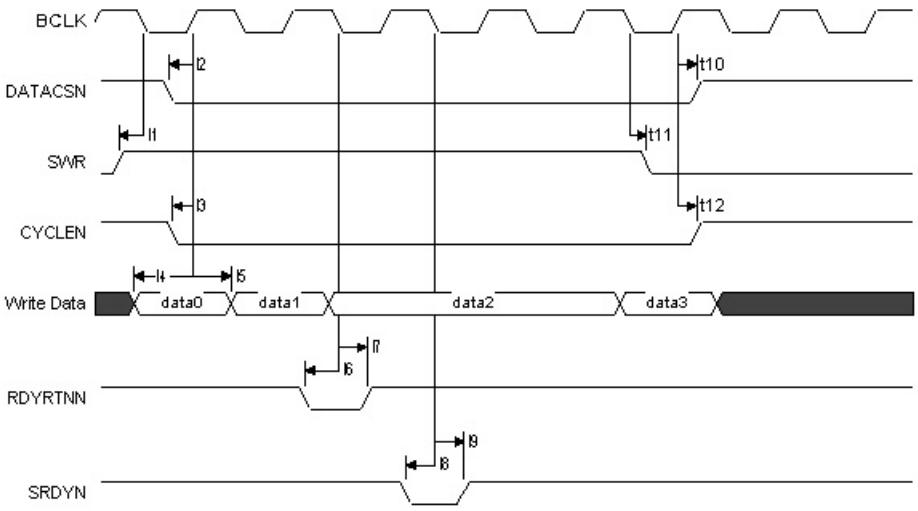


TABLE 7-5: SYNCHRONOUS BURST WRITE TIMING PARAMETERS

Symbol	Parameter	Min.	Max.	Units
t1	SWR setup to BCLK falling	4	—	ns
t2	DATDCSN setup to BCLK rising	4	—	ns
t3	CYCLEN setup to BCLK rising	4	—	ns
t4	Write data setup to BCLK rising	6	—	ns
t5	Write data hold to BCLK rising	2	—	ns
t6	RDYRTNN setup to BCLK falling	5	—	ns
t7	RDYRTNN hold to BCLK falling	3	—	ns
t8	SRDYN setup to BCLK rising	4	—	ns
t9	SRDYN hold to BCLK rising	3	—	ns
t10	DATACSN hold to BCLK rising	2	—	ns
t11	SWR hold to BCLK falling	2	—	ns
t12	CYCLEN hold to BCLK rising	2	—	ns

7.6 Synchronous Timing in Burst Read (VLBUSN = 1)

FIGURE 7-6: SYNCHRONOUS BURST READ CYCLES – VLBUSN = 1

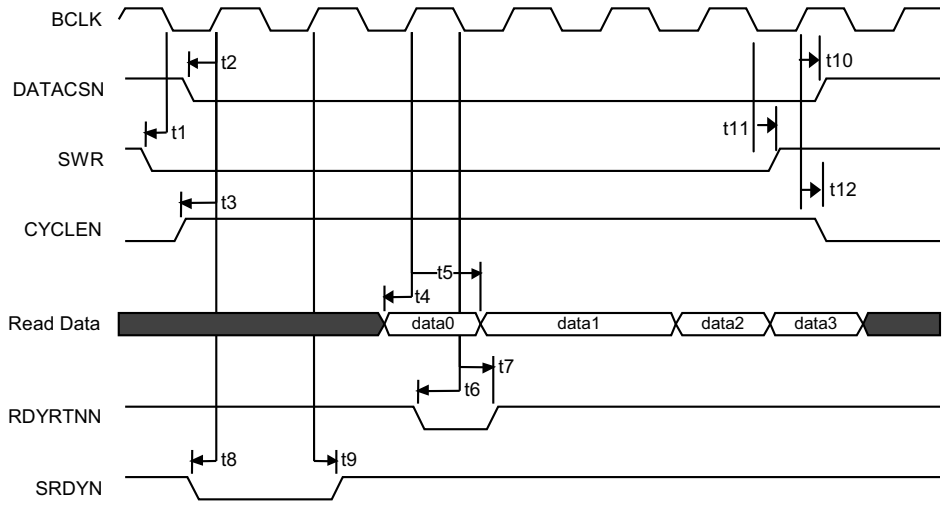


TABLE 7-6: SYNCHRONOUS BURST READ TIMING PARAMETERS

Symbol	Parameter	Min.	Max.	Units
t1	SWR setup to BCLK falling	4	—	ns
t2	DATDCSN setup to BCLK rising	4	—	ns
t3	CYCLEN setup to BCLK rising	4	—	ns
t4	Read data setup to BCLK rising	6	—	ns
t5	Read data hold to BCLK rising	2	—	ns
t6	RDYRTNN setup to BCLK falling	5	—	ns
t7	RDYRTNN hold to BCLK falling	3	—	ns
t8	SRDYN setup to BCLK rising	4	—	ns
t9	SRDYN hold to BCLK rising	3	—	ns
t10	DATACSN hold to BCLK rising	2	—	ns
t11	SWR hold to BCLK falling	2	—	ns
t12	CYCLEN hold to BCLK rising	2	—	ns

7.7 Synchronous Write Timing (VLBUSN = 0)

FIGURE 7-7: SYNCHRONOUS WRITE CYCLE – VLBUSN = 0

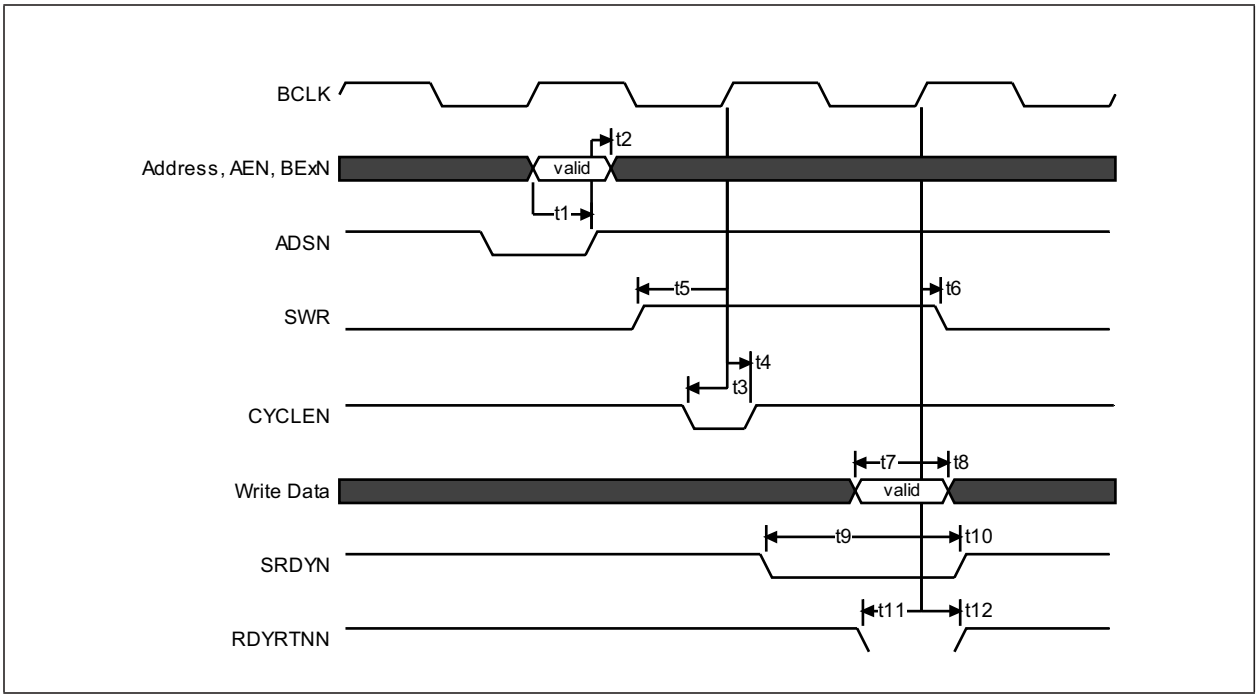


TABLE 7-7: SYNCHRONOUS WRITE (VLBUSN = 0) TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	A1-A15, AEN, BExN[3:0] setup to ADSN rising	4	—	—	ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2	—	—	ns
t3	CYCLEN setup to BCLK rising	4	—	—	ns
t4	CYCLEN hold after BCLK rising (non-burst mode)	2	—	—	ns
t5	SWR setup to BCLK	4	—	—	ns
t6	SWR hold after BCLK rising with SRDYN active	0	—	—	ns
t7	Write data setup to BCLK rising	5	—	—	ns
t8	Write data hold from BCLK rising	1	—	—	ns
t9	SRDYN setup to BCLK	8	—	—	ns
t10	SRDYN hold to BCLK	1	—	—	ns
t11	RDYRTNN setup to BCLK	4	—	—	ns
t12	RDYRTNN hold to BCLK	1	—	—	ns

7.8 Synchronous Read Timing (VLBUSN = 0)

FIGURE 7-8: SYNCHRONOUS READ CYCLE – VLBUSN = 0

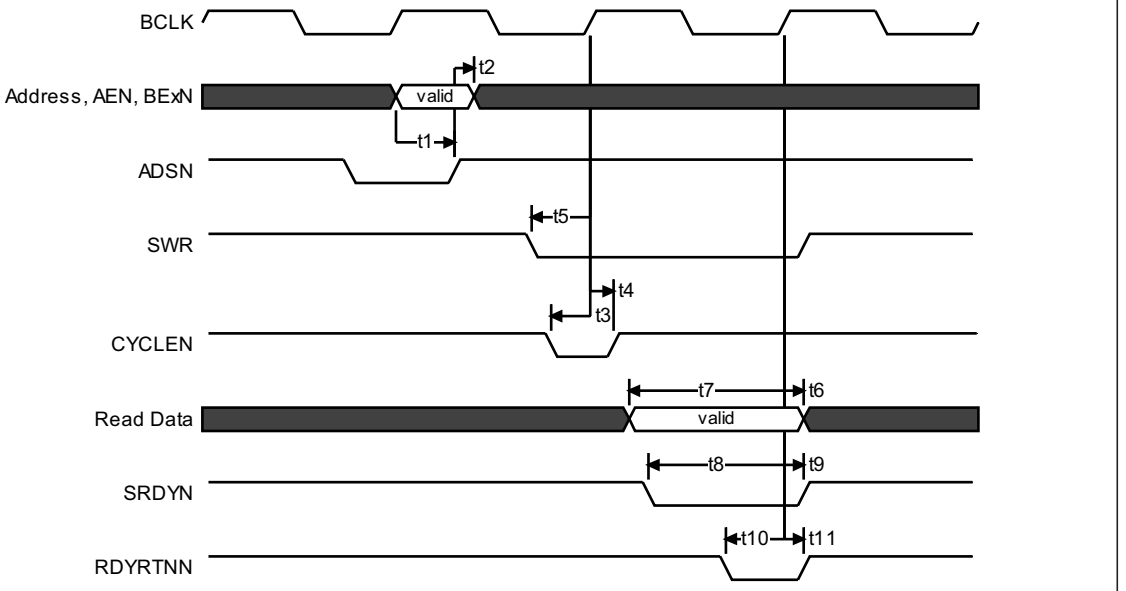


TABLE 7-8: SYNCHRONOUS READ (VLBUSN = 0) TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	A1-A15, AEN, BExN[3:0] setup to ADSN rising	4	—	—	ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2	—	—	ns
t3	CYCLEN setup to BCLK rising	4	—	—	ns
t4	CYCLEN hold after BCLK rising (non-burst mode)	2	—	—	ns
t5	SWR setup to BCLK	4	—	—	ns
t6	Read data hold from BCLK rising	1	—	—	ns
t7	Read data setup to BCLK	8	—	—	ns
t8	SRDYN setup to BCLK	8	—	—	ns
t9	SRDYN hold to BCLK	1	—	—	ns
t10	RDYRTNN setup to BCLK rising	4	—	—	ns
t11	RDYRTNN hold after BCLK rising	1	—	—	ns

7.9 Auto-Negotiation Timing

FIGURE 7-9: AUTO-NEGOTIATION TIMING

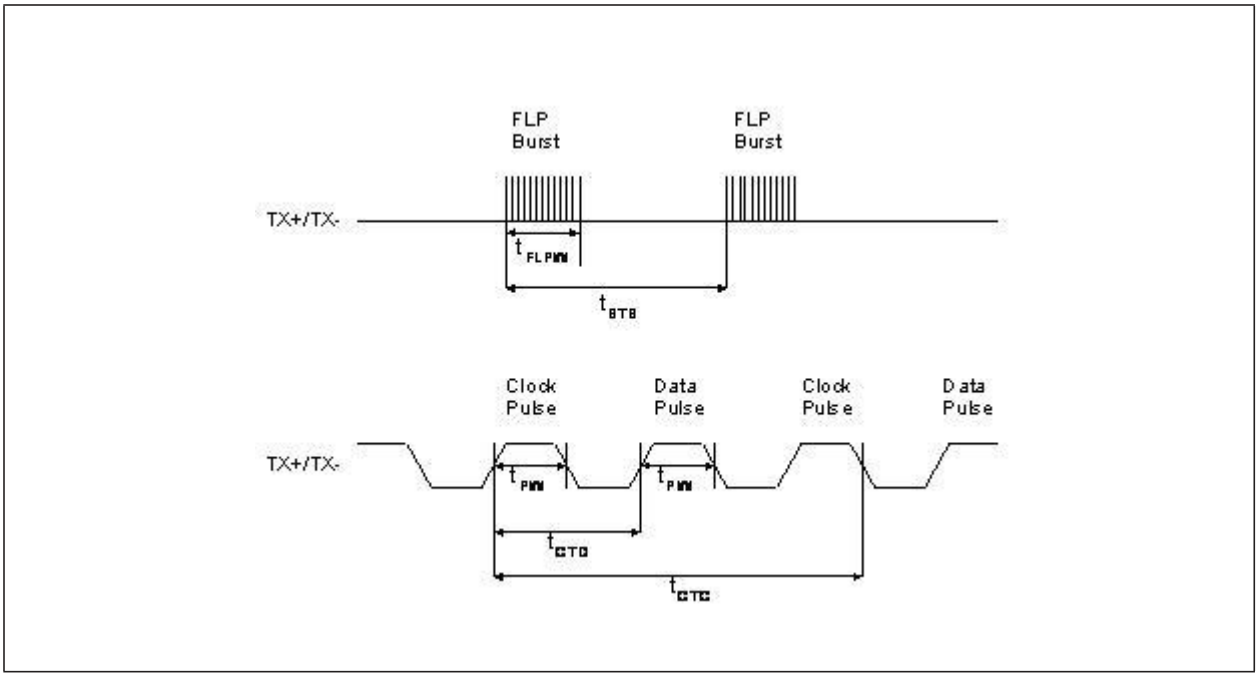


TABLE 7-9: AUTO-NEGOTIATION TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width	—	2	—	ms
t_{PW}	Clock/Data pulse width	—	100	—	ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
—	Number of Clock/Data pulses per burst	17	—	33	—

7.10 Reset Timing

As long as the stable supply voltages to reset High timing (minimum of 10 ms) are met, there is no power-sequencing requirement for the KSZ8841M supply voltages (3.3V).

The reset timing requirement is summarized in Figure 7-10 and Table 7-10.

FIGURE 7-10: RESET TIMING

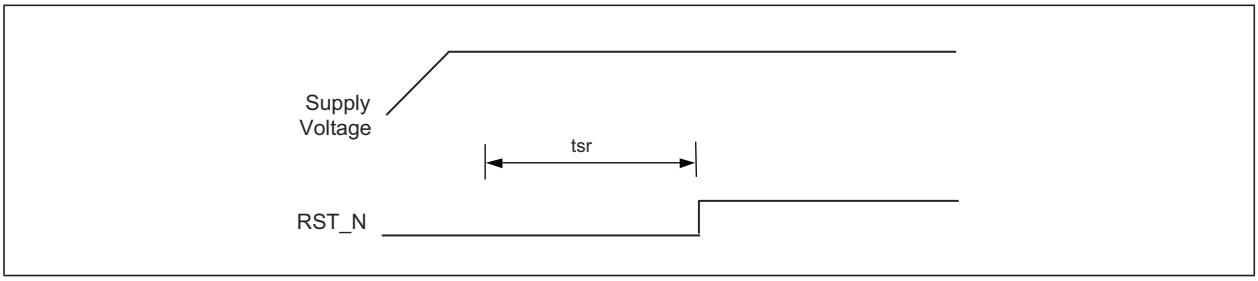


TABLE 7-10: RESET TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{SR}	Stable supply voltages to reset high	10	—	—	ms

7.11 EEPROM Timing

FIGURE 7-11: EEPROM READ CYCLE TIMING DIAGRAM

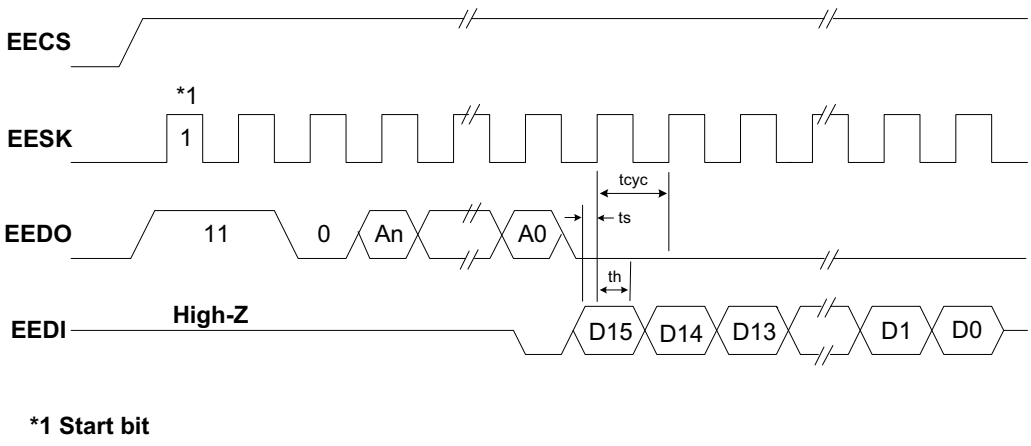


TABLE 7-11: EEPROM TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CYC}	Clock cycle	—	4 (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 0.8 (OBCR[1:0]=00 on-chip bus speed @ 125 MHz)	—	µs
t_S	Setup time	20	—	—	ns
t_h	Hold time	20	—	—	ns

8.0 SELECTION OF ISOLATION TRANSFORMERS

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 8-1 lists recommended transformer characteristics.

TABLE 8-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT : 1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
D.C. Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	1.0 dB	0 MHz to 65 MHz
HIPOT (min.)	1500 V_{RMS}	—

TABLE 8-2: QUALIFIED SINGLE-PORT MAGNETICS

Manufacturer	Part Number	Auto MDI-X
Bel Fuse	S558-5999-U7	Yes
Delta	LF8505	Yes
LanKom	LF-H41S	Yes
Pulse	H1102	Yes
Pulse (Low Cost)	H1260	Yes
Transpower	HB726	Yes
TDK (Mag Jack)	TLA-6T718	Yes

TABLE 8-3: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

Characteristic	Value
Frequency	25 MHz
Frequency Tolerance (max.)	±50 ppm
Load Capacitance (max.)	20 pF
Series Resistance	25Ω

9.0 PACKAGE OUTLINE

9.1 Package Marking Information

128-Lead PQFP*

```
MICREL
XXXXXXX-XX
XXX
YYWWA7
XXXXXYYWWNNN
YYWWNNN
●
```

Example

```
MICREL
KSZ8862-16
MQL
1921A7
G00001921917
1921917
●
```

128-Lead PQFP*

```
MICREL
XXXXXXX-XX
XXX-XX
YYWWA7
XXXXXYYWWNNN
YYWWNNN
●
```

Example

```
MICREL
KSZ8862-32
MQL-FX
2014A7
G00002014808
2014808
●
```

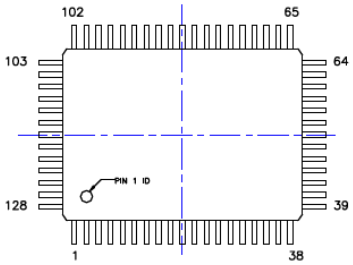
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

FIGURE 9-1: 128-LEAD PQFP 14 MM X 20 MM PACKAGE OUTLINE AND RECOMMENDED LAND PATTERN

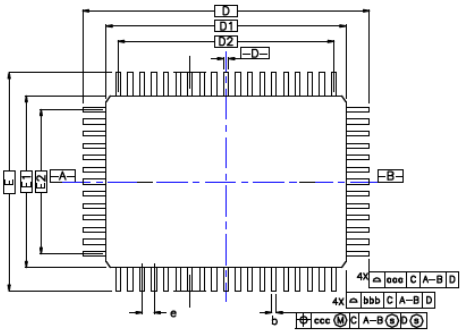
TITLE

128 LEAD PQFP 14x20mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

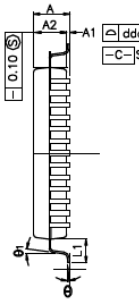
DRAWING #	PQFP14x20-128LD-PL-1	UNIT	MM [INCHES]



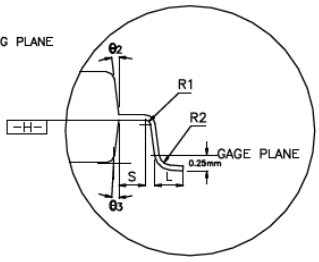
TOP VIEW
Note 1,2,3



BOTTOM VIEW
Note 1,2,3



SIDE VIEW
Note 1,2,3



DETAILED VIEW

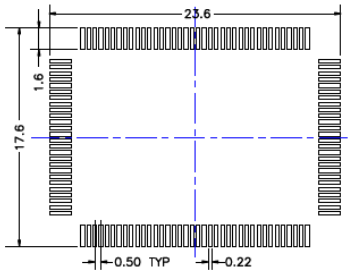
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2 , θ3	15° REF			15° REF		

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.
4. ALL UNITS IN mm. TOLERANCE +/− 0.05 IF NOT NOTED.



RECOMMENDED LAND PATTERN
Note 4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003324A (01-14-20)	—	Converted Micrel data sheet KSZ8862-16M/-32M to Microchip DS00003324A. Minor text changes throughout.

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Device	-XX	X	X	X	[X]	[-XX]	[-XX]
Part Number	Bus Design	Interface	Package	Supply Voltage	Tempera-ture	Port 1 Support	Media Type

Device:	KSZ8862: Two-Port Ethernet Switch with Non-PCI Interface and Fiber Support
Bus Design:	-16 = 8-bit or 16-bit -32 = 32-bit
Interface:	M = Non-PCI Interface
Package:	Q = 128-lead PQFP
Supply Voltage:	L = Single 3.3V Power Supply Supported with Internal 1.8V LDO
Temperature:	<blank> = 0°C to +70°C (Commercial)
Port 1 Support:	FX = Fiber Support on Port 1
Media Type:	<blank> = 66/Tray

Examples:

a) KSZ8862-16MQL:

8-Bit or 16-Bit Bus Design, Non-PCI Interface, 128-Lead PQFP, Single 3.3V Power Supply with Internal 1.8V LDO, Commercial Temperature Range, 66/Tray

b) KSZ8862-16MQL-FX:

8-Bit or 16-Bit Bus Design, Non-PCI Interface, 128-Lead PQFP, Single 3.3V Power Supply with Internal 1.8V LDO, Commercial Temperature Range, Fiber Support on Port 1, 66/Tray

c) KSZ8862-32MQL:

32-Bit Bus Design, Non-PCI Interface, 128-Lead PQFP, Single 3.3V Power Supply with Internal 1.8V LDO, Commercial Temperature Range, 66/Tray

d) KSZ8862-32MQL-FX:

32-Bit Bus Design, Non-PCI Interface, 128-Lead PQFP, Single 3.3V Power Supply with Internal 1.8V LDO, Commercial Temperature Range, Fiber Support on Port 1, 66/Tray

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Fax: 39-0331-466781

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UK - Wokingham
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Fax: 44-118-921-5820