

# 100370

## Low Power Universal Demultiplexer/Decoder

### General Description

The 100370 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable ( $\bar{E}$ ) inputs. Pin assignments for the  $\bar{E}$  inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables ( $\bar{E}_{1a}$  to  $\bar{E}_{1b}$ ,  $\bar{E}_{2a}$  to  $\bar{E}_{2b}$ ). Signals applied to auxiliary inputs  $H_a$ ,  $H_b$ , and  $H_c$  determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are  $A_{0a}$ ,  $A_{1a}$  and  $A_{0b}$ ,

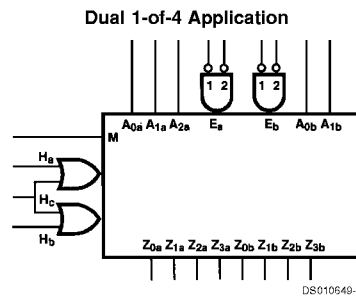
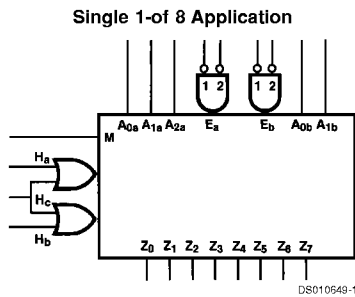
$A_{1b}$  with  $A_{2a}$  unused (i.e., left open, tied to  $V_{EE}$  or with LOW signal applied). In the 1-of-8 mode, the Address inputs are  $A_{0a}$ ,  $A_{1a}$ ,  $A_{2a}$  with  $A_{0b}$  and  $A_{1b}$  LOW or open. All inputs have 50 k $\Omega$  pull-down resistors.

### Features

- 35% power reduction of the 100170
- 2000V ESD protection
- Pin/function compatible with 100170
- Voltage compensated operating range = -4.2V to -5.7V

### Ordering Code:

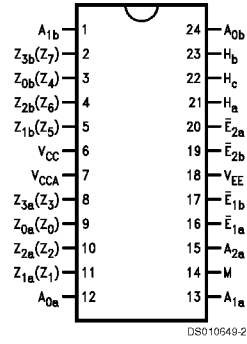
### Logic Symbols



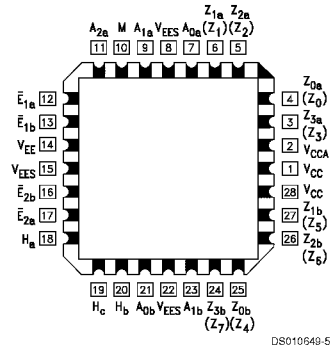
Pin Names	Description
$A_{na}, A_{nb}$	Address Inputs
$\bar{E}_{na}, \bar{E}_{nb}$	Enable Inputs
M	Mode Control Input
$H_a$	$Z_0-Z_3$ ( $\bar{Z}_{0a}-\bar{Z}_{3a}$ ) Polarity Select Input
$H_b$	$Z_4-Z_7$ ( $\bar{Z}_{0b}-\bar{Z}_{3b}$ ) Polarity Select Input
$H_c$	Common Polarity Select Input
$Z_0-Z_7$	Single 1-of-8 Data Outputs
$Z_{na}, Z_{nb}$	Dual 1-of-4 Data Outputs

## Connection Diagrams

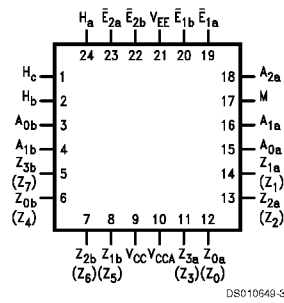
24-Pin DIP



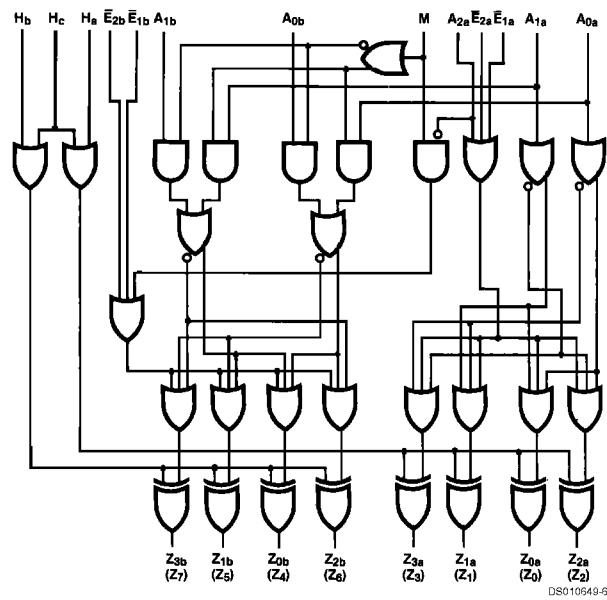
28-Pin PCC



24-Pin Quad Cerpak



## Logic Diagram



Note 1: ( $Z_n$ ) for 1-of-4 applications.

DS010649-6

## Truth Tables

### Dual 1-of-4 Mode ( $M = A_{2a} = H_c = \text{LOW}$ )

Inputs				Active HIGH Outputs ( $H_a$ and $H_b$ Inputs HIGH)				Active LOW Outputs ( $H_a$ and $H_b$ Inputs LOW)			
$\bar{E}_{1a}$	$\bar{E}_{2a}$	$A_{1a}$	$A_{0a}$	$Z_{0a}$	$Z_{1a}$	$Z_{2a}$	$Z_{3a}$	$Z_{0a}$	$Z_{1a}$	$Z_{2a}$	$Z_{3a}$
$\bar{E}_{1b}$	$\bar{E}_{2b}$	$A_{1b}$	$A_{0b}$	$Z_{0b}$	$Z_{1b}$	$Z_{2b}$	$Z_{3b}$	$Z_{0b}$	$Z_{1b}$	$Z_{2b}$	$Z_{3b}$
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

### Single 1-of-8 Mode ( $M = \text{HIGH}$ ; $A_{0b} = A_{1b} = H_a = H_b = \text{LOW}$ )

Inputs					Active HIGH Outputs (Note 2) ( $H_c$ Input HIGH)							
$\bar{E}_1$	$\bar{E}_2$	$A_{2a}$	$A_{1a}$	$A_{0a}$	$Z_0$	$Z_1$	$Z_2$	$Z_3$	$Z_4$	$Z_5$	$Z_6$	$Z_7$
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

$\bar{E}_1 = \bar{E}_{1a}$  and  $\bar{E}_{1b}$  wired;  $\bar{E}_2 = \bar{E}_{2a}$  and  $\bar{E}_{2b}$  wired

Note 2: for  $H_c = \text{LOW}$ , output states are complemented

## Absolute Maximum Ratings (Note 3)

Above which the useful life may be impaired.

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 4)	≥2000V

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V

**Note 3:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 4:** ESD testing conforms to MIL-STD-883, Method 3015.

## Commercial Version DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$  (Note 5)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV		
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610	mV		
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}$ (Min)	
$I_{IH}$	Input HIGH Current			240	μA	$V_{IN} = V_{IH}$ (Max)	
$I_{EE}$	Power Supply Current	-95		-50	mA	Inputs Open	

**Note 5:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	0.75	1.85	0.75	1.85	0.85	2.05	ns	Figures 1, 2
$t_{PHL}$									
$t_{PLH}$	Propagation Delay $A_{na}, A_{nb}$ to Output	0.75	2.20	0.75	2.20	0.75	2.30		
$t_{PHL}$									
$t_{PLH}$	Propagation Delay $H_a, H_b, H_c$ to Output	0.75	2.20	0.75	2.20	0.75	2.20		
$t_{PHL}$									
$t_{PLH}$	Propagation Delay M to Output	1.10	2.70	1.10	2.70	1.10	3.00		
$t_{PHL}$									
$t_{TLH}$	Transition Time	0.40	1.30	0.40	1.30	0.40	1.30	ns	
$t_{THL}$	20% to 80%, 80% to 20%								

## PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	0.75	1.65	0.75	1.65	0.85	1.85	ns	Figures 1, 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_{na}, A_{nb}$ to Output	0.75	2.00	0.75	2.00	0.75	2.10	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $H_a, H_b, H_c$ to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay M to Output	1.10	2.50	1.10	2.50	1.10	2.80	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	

## Industrial Version PCC DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$  (Note 6)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Typ	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with $50\Omega$ to $-2.0V$
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620	mV		
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with $50\Omega$ to $-2.0V$
$V_{OLC}$	Output LOW Voltage		-1565		-1610	mV		
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50		0.50		$\mu A$	$V_{IN} = V_{IL}$ (Min)	
$I_{IH}$	Input HIGH Current		300		240	$\mu A$	$V_{IN} = V_{IH}$ (Max)	
$I_{EE}$	Power Supply Current	-95	-50	-95	-50	mA	Inputs Open	

**Note 6:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## PCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	0.75	1.65	0.75	1.65	0.85	1.85	ns	Figures 1, 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_{na}, A_{nb}$ to Output	0.65	2.00	0.75	2.00	0.75	2.10	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $H_a, H_b, H_c$ to Output	0.70	2.00	0.75	2.00	0.75	2.00	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay M to Output	1.10	2.50	1.10	2.50	1.10	2.80	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.40	1.30	0.40	1.20	0.40	1.20	ns	

## Military Version—Preliminary DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with $50\Omega$ to $-2.0V$
		-1085	-870	mV	$-55^\circ C$		
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$		
		-1830	-1555	mV	$-55^\circ C$		
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with $50\Omega$ to $-2.0V$
		-1085		mV	$-55^\circ C$		
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$		
			-1555	mV	$-55^\circ C$		
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs	(Notes 7, 8, 9, 10)
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs	(Notes 7, 8, 9, 10)
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)	(Notes 7, 8, 9)
$I_{IH}$	Input HIGH Current $H_c, A_{0a}, A_{1a}, A_{2a}$ All Others		310	$\mu A$	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	(Notes 7, 8, 9)
			250	$\mu A$	$-55^\circ C$		
$I_{IH}$	$H_c, A_{0a}, A_{1a}, A_{2a}$ All Others		465	$\mu A$	$-55^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	(Notes 7, 8, 9)
			350	$\mu A$	$-55^\circ C$		
$I_{EE}$	Power Supply Current	-110	-70	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open	(Notes 7, 8, 9)

**Note 7:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ , then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 8:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.

**Note 9:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

**Note 10:** Guaranteed by applying specific input condition and testing  $V_{OH}/V_{OL}$ .

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	0.90	2.30	0.90	2.20	0.90	2.30	ns	Figures 1, 2	(Notes 11, 12, 13)
$t_{PLH}$	Propagation Delay $A_{na}, A_{nb}$ to Output	1.00	2.80	1.00	2.70	1.00	2.90	ns		
$t_{PLH}$	Propagation Delay $H_a, H_b, H_c$ to Output	1.00	3.00	1.00	2.90	1.00	3.00	ns		
$t_{PLH}$	Propagation Delay M to Output	1.50	3.90	1.60	3.80	1.60	3.90	ns		
$t_{TLH}$	Transition Time	0.45	1.70	0.45	1.70	0.45	1.80	ns		
$t_{THL}$	20% to 80%, 80% to 20%									(Note 14)

## AC Electrical Characteristics (Continued)

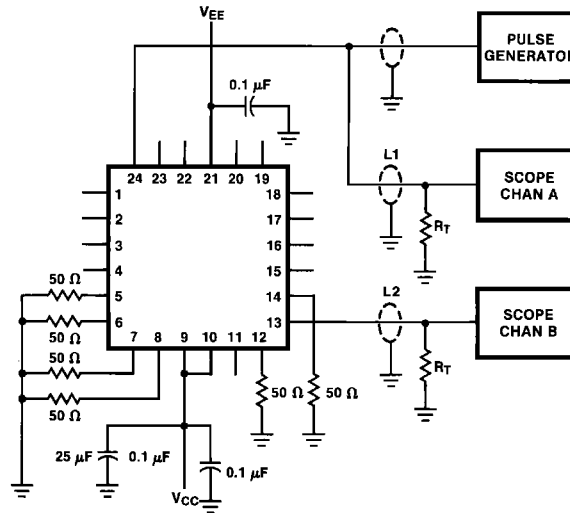
**Note 11:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^{\circ}\text{C}$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 12:** Screen tested 100% on each device at  $+25^{\circ}\text{C}$ , temperature only, Subgroup A9.

**Note 13:** Sample tested (Method 5005, Table I) on each Mfg. lot at  $+25^{\circ}\text{C}$ , Subgroup A9, and at  $+125^{\circ}\text{C}$ , and  $-55^{\circ}\text{C}$  Temp., Subgroups A10 and A11.

**Note 14:** Not tested at  $+25^{\circ}\text{C}$ ,  $+125^{\circ}\text{C}$  and  $-55^{\circ}\text{C}$  Temperature (design characterization data).

## Test Circuit



DS010549-7

### Notes:

$V_{CC}$ ,  $V_{CCA} = +2\text{V}$ ,  $V_{EE} = -2.5\text{V}$

L1 and L2 = equal length  $50\Omega$  impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling  $0.1\ \mu\text{F}$  from GND to  $V_{CC}$  and  $V_{EE}$

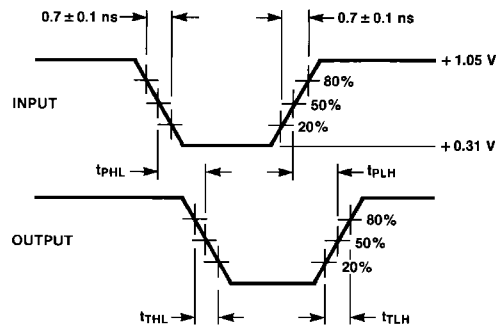
All unused outputs are loaded with  $50\Omega$  to GND

$C_L$  = Fixture and stray capacitance  $\leq 3\ \text{pF}$

Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

## Switching Waveforms



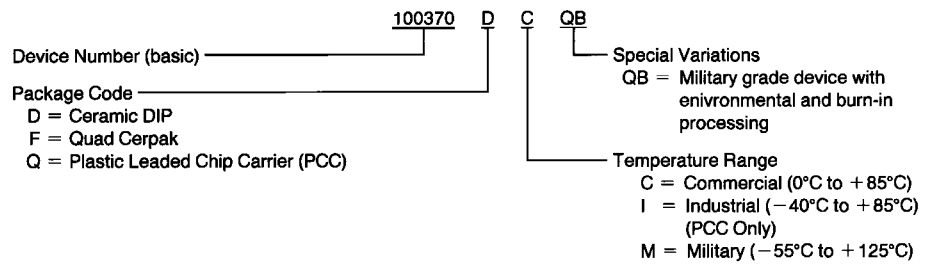
DS010549-8

FIGURE 2. Propagation Delay and Transition Times



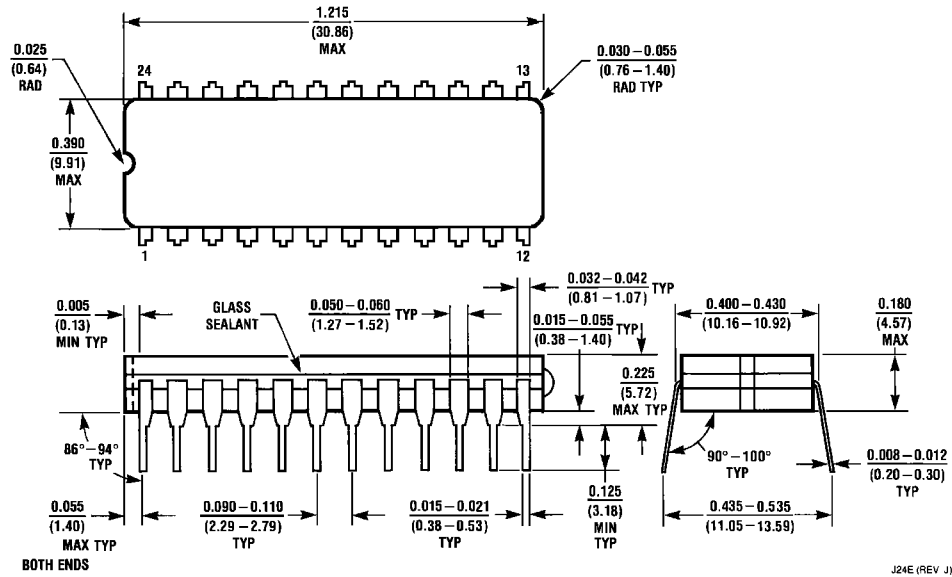
## Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



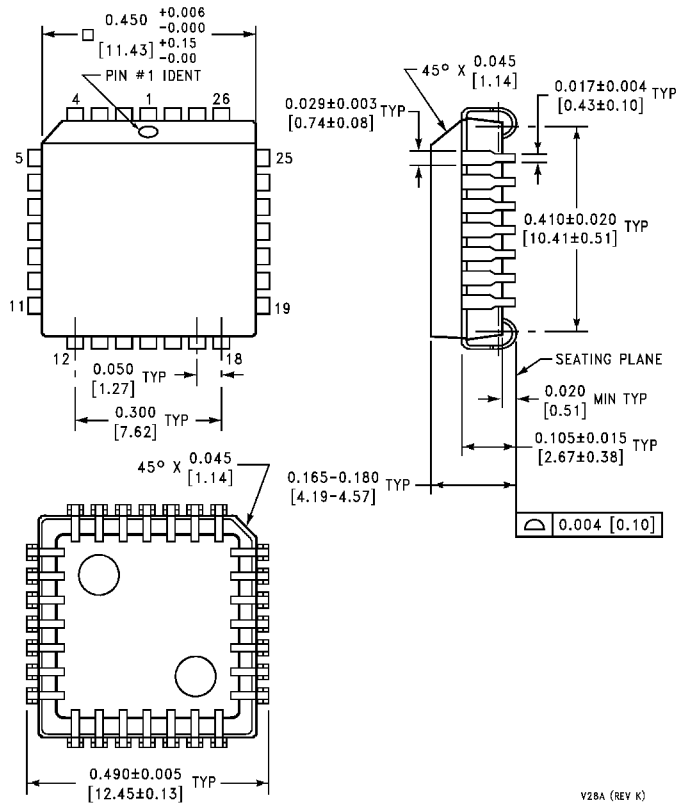
DS010549-9

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Ceramic Dual-In-Line Package (D)  
Package Number J24E**

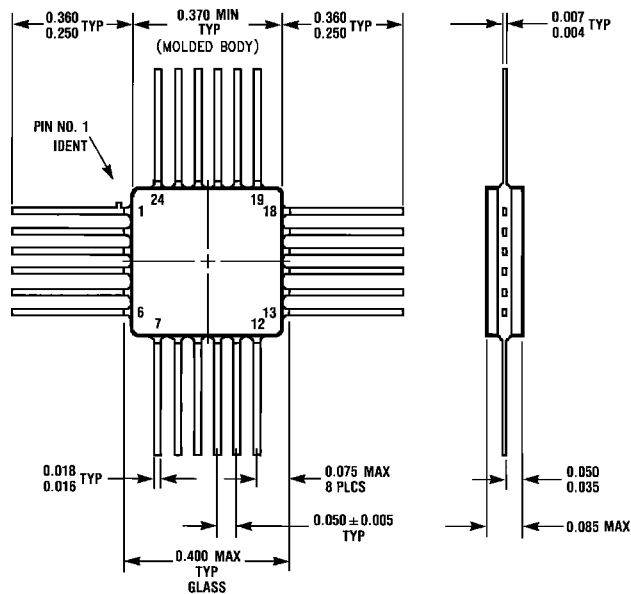
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Chip Carrier (Q)**  
**Package Number V28A**

V28A (REV K)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24B (REV D)

**24-Lead Ceramic Flatpak (F)  
NS Package Number W24B**

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation  
Americas  
Customer Response Center  
Tel: 1-888-522-5372

Fairchild Semiconductor Europe  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 8 141-35-0  
English Tel: +44 (0) 1 793-85-68-56  
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: +852 2737-7200  
Fax: +852 2314-0061

National Semiconductor Japan Ltd.  
Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179

www.fairchildsemi.com