800 MHz, 50 mW Current Feedback Amplifier

AD8001

FEATURES

Excellent Video Specifications (R_L = 150 Ω, G = +2)
- Gain Flatness 0.1 dB to 100 MHz
- 0.01% Differential Gain Error
- 0.025° Differential Phase Error

Low Power
- 5.5 mA Max Power Supply Current (55 mW)

High Speed and Fast Settling
- 880 MHz, –3 dB Bandwidth (G = +1)
- 440 MHz, –3 dB Bandwidth (G = +2)
- 1200 V/μs Slew Rate
- 10 ns Settling Time to 0.1%

Low Distortion
- –65 dBc THD, f_C = 5 MHz
- 33 dBm Third Order Intercept, F_1 = 10 MHz
- –66 dB SFDR, f = 5 MHz

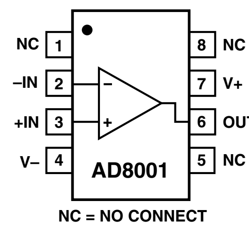
High Output Drive
- 70 mA Output Current
- Drives Up to 4 Back-Terminated Loads (75 Ω Each) While Maintaining Good Differential Gain/Phase Performance (0.05%/0.25°)

APPLICATIONS

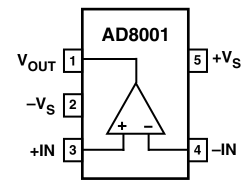
A-to-D Drivers
Video Line Drivers
Professional Cameras
Video Switchers
Special Effects
RF Receivers

FUNCTIONAL BLOCK DIAGRAMS

8-Lead PDIP (N-8), CERDIP (Q-8) and SOIC (R-8)



5-Lead SOT-23-5 (RT-5)



GENERAL DESCRIPTION

The AD8001 is a low power, high speed amplifier designed to operate on ±5 V supplies. The AD8001 features unique transimpedance linearization circuitry. This allows it to drive video loads with excellent differential gain and phase performance on only 50 mW of power. The AD8001 is a current feedback amplifier and features gain flatness of 0.1 dB to 100 MHz while offering differential gain and phase error of 0.01% and 0.025°. This makes the AD8001 ideal for professional video electronics such as cameras and video switchers. Additionally, the AD8001's low distortion and fast settling make it ideal for buffer high speed A-to-D converters.

The AD8001 offers low power of 5.5 mA max (V_S = ±5 V) and can run on a single +12 V power supply, while being capable of delivering over 70 mA of load current. These features make this amplifier ideal for portable and battery-powered applications where size and power are critical.

The outstanding bandwidth of 800 MHz along with 1200 V/μs of slew rate make the AD8001 useful in many general-purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 6 V to 12 V are needed. The AD8001 is available in the industrial temperature range of –40°C to +85°C.

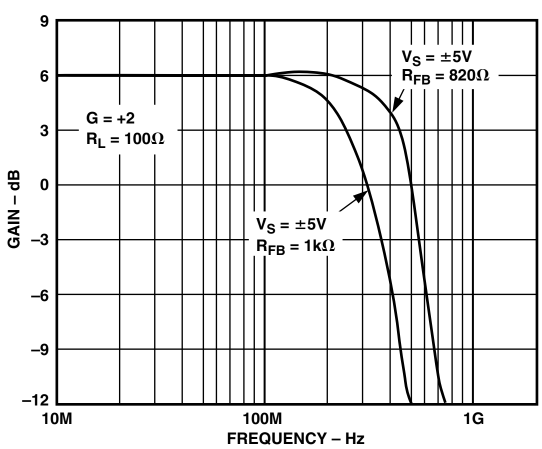


Figure 1. Frequency Response of AD8001

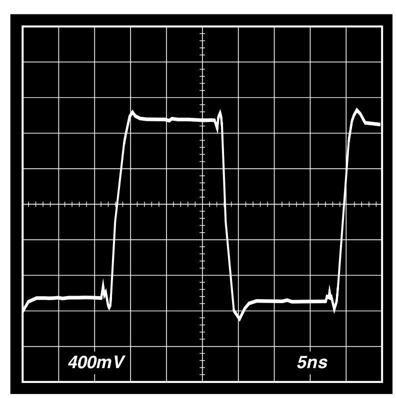


Figure 2. Transient Response of AD8001; 2 V Step, G = +2

REV. D

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AD8001–SPECIFICATIONS (@ T_A = + 25°C, V_S = ±5 V, R_L = 100 Ω, unless otherwise noted.)

Model		Conditions	AD8001A			Unit
			Min	Typ	Max	
DYNAMIC PERFORMANCE						
–3 dB Small Signal Bandwidth,	N Package	G = +2, < 0.1 dB Peaking, R_F = 750 Ω	350	440		MHz
		G = +1, < 1 dB Peaking, R_F = 1 kΩ	650	880		MHz
	R Package	G = +2, < 0.1 dB Peaking, R_F = 681 Ω	350	440		MHz
		G = +1, < 0.1 dB Peaking, R_F = 845 Ω	575	715		MHz
	RT Package	G = +2, < 0.1 dB Peaking, R_F = 768 Ω	300	380		MHz
		G = +1, < 0.1 dB Peaking, R_F = 1 kΩ	575	795		MHz
Bandwidth for 0.1 dB Flatness						
	N Package	G = +2, R_F = 750 Ω	85	110		MHz
	R Package	G = +2, R_F = 681 Ω	100	125		MHz
	RT Package	G = +2, R_F = 768 Ω	120	145		MHz
Slew Rate		G = +2, V_O = 2 V Step	800	1000		V/µs
		G = –1, V_O = 2 V Step	960	1200		V/µs
Settling Time to 0.1%		G = –1, V_O = 2 V Step		10		ns
Rise and Fall Time		G = +2, V_O = 2 V Step, R_F = 649 Ω		1.4		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion		f_C = 5 MHz, V_O = 2 V p-p		–65		dBc
		G = +2, R_L = 100 Ω				
Input Voltage Noise		f = 10 kHz		2.0		nV/√Hz
Input Current Noise		f = 10 kHz, +In		2.0		pA/√Hz
		–In		18		pA/√Hz
Differential Gain Error		NTSC, G = +2, R_L = 150 Ω		0.01	0.025	%
Differential Phase Error		NTSC, G = +2, R_L = 150 Ω		0.025	0.04	Degree
Third Order Intercept		f = 10 MHz		33		dBm
1 dB Gain Compression		f = 10 MHz		14		dBm
SFDR		f = 5 MHz		–66		dB
DC PERFORMANCE						
Input Offset Voltage				2.0	5.5	mV
		T_{MIN}–T_{MAX}		2.0	9.0	mV
Offset Drift				10		µV/°C
–Input Bias Current				5.0	25	±µA
		T_{MIN}–T_{MAX}			35	±µA
+Input Bias Current				3.0	6.0	±µA
		T_{MIN}–T_{MAX}			10	±µA
Open-Loop Transresistance		V_O = ±2.5 V	250	900		kΩ
		T_{MIN}–T_{MAX}	175			kΩ
INPUT CHARACTERISTICS						
Input Resistance		+Input		10		MΩ
		–Input		50		Ω
Input Capacitance		+Input		1.5		pF
Input Common-Mode Voltage Range				3.2		±V
Common-Mode Rejection Ratio						
Offset Voltage		V_{CM} = ±2.5 V	50	54		dB
–Input Current		V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.3	1.0	µA/V
+Input Current		V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.2	0.7	µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing		R_L = 150 Ω	2.7	3.1		±V
Output Current		R_L = 37.5 Ω	50	70		mA
Short Circuit Current			85	110		mA
POWER SUPPLY						
Operating Range			±3.0		±6.0	V
Quiescent Current		T_{MIN}–T_{MAX}		5.0	5.5	mA
Power Supply Rejection Ratio		$+V_S$ = +4 V to +6 V, $–V_S$ = –5 V	60	75		dB
		$–V_S$ = –4 V to –6 V, $+V_S$ = +5 V	50	56		dB
–Input Current		T_{MIN}–T_{MAX}		0.5	2.5	µA/V
+Input Current		T_{MIN}–T_{MAX}		0.1	0.5	µA/V

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . 12.6 V
Internal Power Dissipation @ 25°C[2]
PDIP Package (N) . . . . 1.3 W
SOIC (R) . . . . 0.8 W
8-Lead CERDIP . . . . 1.1 W
SOT-23-5 Package (RT) . . . . 0.5 W
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±1.2 V
Output Short Circuit Duration
. . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead PDIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W
8-Lead CERDIP Package: θ_{JA} = 110°C/W
5-Lead SOT-23-5 Package: θ_{JA} = 260°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8001 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8001 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

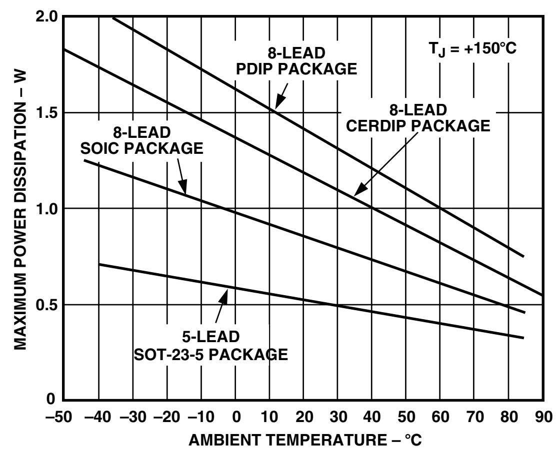


Figure 3. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

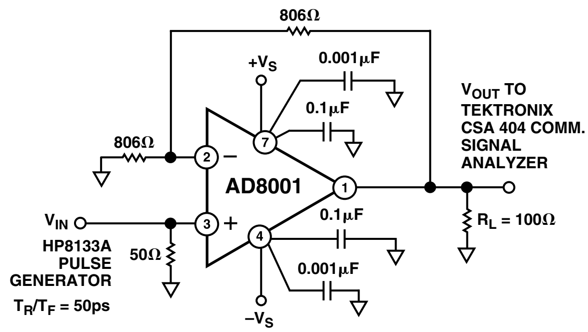
Model	Temperature Range	Package Description	Package Option	Branding
AD8001AN	–40°C to +85°C	8-Lead PDIP	N-8	
AD8001AQ	–55°C to +125°C	8-Lead CERDIP	Q-8	
AD8001AR	–40°C to +85°C	8-Lead SOIC	R-8	
AD8001AR-REEL	–40°C to +85°C	13" Tape and REEL	R-8	
AD8001AR-REEL7	–40°C to +85°C	7" Tape and REEL	R-8	
AD8001ART-REEL	–40°C to +85°C	13" Tape and REEL	RT-5	HEA
AD8001ART-REEL7	–40°C to +85°C	7" Tape and REEL	RT-5	HEA
AD8001ACHIPS	–40°C to +85°C	Die Form		
5962-9459301MPA*	–55°C to +125°C	8-Lead CERDIP	Q-8	

*Standard Military Drawing Device.

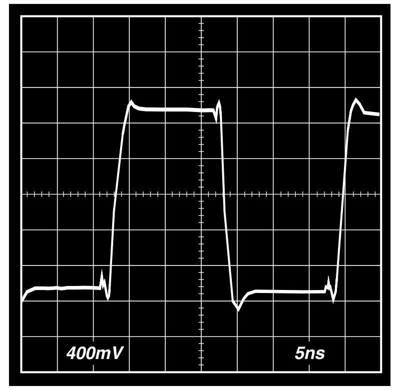
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8001 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

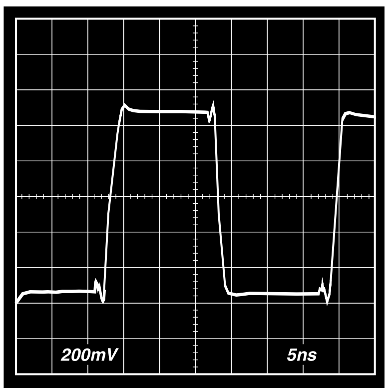
AD8001–Typical Performance Characteristics



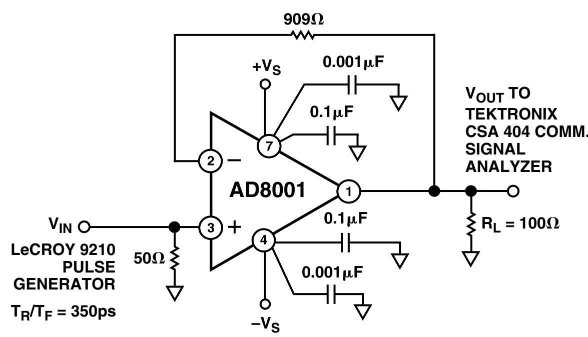
TPC 1. Test Circuit , Gain = +2



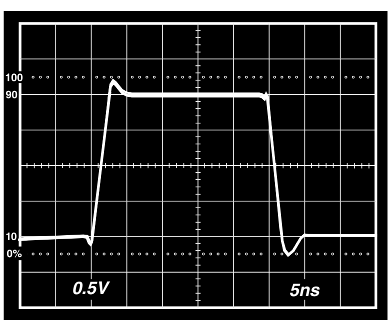
TPC 4. 2 V Step Response, G = +2



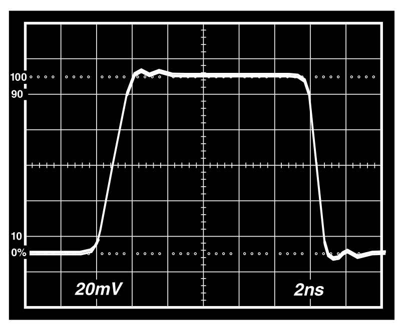
TPC 2. 1 V Step Response, G = +2



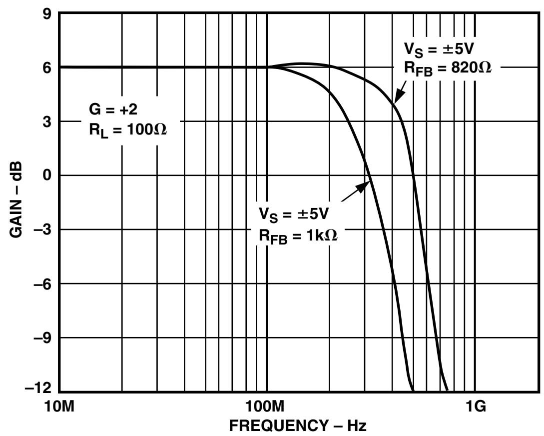
TPC 5. Test Circuit, Gain = +1



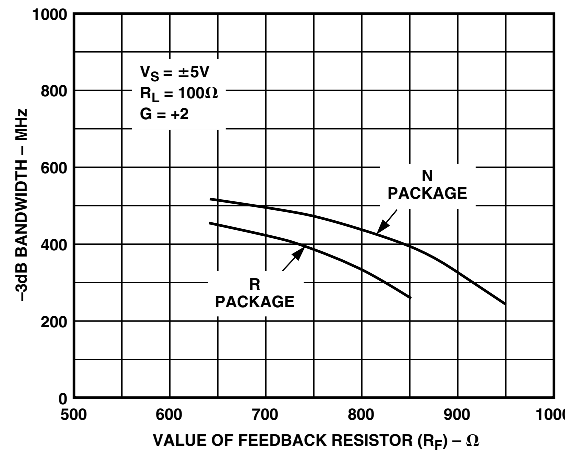
TPC 3. 2 V Step Response, G = +1



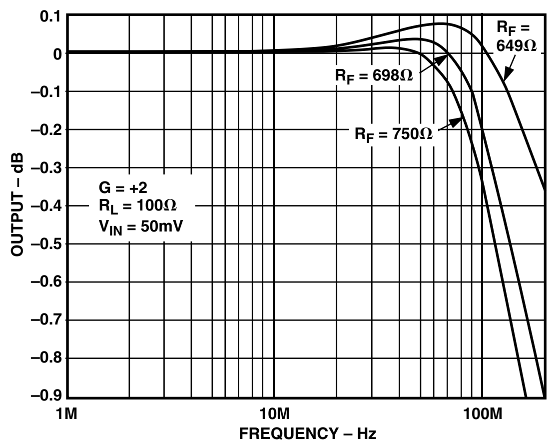
TPC 6. 100 mV Step Response, G = +1



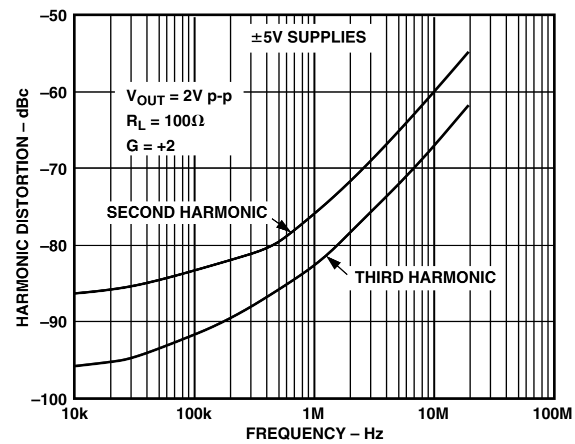
TPC 7. Frequency Response, G = +2



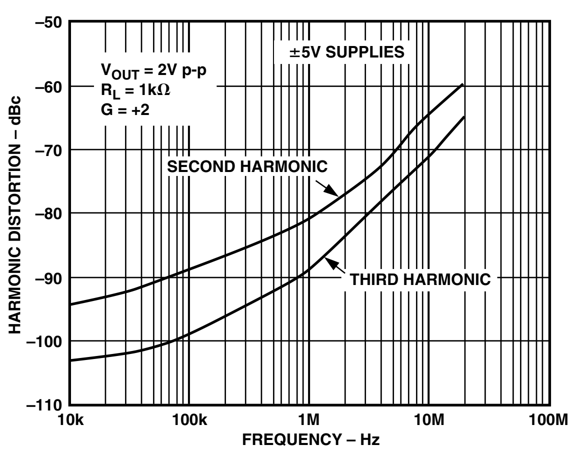
TPC 10. –3 dB Bandwidth vs. R_F



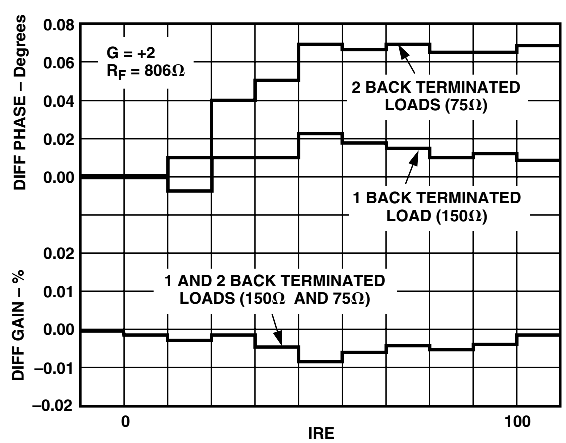
TPC 8. 0.1 dB Flatness, R Package (for N Package Add 50 Ω to R_F)



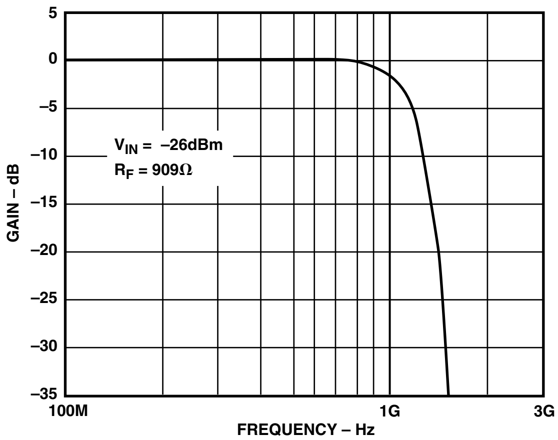
TPC 11. Distortion vs. Frequency, R_L = 100 Ω



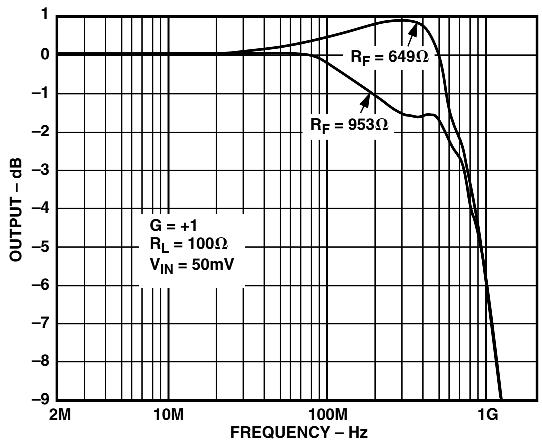
TPC 9. Distortion vs. Frequency, R_L = 1 kΩ



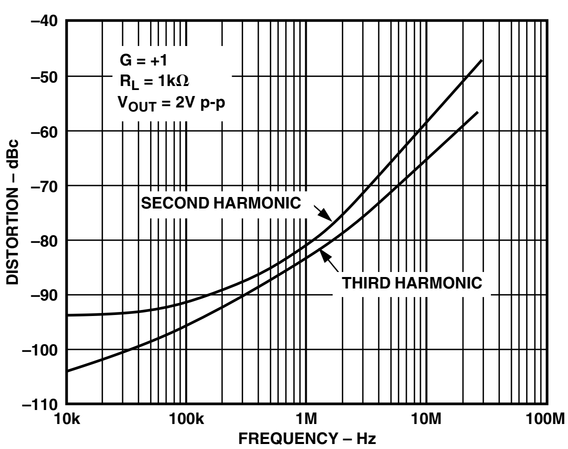
TPC 12. Differential Gain and Differential Phase



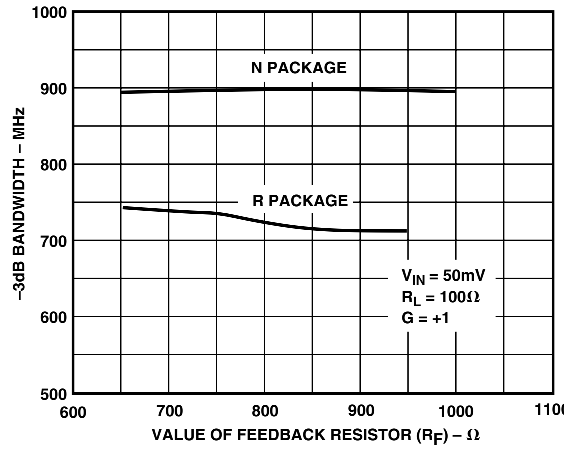
TPC 13. *Frequency Response, G = +1*



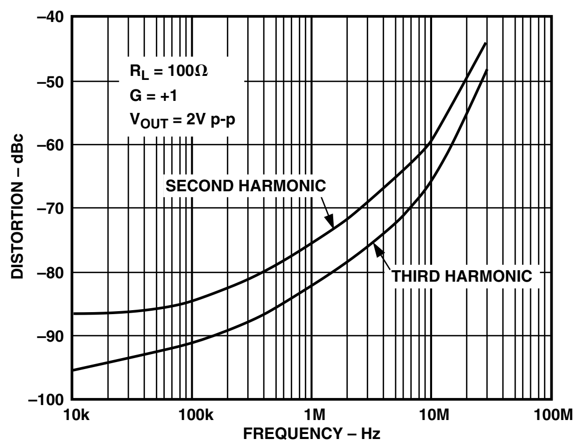
TPC 14. *Flatness, R Package, G = +1 (for N Package Add 100 Ω to* R_F*)*



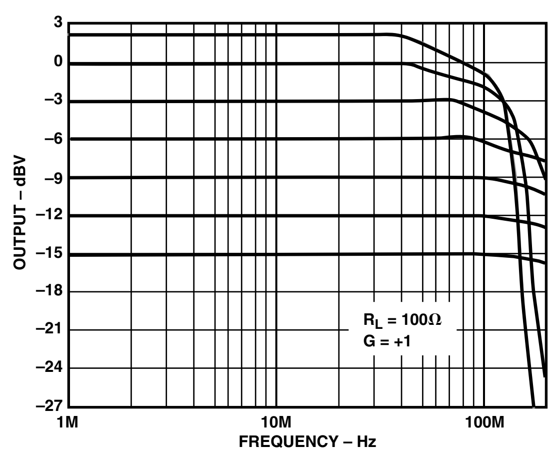
TPC 15. *Distortion vs. Frequency,* R_L *= 1 kΩ*



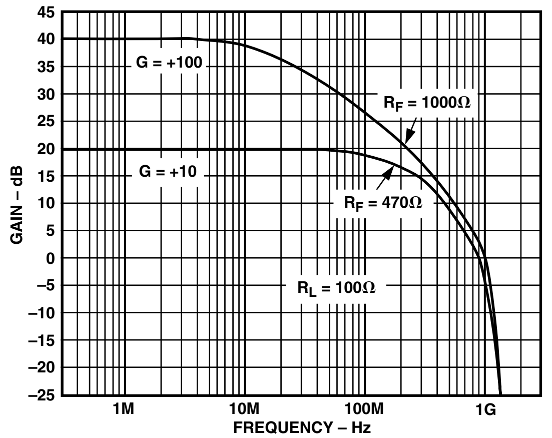
TPC 16. *–3 dB Bandwidth vs.* R_F*, G = +1*



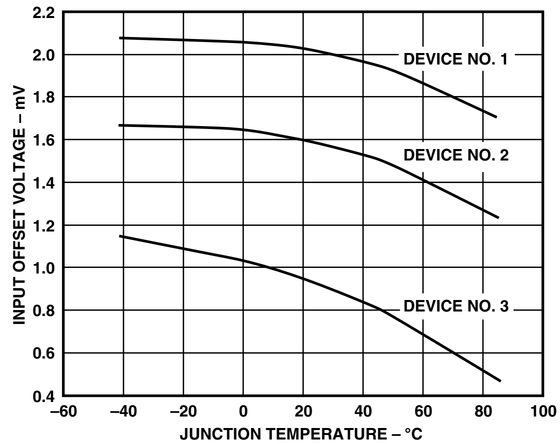
TPC 17. *Distortion vs. Frequency,* R_L *= 100 Ω*



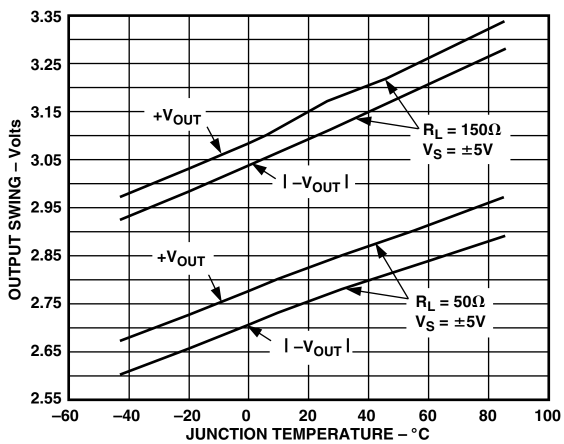
TPC 18. *Large Signal Frequency Response, G = +1*



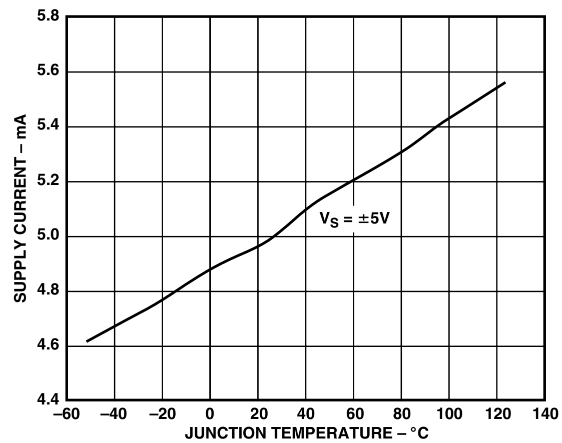
TPC 19. Frequency Response, G = +10, G = +100



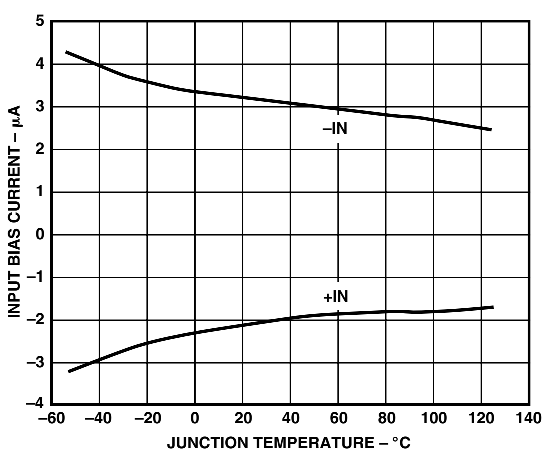
TPC 22. Input Offset vs. Temperature



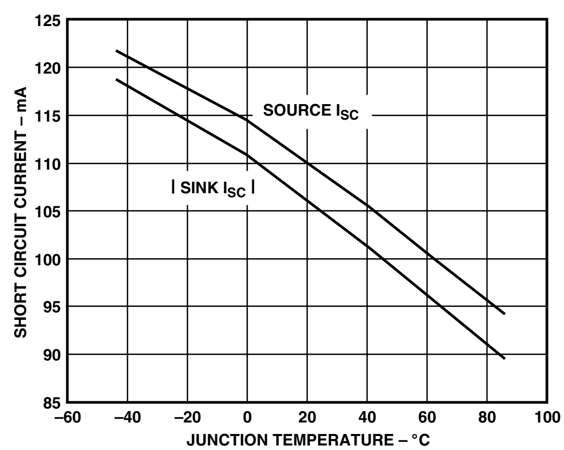
TPC 20. Output Swing vs. Temperature



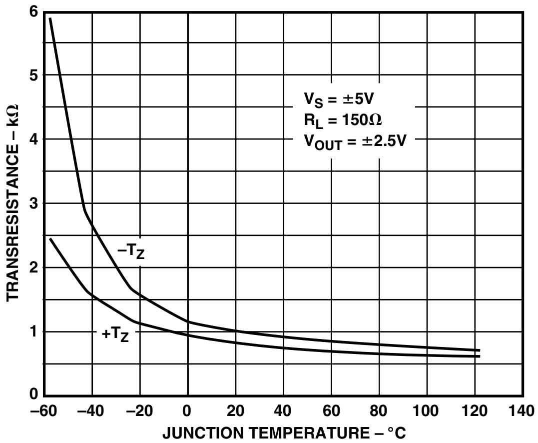
TPC 23. Supply Current vs. Temperature



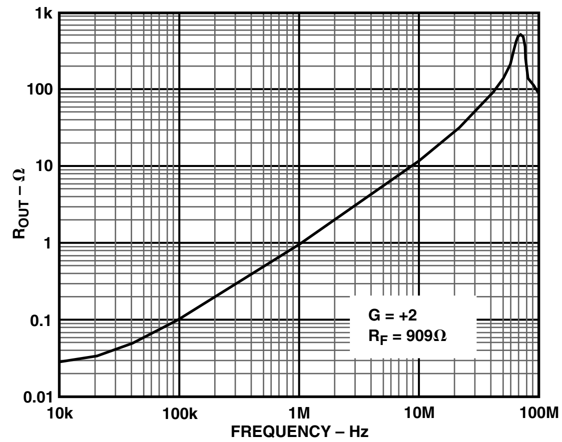
TPC 21. Input Bias Current vs. Temperature



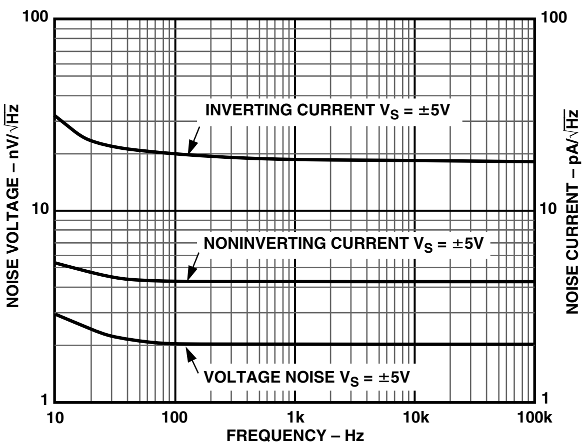
TPC 24. Short Circuit Current vs. Temperature



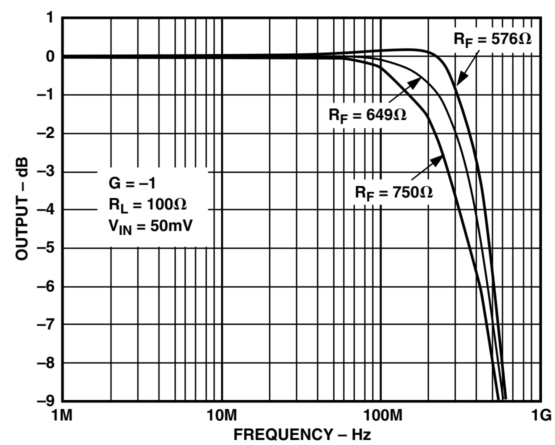
TPC 25. Transresistance vs. Temperature



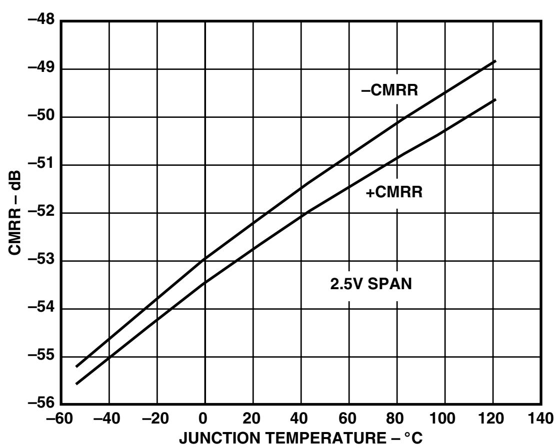
TPC 28. Output Resistance vs. Frequency



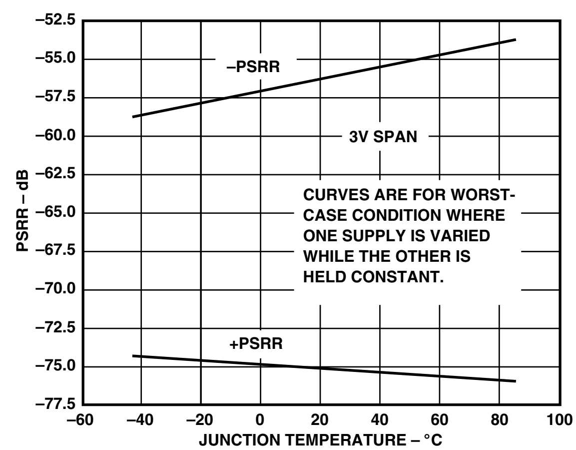
TPC 26. Noise vs. Frequency



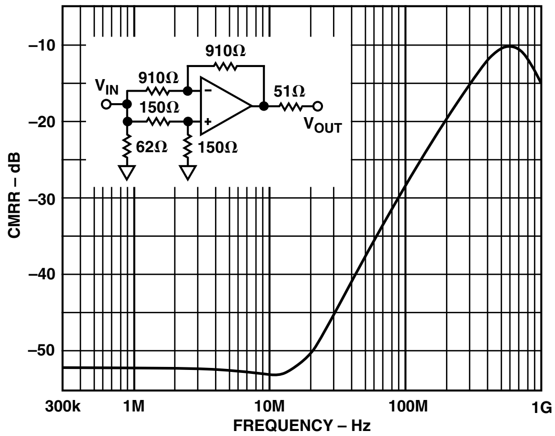
TPC 29. –3 dB Bandwidth vs. Frequency, G = –1



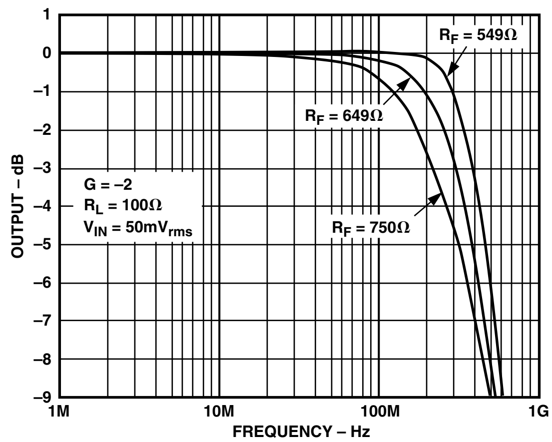
TPC 27. CMRR vs. Temperature



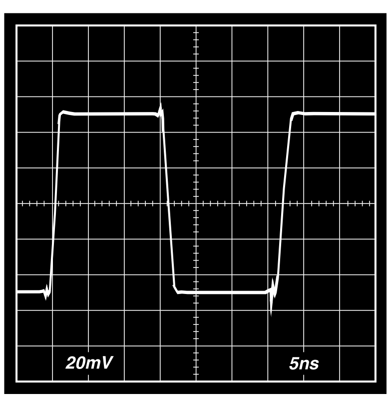
TPC 30. PSRR vs. Temperature



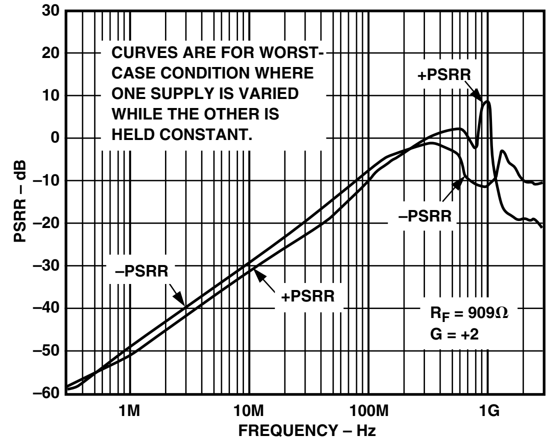
TPC 31. CMRR vs. Frequency



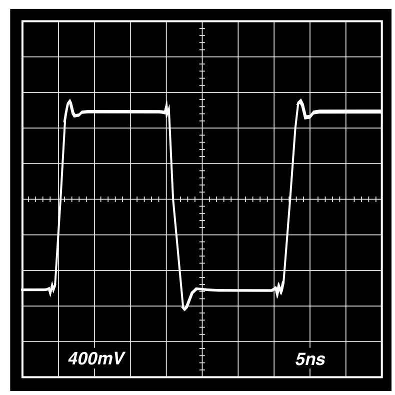
TPC 32. –3 dB Bandwidth vs. Frequency, G = –2



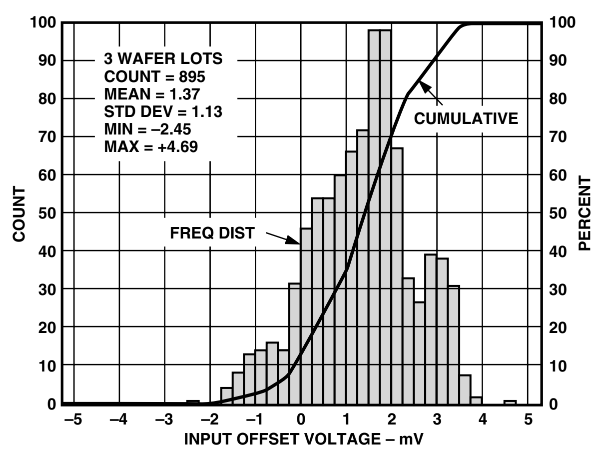
TPC 33. 100 mV Step Response, G = –1



TPC 34. PSRR vs. Frequency



TPC 35. 2 V Step Response, G = –1



TPC 36. Input Offset Voltage Distribution

THEORY OF OPERATION

A very simple analysis can put the operation of the AD8001, a current feedback amplifier, in familiar terms. Being a current feedback amplifier, the AD8001's open-loop behavior is expressed as transimpedance, $\Delta V_O/\Delta I_{IN}$, or T_Z. The open-loop transimpedance behaves just as the open-loop voltage gain of a voltage feedback amplifier, that is, it has a large dc value and decreases at roughly 6 dB/octave in frequency.

Since the R_{IN} is proportional to $1/g_M$, the equivalent voltage gain is just $T_Z \times g_M$, where the g_M in question is the transconductance of the input stage. This results in a low open-loop input impedance at the inverting input, a now familiar result. Using this amplifier as a follower with gain, Figure 4, basic analysis yields the following result.

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z\ (S)}{T_Z\ (S) + G \times R_{IN} + R1}$$

$$G = 1 + \frac{R1}{R2} \qquad R_{IN} = 1/g_M \approx 50\ \Omega$$

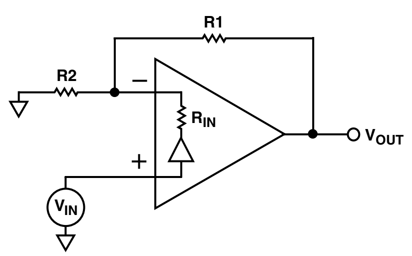


Figure 4. Follower with Gain

Recognizing that $G \times R_{IN} << R1$ for low gains, it can be seen to the first order that bandwidth for this amplifier is independent of gain (G). This simple analysis in conjunction with Figure 5 can, in fact, predict the behavior of the AD8001 over a wide range of conditions.

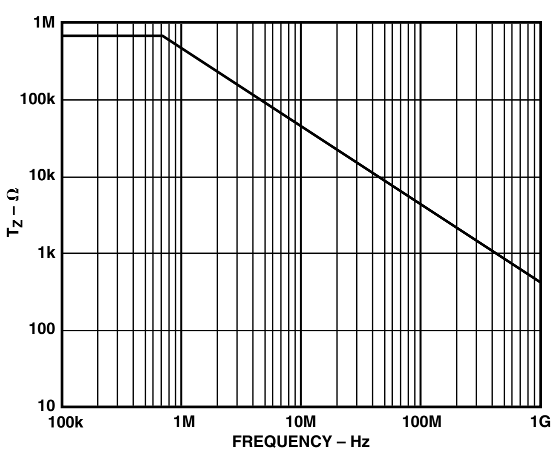


Figure 5. Transimpedance vs. Frequency

Considering that additional poles contribute excess phase at high frequencies, there is a minimum feedback resistance below which peaking or oscillation may result. This fact is used to determine the optimum feedback resistance, R_F. In practice, parasitic capacitance at Pin 2 will also add phase in the feedback loop, so picking an optimum value for R_F can be difficult. Figure 6 illustrates this problem. Here the fine scale (0.1 dB/div) flatness is plotted versus feedback resistance. These plots were taken using an evaluation card which is available to customers so that these results may readily be duplicated.

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

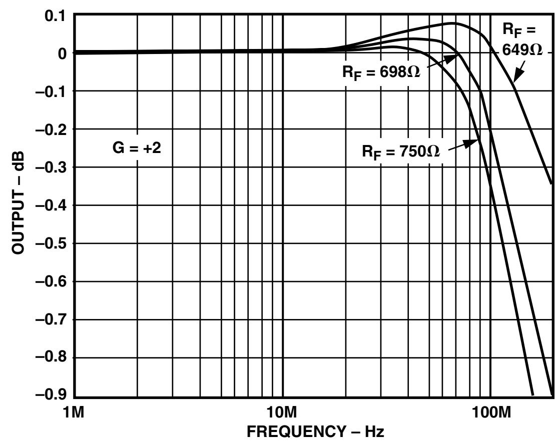


Figure 6. 0.1 dB Flatness vs. Frequency

Choice of Feedback and Gain Resistors

Because of the above-mentioned relationship between the bandwidth and feedback resistor, the fine scale gain flatness will, to some extent, vary with feedback resistance. It, therefore, is recommended that once optimum resistor values have been determined, 1% tolerance values should be used if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface-mount resistors were used for the bulk of the characterization for this data sheet. It is not recommended that leaded components be used with the AD8001.

Printed Circuit Board Layout Considerations

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed-loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, a space (5 mm min) should be left around the signal lines to minimize coupling. Additionally, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths on the order of less than 5 mm are recommended. If long runs of coaxial cable are being driven, dispersion and loss must be considered.

Power Supply Bypassing

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. A parallel combination of 4.7 μF and 0.1 μF is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

DC Errors and Noise

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors, refer to the equation below. For noise error the terms are root-sum-squared to give a net output error. In the circuit in Figure 7 they are input offset (V_{IO}), which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_I$), noninverting input current ($I_{BN} \times R_N$) also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_I and subsequently multiplied by the noise gain always appears at the output as $I_{BN} \times R_F$. The input voltage noise of the AD8001 is a low 2 nV/$\sqrt{\text{Hz}}$. At low gains though the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to better offset and drift specifications for the AD8001 compared to many other current feedback amplifiers. The typical performance curves in conjunction with the following equations can be used to predict the performance of the AD8001 in any application.

$$V_{OUT} = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BN} \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BI} \times R_F$$

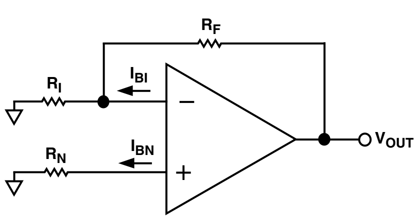


Figure 7. Output Offset Voltage

Driving Capacitive Loads

The AD8001 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, best frequency response is obtained by the addition of a small series resistance, as shown in Figure 8. The accompanying graph shows the optimum value for R_{SERIES} versus capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

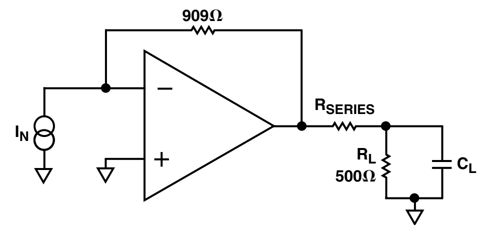


Figure 8. Driving Capacitive Loads

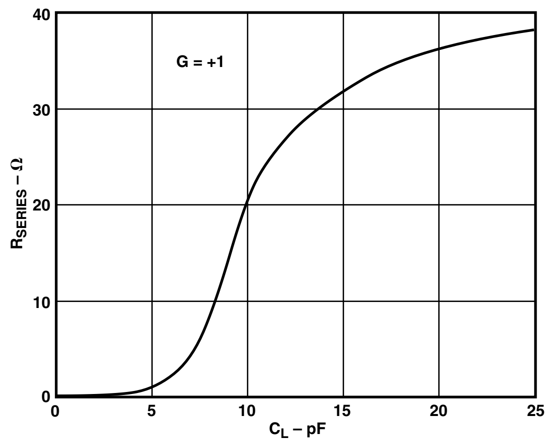


Figure 9. Recommended R_{SERIES} vs. Capacitive Load

Communications

Distortion is a key specification in communications applications. Intermodulation distortion (IMD) is a measure of the ability of an amplifier to pass complex signals without the generation of spurious harmonics. The third order products are usually the most problematic since several of them fall near the fundamentals and do not lend themselves to filtering. Theory predicts that the third order harmonic distortion components increase in power at three times the rate of the fundamental tones. The specification of third order intercept as the virtual point where fundamental and harmonic power are equal is one standard measure of distortion performance. Op amps used in closed-loop applications do not always obey this simple theory. At a gain of +2, the AD8001 has performance summarized in Figure 10. Here the worst third order products are plotted versus input power. The third order intercept of the AD8001 is +33 dBm at 10 MHz.

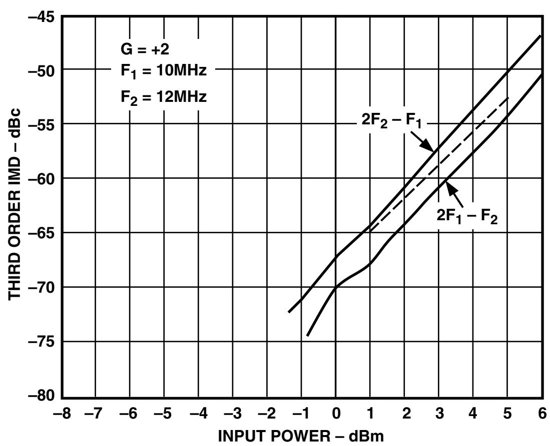


Figure 10. Third Order IMD; F_1 = 10 MHz, F_2 = 12 MHz

Operation as a Video Line Driver

The AD8001 has been designed to offer outstanding performance as a video line driver. The important specifications of differential gain (0.01%) and differential phase (0.025°) meet the most exacting HDTV demands for driving one video load. The AD8001 also drives up to two back terminated loads as shown in Figure 11, with equally impressive performance (0.01%, 0.07°). Another important consideration is isolation between loads in a multiple load application. The AD8001 has more than 40 dB of isolation at 5 MHz when driving two 75 Ω back terminated loads.

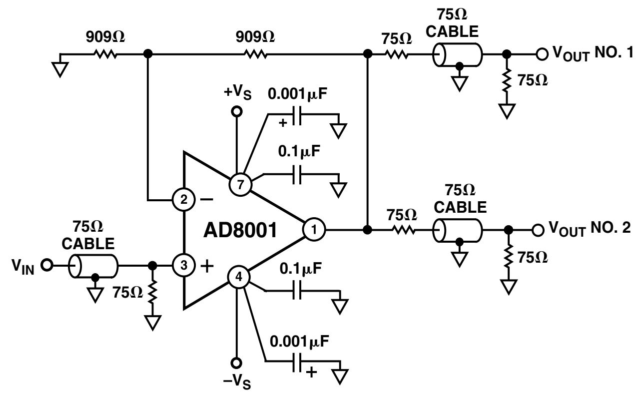


Figure 11. Video Line Driver

Driving A-to-D Converters

The AD8001 is well suited for driving high speed analog-to-digital converters such as the AD9058. The AD9058 is a dual 8-bit 50 MSPS ADC. In the circuit below, the AD8001 is shown driving the inputs of the AD9058, which are configured for 0 V to 2 V ranges. Bipolar input signals are buffered, amplified (–2×), and offset (by +1.0 V) into the proper input range of the ADC. Using the AD9058's internal +2 V reference connected to both ADCs as shown in Figure 12 reduces the number of external components required to create a complete data acquisition system. The 20 Ω resistors in series with ADC inputs are used to help the AD8001s drive the 10 pF ADC input capacitance. The AD8001 only adds 100 mW to the power consumption while not limiting the performance of the circuit.

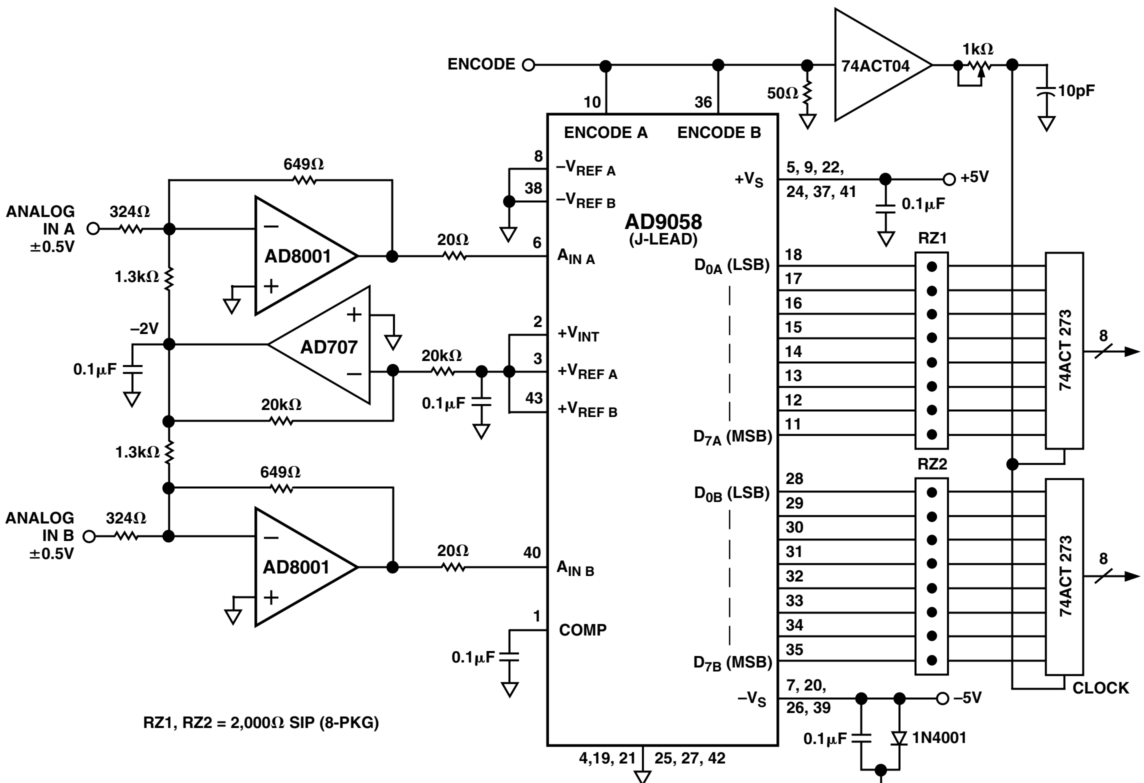


Figure 12. AD8001 Driving a Dual A-to-D Converter

Layout Considerations

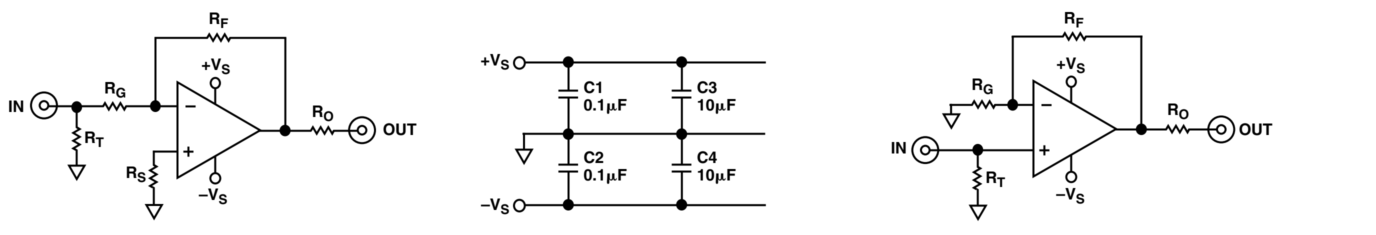
The specified high speed performance of the AD8001 requires careful attention to board layout and component selection. Proper R_F design techniques and low parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing (see Figure 13). One end should be connected to the ground plane and the other within 1/8 inch of each power pin. An additional large (4.7 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large-signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.



Inverting Configuration *Supply Bypassing* *Noninverting Configuration*

Figure 13. Inverting and Noninverting Configurations for Evaluation Boards

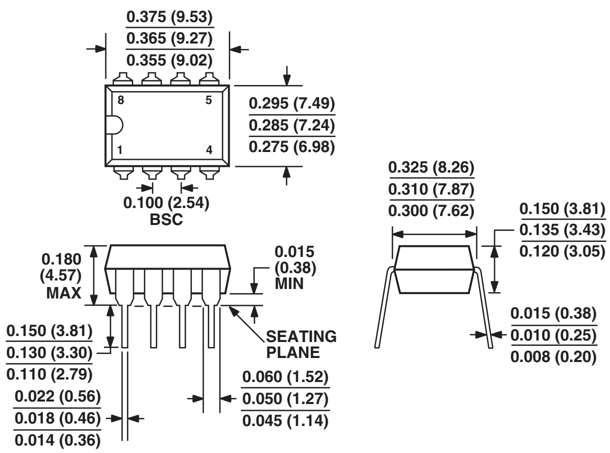
Table I. Recommended Component Values

	AD8001AN (PDIP) Gain					AD8001AR (SOIC) Gain					AD8001ART (SOT-23-5) Gain				
Component	**–1**	**+1**	**+2**	**+10**	**+100**	**–1**	**+1**	**+2**	**+10**	**+100**	**–1**	**+1**	**+2**	**+10**	**+100**
R_F (Ω)	649	1050	750	470	1000	604	953	681	470	1000	845	1000	768	470	1000
R_G (Ω)	649		750	51	10	604		681	51	10	845		768	51	10
R_O (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_S (Ω)	0					0					0				
R_T (Nominal) (Ω)	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	340	880	460	260	20	370	710	440	260	20	240	795	380	260	20
0.1 dB Flatness (MHz)	105	70	105			130	100	120			110	300	145		

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP] (N-8)

Dimensions shown in inches and (millimeters)

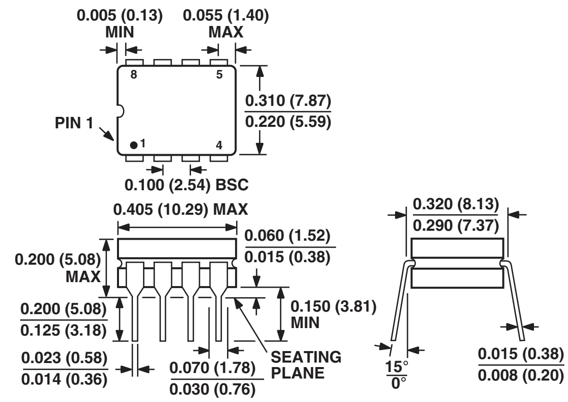


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)

Dimensions shown in inches and (millimeters)



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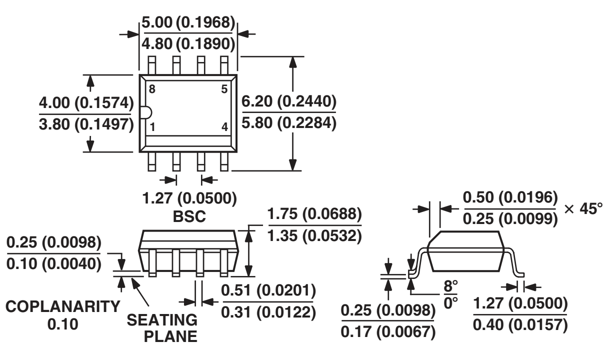
8-Lead Standard Small Outline Package [SOIC] (R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA

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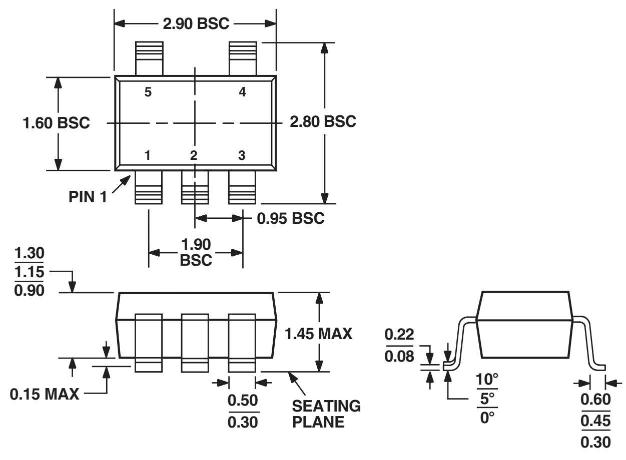
5-Lead Small Outline Transistor Package [SOT-23] (RT-5)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178AA

Revision History

Location	Page
7/03—Data Sheet changed from REV. C to REV. D	
Renumbered figures and TPCs	Universal
Changes to ORDERING GUIDE	3
Updated OUTLINE DIMENSIONS	15

C01043–0–7/03(D)