CY28330

Clock Generator for AMD™ Hammer

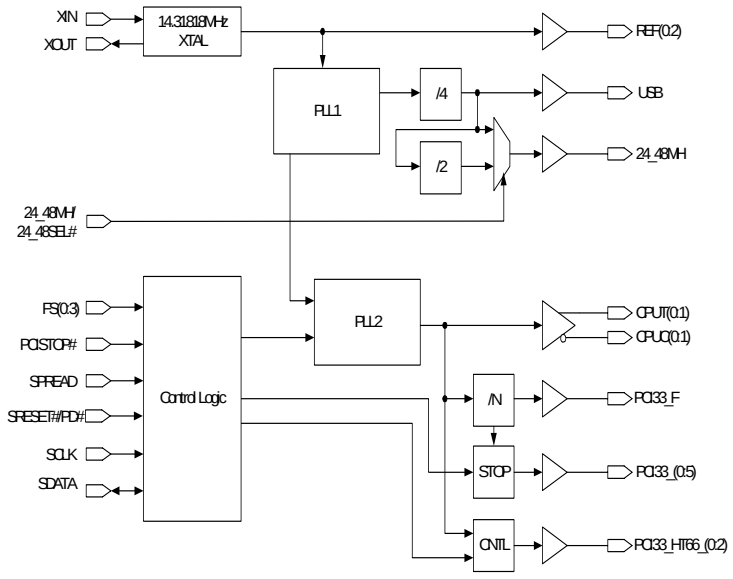
Features

- **Supports AMD™ Hammer CPU**
- **2 differential Pair of CPU Clocks**
- **6 Low Skew/Jitter PCI Clocks**
- **1 Free-running PCI Clock**
- **3 Low Skew/Jitter AGP/HT Clocks**
- **148M Output for USB**
- **1 programmable 24M or 48M for FDC**
- **3 REF 14.318MHz Clocks**
- **Dial-a-Frequency™ Programmability**
- **Cypress Spread Spectrum for Best EMI Reduction**
- **SMBus Register Programmable Options**
- **5V Tolerance SCLK and SDATA Lines**
- **3.3V Operation**
- **Power Management Control Pins**
- **48 Pin SSOP Package**

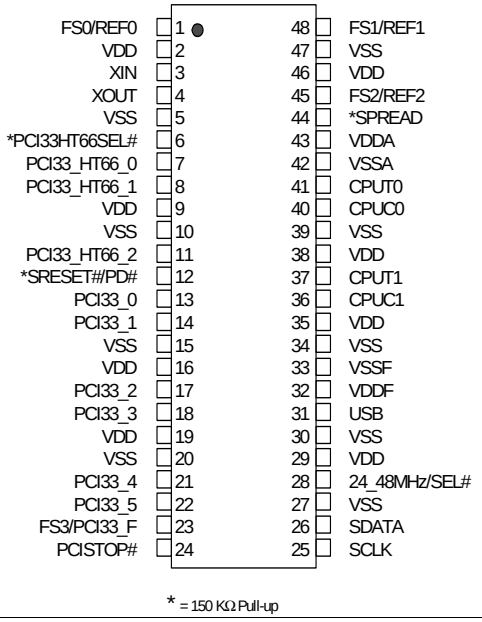
Table 1. Frequency Table (MHz)[1]

FS (3:0)	CPU	PCI_HT SEL	PCI_HT	PCI	VC0	CPU Div	PCI_HT Div	PCI Div
0000	Hi-Z	X	Hi-Z	Hi-Z				
0001	XIN	0	XIN/3	XIN/6				
0001	XIN	1	XIN/6	XIN/6				
0010	100.0	0/1	66.7/33.3	33.31	200	2	3/6	6
0011	100.0	0/1	66.7/33.3	33.31	200	2	3/6	6
0100	100.0	0/1	66.7/33.3	33.31	200	2	3/6	6
0101	133.3	0/1	66.7/33.3	33.31	266.6	2	4/8	8
0110	166.7	0/1	66.7/33.3	33.31	333.3	2	5/10	10
0111	200.0	0/1	66.7/33.3	33.31	400.0	2	6/12	12
1000	105.0	0/1	70.0/35.0	35.00	210.0	2	3/6	6
1001	110.0	0/1	73.3/36.7	36.67	220.0	2	3/6	6
1010	115.0	0/1	76.7/38.3	38.33	230.0	2	3/6	6
1011	120.0	0/1	60.0/30.0	30.00	240.0	2	4/8	8
1100	140.0	0/1	70.0/35.0	35.00	280.0	2	4/8	8
1101	150.0	0/1	60.0/30.0	30.00	300.0	2	5/10	10
1110	160.0	0/1	64.0/32.0	32.00	320.0	2	5/10	10
1111	180.0	0/1	60.0/30.0	30.00	360.0	2	6/12	12

Block Diagram



Pin Configuration



* = 150 KΩ Pull-up

Note:
1. All outputs except XOUT will be three-stated when FS(3:0) = 0000.

Pin Description

Pin	Name	PWR	I/O	Description
3	XIN	VDD	I	**Oscillator Buffer Input**. Connect to a crystal or to an external clock.
4	XOUT	VDD	O	**Oscillator Buffer Output**. Connect to a crystal. Do not connect when an external clock is applied at XIN.
41, 37	CPUT(0:1)	VDDC	O	**CPU clock outputs 0 and 1**: push-pull "true" output of differential pair.
40, 36	CPUC(0:1)	VDDC	O	**CPU clock outputs 0 and 1**: push-pull "compliment" output of differential pair.
23	PCI33_F	VDD	O	**3.3V free-running PCI clock output**.
13, 14, 17, 18, 21, 22	PCI33(0:5)	VDD	O	**3.3V PCI clock outputs controlled by PCISTOP#**.
7, 8, 11	PCI33_HT66(0:2)	VDD	O	**3.3V PCI 33MHz or HyperTransport™ 66 clock outputs**. This group is selectable between 33 MHz and 66 MHz based upon the state of the PCI33HT66SEL#.
6	PCI33_HT66SEL#	VDD	I PU	**This input selects the output frequency of PCI33_HT66 outputs to either 33 MHz or 66 MHz**. There is an internal 150K ohm pull-up resistor. This pin will be externally strapped low using a 10Kohm resistor to VSS. 0 = 66 MHz, 1 = 33 MHz.
31	USB	VDDF	O	**3.3V USB clock output at 48 MHz**.
28	24_48/SEL#	VDDF	I/O PU	**3.3v Super I/O clock output**. At power up this pin is sensed to determine whether the output is 24 MHz or 48 MHz. There is an internal 150K ohm pull-up resistor. This pin will be externally strapped low using a 10K ohm resistor to VSS. 0 = 48 MHz, 1 = 24 MHz.
1, 48, 45	REF(0:2)/FS(0:2)	VDD	I/O PU	**3.3V Reference clock output**. At power up this pin is sensed to determine the CPU output frequency. There is an internal 150K ohm pull-up resistor. These pins will be externally strapped low using a 10K ohm resistor to VSS. See *Table 1*.
44	SPREAD	VDD	I PU	**Spread Spectrum clock enable**. At power up this pin is sensed to determine whether spread spectrum clocking in enabled on all output except the USB and 24_48/SEL#. There is an internal 150K ohm pull-up resistor. This pin will be externally strapped low using a 10K ohm resistor to VSS. 0=disable, 1=enable.
24	PCISTOP#	VDD	I PU	**Control for PCI33(0:5) and PCI33_HT66(0:2) outputs**. Active LOW control input to halt all 33MHz PCI clocks except PCI33_F. Only the PCI33_HT66 outputs that are running at 33MHz will be stopped. The outputs will be glitch free when turning off and turning on. There is an internal 150K ohm pull-up resistor.
12	SRESET#	VDD	O	**SRESET output from Watchdog timer**. Active low.
	PD#	VDD	I PU	**Power-down input**. 1 = running, 0 = Power Down. There is an internal 150K ohm pull-up resistor.
26	SDATA	VDD	I/O	**Data pin for SMBus (rev2.0)**.
25	SCLK	VDD	I	**Clock pin for SMBus (rev2.0)**.
2, 9, 16, 19, 29, 35, 38, 46	VDD		PWR	**Power connection to 3.3V for the core**.
5, 10, 15, 20, 27, 30, 34, 39, 47	VSS		GND	**Power connection to GROUND for the CORE section of the chip**.
43	VDDA		PWR	**Power connection to 3.3V for the ANALOG section of the chip**.
42	VSSA		GND	**Power connection to GROUND for the ANALOG section of the chip**.
32	VDDF		PWR	**Power connection to 3.3V for the 48-MHz PLL section of the chip**.
33	VSSF		GND	**Power connection to GROUND for the 48-MHz PLL section of the chip**.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled.

The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operation from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol.

The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be ’0000000’

Table 3. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit ’00000000’ stands for block operation	11:18	Command Code - 8 Bit ’00000000’ stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count from master - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 from master- 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 from master - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data bytes from master/Acknowledge	39:46	Data byte 0 from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte 1 from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Serial Control Registers

Byte 0: Frequency and Spread Spectrum Control Register

Bit	@Pup	Description
7	Inactive = 0	Write Disable (write once). A 1 written to this bit after a 1 has been written to Byte0 bit0 will permanently disable modification of all configuration registers until the part has been powered off. Once the clock generator has been Write Disabled, the SMBus controller should still accept and acknowledge subsequent write cycles but it should not modify any of the registers.
6	Inactive = 0	Spread Spectrum enable (0=disable, 1=enable). This bit provides a SW programmable control for spread spectrum clocking. See *Table 5*. The readback version of this bit is the hardware strapped value such that the SW has the ability to know each state, either by readback or by writing the SSE bit.
5	0	ATPG Mode. 0 = disable, 1 = enable. See Byte 8, bit 7.
4	FS3 pin	FS(3) (corresponds to Frequency Selection. See *Table 1*.
3	FS2 pin	FS(2) (corresponds to Frequency Selection. See *Table 1*.
2	FS1 pin	FS(1) (corresponds to Frequency Selection. See *Table 1*.
1	FS0 pin	FS(0) (corresponds to Frequency Selection. See *Table 1*.
0	Inactive = 0	Write Enable. A 1 written to this bit after power up will enable modification of all configuration registers and subsequent 0's written to this bit will disable modification of all configuration except this single bit. Note that block write transactions to the interface will complete, however unless the interface has been previously un-locked, the writes will have no effect. The effect of writing this bit does not take effect until the subsequent block write command.

Table 5. Spread Spectrum Enable

Pin 44	B0b6	Spread Enable
0	0	Off
0	1	On
1	0	On
1	1	On

Byte 1: PCI Clock Control Register

Bit	@Pup	Pin#	Name	Test Condition
7	1	8	PCI33_HT66_1	enable (1=Enabled, 0=Disabled)
6	1	7	PCI33_HT66_0	enable (1=Enabled, 0=Disabled)
5	1	22	PCI33_5	enable (1=Enabled, 0=Disabled)
4	1	21	PCI33_4	enable (1=Enabled, 0=Disabled)
3	1	18	PCI33_3	enable (1=Enabled, 0=Disabled)
2	1	17	PCI33_2	enable (1=Enabled, 0=Disabled)
1	1	14	PCI33_1	enable (1=Enabled, 0=Disabled)
0	1	13	PCI33_0	enable (1=Enabled, 0=Disabled)

Byte 2: PCI Clock, USB, 24_48MHz, REF(0:2) Control Register

Bit	@Pup	Test Condition
7	active = 1	CPUT/C(1) shutdown. This bit can be optionally used to disable the CPUT/C(1) clock pair. During shutdown, CPUT=low and CPUC=high
6	active = 1	CPUT/C(0) shutdown. This bit can be optionally used to disable the CPUT/C(0) clock pair. During shutdown, CPUT=low and CPUC=high
5	active = 1	REF(2) enable (1=Enabled, 0=Disabled)
4	active = 1	REF(1) enable (1=Enabled, 0=Disabled)
3	active = 1	REF(0) enable (1=Enabled, 0=Disabled)
2	active = 1	24_48MHz enable (1=Enabled, 0=Disabled)
1	active = 1	USB enable (1=Enabled, 0=Disabled)
0	active = 1	PCI33_HT66(2) enable (1=Enabled, 0=Disabled)

Byte 3: PCI Clock Free Running Select Control Register

Bit	@Pup	Description
7	0	PCI33 drive strength. 0 = normal, 1 = high.
6	0	PCI33_HT66 drive strength. 0 = normal, 1 = high.
5	Inactive = 0	PCI(5) free running enable (1=Free running, 0=Disabled)
4	Inactive = 0	PCI(4) free running enable (1=Free running, 0=Disabled)
3	Inactive = 0	PCI(3) free running enable (1=Free running, 0=Disabled)
2	Inactive = 0	PCI(2) free running enable (1=Free running, 0=Disabled)
1	Inactive = 0	PCI(1) free running enable (1=Free running, 0=Disabled)
0	Inactive = 0	PCI(0) free running enable (1=Free running, 0=Disabled)

Byte 4: Pin Latched/Real Time State (and one free running control)

Bit	@Pup	Description
7	active = 1	PCI33_F output enable. This bit can be optional used to disable the PCI33_F output.
6	Pin 44	SPREAD pin state, not latched
5	Pin 28	24_48SEL# pin power up latched state
4	Pin 6	PCI33_HT66SEL# pin statement latched
3	Pin 45	FS(2) power up latched state
2	Pin 48	FS(1) power up latched state
1	Pin 1	FS(0) power up latched state
0	Pin 23	FS(3) power up latched state

Byte 5: Clock Vendor ID

Bit	@Pup	Description
7	1	Vendor ID, Cypress = 100
6	0	Vendor ID
5	0	Vendor ID
4	0	Device Revision ID
3	0	Device Revision ID
2	0	Device Revision ID
1	0	Device Revision ID
0	0	Device Revision ID

Byte 6: SSCG, Dial-a-Skew™ and Dial-a-Ratio™ Register

Bit	@Pup	Description
7	0	SS_MODE; 0 = down spread, 1 = center spread See *Table 6*.
6	0	SST1 Select spread percentage. See *Table 6*.
5	0	SST0 Select spread percentage. See *Table 6*.
4	1	Reserved PCI33_HT66(3) enable (1=Enabled, 0=Disabled) (only offered on our high end model)
3	0	DASAG1; Programming these b its allow shifting the skew of the HT66(0:2) signals relative to their default value. See *Table 7*.
2	0	DASAG0; Programming these bits allow shifting the skew of the HT66(0:2) signals relative to their default value. See *Table 7*.
1	0	DARAG1; Programming these bits allow shifting the ratio of the HT66(0:2) signals relative to their default value. See *Table 8*.
0	0	DARAG0; Programming these bits allow shifting the ratio of the HT(0:2) signals relative to their default value. See *Table 8*.

Table 6. Spread Spectrum Table

SS_Mode (B6b7)	SST1 (B6b6)	SST0 (B6b5)	% Spread
0	0	0	-1.5%
0	0	1	-1.0%
0	1	0	-0.7%
0	1	1	-0.5%
1	0	0	±0.75%
1	0	1	±0.5
1	1	0	±0.35%
1	1	1	± 0.25%

Table 7. Dial-a-Skew CPU to HT66

DASAG(1:0)	HT66 Skew Shift
00	Default
01	-150 ps
10	+ 150ps
11	+ 300 ps

Table 8. Dial-a-Ratio CPU to HT66

DASAG(1:0)	CPU/HT66 Ratio
00	Frequency selection default
01	2/1
10	2.5/1
11	3/1

Byte 7: Watchdog Control Register

Bit	@Pup	Name	Description
7	0	Pin 12 Mode Select	SRESET#; 1 = Pin 12 is the input pin which functions as a PD# signal. 0 = Pin 12 is the output pin as SRESET# signal.
6	0	Frequency Reversion	This bit allows setting the Revert Frequency once the system is rebooted due to Watchdog time out only. 0 = selects frequency of existing H/W setting 1 = selects frequency of the second to last S/W setting. (the software setting prior to the one that caused a system reboot).
5	0		For Test, ALWAYS program to '0'
4	0	WD Time-out	This bit is set to "1" when the Watchdog times out. It is reset to "0" when the system clears the WD time stamps (WD3:0).
3	0	WD3	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 9*.
2	0	WD2	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 9*
1	0	WD1	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 9*.
0	0	WD0	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 9*.

Table 9. Watchdog Time Stamp

WD3	WD2	WD1	WD0	Function
0	0	0	0	Off
0	0	0	1	1 second
0	0	1	0	2 seconds
0	0	1	1	3 seconds
0	1	0	0	4 seconds
0	1	0	1	5 seconds
0	1	1	0	6 seconds
0	1	1	1	7 seconds
1	0	0	0	8 seconds
1	0	0	1	9 seconds
1	0	1	0	10 seconds
1	0	1	1	11 seconds
1	1	0	0	12 seconds
1	1	0	1	13 seconds
1	1	1	0	14 seconds
1	1	1	1	15 seconds

Byte 8: Dial-a-Frequency™ Control Register N

Bit	@PUp	Description
7	0	**ATPG Pulse**. A 0 to 1 transition on this bit will trigger a differential pulse on the CPUT/C lines whose pulse width is equal to the period of the currently latched frequency.
6	N6	**These bits are for programming the PLL's internal N register**. This access allows the user to modify the CPU frequency with great accuracy. All other synchronous clocks (clocks that are generated from the same PLL, such as PCI, remain at their existing ratios relative to the CPU clock.
5	N5	
4	N4	
3	N3	
2	N2	
1	N1	
0	N0	

Byte 9: Dial-a-Frequency™ Control Register M

Bit	@Pup	Description
7	0	CPU output skew; 0 = normal, 1 = -200ps Pin 41 to Pin 7
6	R5	These bits are for programming the PLL's internal R register. This access allows the user to modify the CPU frequency with great accuracy. All other synchronous clocks (clocks that are generated from the same PLL, such as PCI, remain at their existing ratios relative to the CPU clock.
5	R4	
4	R3	
3	R2	
2	R1	
1	R0	
0	0	When this bit = 1, it enables the Dial-a-Frequency N and R bits to be multiplexed into the internal N and R registers. When this bit = 0, the ROM based N and R values are loading into the internal N and R registers.

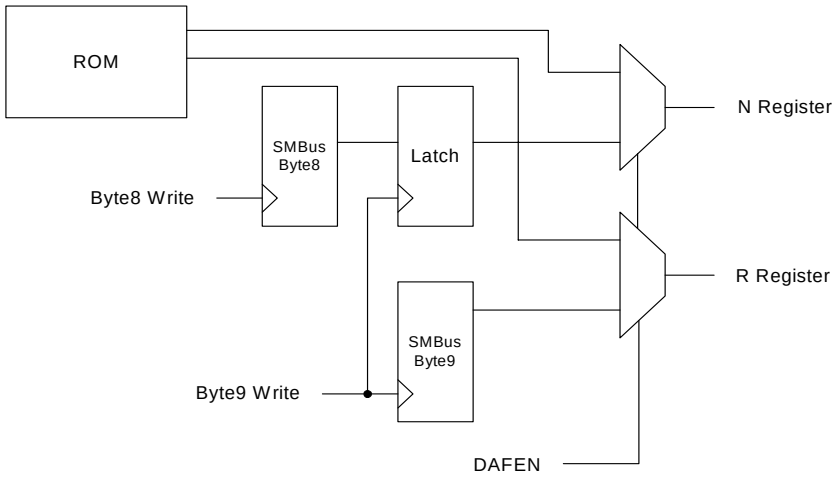


Figure 1. Dial-a-Frequency Register Loading

Dial-a-Frequency Feature

Dial-a-Frequency gives the designer direct access to the reference divider (M) and the feedback divider (N) of the internal Phase Lock Loop (PLL). The algorithm is the same for all P values, which is F_{cpu} = (P * N) / M with the following conditions. M = (20..56), N = (21..127) and N > M > N/2. 'P' is a large value constant that translates the output of the PLL into the CPU frequency. The Value of 'P' is relative to the latest frequency selected in the device prior to enabling the Dial-a-Frequency feature. Furthermore, P is an indication that the frequency ratios between the CPU, SDRAM, AGP (3V66), and PCI clock outputs remains unchanged when the Dial-a-Frequency feature is enabled.

Table 10.

FS(3:0)	P
XXXX	95995000

Operation

Pin strapping on any configuration pin is based on a 10K ohm resistor connected to either 3.3V (VDD) or ground (VSS). When the VDD supply goes above 2.0V, the Power-On-Reset circuitry latches all of the configuration bits into their respective registers and then allows the outputs to be enabled. The output may not occur immediately after this time as the PLL needs to be locked and will not output an invalid frequency. The CPU frequencies are defined from the hardware-sampled inputs. Additional frequencies and operating states can be selected through the SMBus programmable interface.

Spread spectrum modulation is required for all outputs derived from the internal CPU PLL2 (see *Block Diagram*). This include the CPU(0:1), PCI33(0:5), PCI33_F and PCI33_HT66(0:2). The REF (0:2), USB and 24_48 clocks are not affected by the spread spectrum modulation. The spread spectrum modulation is set for both center and down modes using linear and Lexmark profiles for amounts of 0.5% and 1.0% at a 33KHz rate.

The CPU clock driver is of a push-pull type for the differential outputs, instead of the AMD Athlon™ open-drain style. The CPU clock termination has been derived such that a 15-40 ohm, 3.3V output driver can be used for the CPU clock.

The PCISTOP# signal provides for synchronous control over the any output, except the PCI33_F, that is running at 33MHz. If the PCI33_HT66 outputs are configured to run at 66MHz will not be stopped by this signal. The PCISTOP# signal is sampled by an internal PCI clock such that once it is sensed low or active, the 33MHz signals are stopped on the next high to low transition such that there is always a valid high signal.

Absolute Maximum Rating

Parameter	Description	Rating	Unit
VDD, VDDA, VDDF	Supply voltage	–0.5 to 3.8	V
VIN1, VIN2	Input voltage	–0.5 to 3.8	V
TSTG	Storage temperature	–65 to +150	°C
ESDprotection	Input ESD (HBN)	> 2,000	V

Operating Condition[2]

Parameter	Description	Min.	Typ.	Max.	Unit
VDD, VDDA, VDDF	Supply voltage	3.135	3.3	3.465	V
TA	Operating temperature, Ambient	0		70	°C
Finput	Input frequency (crystal or reference)	10	14.318	16	MHz

SCLK and SDATA Input Electrical Characteristics (5V tolerant)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VIL	Supply voltage		VSS-0.3		0.8	V
VIH	Input voltage		2.0		VDD+0.3	V
IIL, IIH	Input high/low current	0<VIN<VDD			±µ5	µA
VOL	Output high voltage	IOL=1.75mA	VSS-0.3		0.4	V
IOL	Output low voltage	VO=0.8V	2		6	mA

DC Parameters (All outputs loaded)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VIL	Input Low Voltage	See Note 3	VSS-0.3		0.8	V
VIH	Input High Voltage		2.0		VDD+0.3	V
IIL	Input Low Current (@VIL = VSS)	For internal Pull up resistors, *See Note 4*			-50	µA
IIH	Input High Current (@VIH =VDD)				50	µA
Ioz	Three-State leakage Current				10	µA
Idd3.3V	Dynamic Supply Current	CPU(0:1) @ 200MHz		250		mA
Ipd3.3V	Power Down Supply Current				2	mA
Cin	Input pin capacitance				5	pF
Cout	Output pin capacitance				6	pF
Lpin	Pin inductance				7	nH
Cxtal	Crystal pin capacitance	Measured from Pin to Ground.	27	36	45	pF
V_{BIAS}	Crystal DC Bias Voltage		0.3Vdd	Vdd/2	0.7Vdd	V
Txs	Crystal Startup time	From Stable 3.3V power supply.			40	µs

Notes:

2. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Applicable to input signals: SPREAD, PCISTOP#, 24–48/Sel#.
4. Internal Pull-up and Pull-down resistors have a typical value of 250Ω.

AC Parameter

Parameter	Description	Test Condition	PCI133_HT66 = 66MHz			Unit
			Min.	Typ.	Max.	
TR	Output Rise Edge Rate	Measured @ the Hammer test load using VOCM±400mV, 0.850V to 1.650V	2		7	V/ns
TF	Output Fall Edge Rate	Measured @ the Hammer test load using VOCM ±400mV, 1.650V to 0.850V	2		7	V/ns
VDIFF	Differential Voltage	Measured @ the Hammer test load (single ended)	0.4	1.25	2.3	V
DVDIFF	Change in VDIFF_DC Magnitude	Measured @ the Hammer test load (single ended)	-150		150	mV
VCM	Common Mode Voltage	Measured @ the Hammer test load (single ended)	1.05	1.25	1.45	V
∆VCM	Change in VCM	Measured @ the Hammer test load (single ended)	-200		200	mV
TD	Duty Cycle	Measured at VOX	45	50	53	%
TJC	Jitter, Cycle to Cycle	Measured at VOX	0	100	200	ps
TJA	Jitter, Accumulated	Measured at VOX	-1000		1000	ps
TJSC_OP	Spectral Content Noise near Hammer frequency		TBD		TBD	dB
TJSC_DC	Spectral Content Noise from 0-200MHz	Noise floor measured with Spread Spectrum on between 0 MHz and 200 MHz. Measured with a 3.3V PECL differential buffer in line with CPU clock output	TBD		TBD	dB
TFS	Frequency Stabilization from Power-up	Measure from full supply voltage	0		3	ms
RON	Output Impedance	Average value during switching transition.	15	35	55	W

Table 11. PCI/Hyper Transport Clock Outputs

Parameter	Description	Conditions	PCI33, PCI33_HT = 33 MHz			PCI33_HT = 66 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
VOL	Output Low Voltage	IOL = 9.0mA	-		0.4			0.4	V
VOH	Output High Voltage	IOH =-12.0mA	2.4			2.4		-	V
IOL	Output Low Current	VO = 0.8V	10			10		-	mA
IOH	Output High Current	VO = 2.0V			-15			-15	mA
F	Frequency Actual			33.33			66.67		MHz
TR	Output Rise Edge Rate	Measured from 20% to 60%	1		4	1		4	V/ns
TF	Output Fall Edge Rate	Measured from 60% to 20%	1		4	1		4	V/ns
TD	Duty Cycle	Measured at 1.5V	45		55	45		55	%
TJC	Jitter, Cycle-to-Cycle	Measured at 1.5V	0		250	0		250	ps
TJA	Jitter Accumulated	Measured at 1.5V	-1000		1000	-1000		1000	ps
TFS	Frequency Stabilization from Power-up	Measure from full supply voltage	0		3			3	ms
RON	Output Impedance	Average value during switching transition.	12	15	55	12	15	55	W

Table 12. REF(0:2) Clock Outputs

Parameter	Description	Test Condition	PCI133_HT66 = 66 MHz			Unit
			Min.	Typ.	Max.	
VOL	Output Low Voltage	IOL = 9.0 mA			0.4	V
VOH	Output High Voltage	IOH = -12.0 mA	2.4			V
IOL	Output Low Current	VO = 0.8V	16			mA
IOH	Output High Current	VO = 2.0V			-22	mA
F	Frequency, Actual			14.318		MHz
TR	Output Rise Edge Rate	Measured from 20% to 60%	0.5		2	V/ns
TF	Output Fall Edge Rate	Measured from 60% to 20%	0.5		2	V/ns
TD	Duty Cycle	Measured at 1.5V	45		55	%
TJC	Jitter, Cycle-to-Cycle	Measured at 1.5V	0	500	1000	ps
TJA	Jitter, Accumulated	Measured at 1.5V	-1000		1000	ps
TFS	Frequency Stabilization from Power-up	Measure from full supply voltage	0		3	mS
RON	Output Impedance	Average value during switching transition.	20	24	60	W

Table 13. USB, 24_24 Clock Outputs

Parameter	Description	Conditions	PCI33, PCI33_HT = 33MHz			PCI33_HT = 66MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
VOL	Output Low Voltage	IOL = 9.0mA			0.4			0.4	V
VOH	Output High Voltage	IOH =-12.0mA	2.4			2.4			V
IOL	Output Low Current	VO = 0.8V	16			16			mA
IOH	Output High Current	VO = 2.0V			-22			-22	mA
F	Frequency Actual			24.004			48.008		MHz
TR	Output Rise Edge Rate	Measured from 20% to 80%	0.5		2	0.5		2	V/ns
TF	Output Fall Edge Rate	Measured from 80% to 20%	0.5		2	0.5		2	V/ns
TD	Duty Cycle	Measured at 1.5V	45		55	45		55	%
TJC	Jitter, Cycle-to-Cycle 24_48 MHz	Measured at 1.5V	0	250	500	0	250	500	ps
TJC	Jitter, Cycle-to-Cycle USB	Measured at 1.5V				0		100	ps
TJA	Jitter Accumulated	Measured at 1.5V	-1000		1000	-1000		1000	ps
TFS	Frequency Stabilization from Power-up	Measure from full supply voltage	0		3	0		3	ms
RON	Output Impedance	Average value during switching transition.	20	24	60	20	24	60	W

Table 14. Skew [5]

Parameter	Description	Conditions	Skew Window	Unit
TSK_CPU_CPU	CPU to CPU skew, time independent	Measured @ crossing points for CPUT rising edges1	250	ps
TSK_CPU_PCI33	CPU to PCI33 skew, time independent	Measured @ crossing points for CPUT rising edge and 1.5V PCI clocks	500	ps
TSK_PCI33_PCI33	PCI33 to PCI33 skew, time independent	Measured between rising @ 1.5V	500	ps

Note:

5. All skews in this skew budget are measured from the first referenced signal to the next. Therefore, this skew specifies the maximum SKEW WINDOW between these two signals to be 500ps whether the CPU crossing leads or lags the PCI clock. This should NOT be interpreted to mean that the PCI33 edge could either be 500ps before the CPU clock to 500ps after the clock, thus defining a 1000ps window in which the PCI33 clock edge could fall.

Table 14. Skew (continued)[5]

Parameter	Description	Conditions	Skew Window	Unit
TSK_PCI33_HT66	PCI33 to HT66 skew, time independent	Measured between rising @ 1.5V	500	ps
TSK_CPU_HT66	CPU to HT66 skew, time independent	Measured @ crossing points for CPUT rising edge and 1.5V for HyperTransport clocks	500	ps
TSK_HT66_HT66	HT66 to HT66 skew, time independent	Measured between rising @ 1.5V	500	ps
TSK_CPU_CPU	CPU to CPU skew, time variant	Measured @ crossing points for CPUT rising edges	200	ps
TSK_CPU_PCI33	CPU to PCI33 skew, time variant	Measured @ crossing points for CPUT rising edge and 1.5V PCI clocks	200	ps
TSK_PCI33_PCI33	PCI33 to PCI33 skew, time variant	Measured between rising @ 1.5V	200	ps
TSK_PCI33_HT66	PCI33 to HT66 skew, time variant	Measured between rising @ 1.5V	200	ps
TSK_CPU_HT66	CPU to HT66 skew, time variant	Measured @ crossing points for CPUT rising edge and 1.5V for HyperTransport clocks	200	ps
TSK_HT66_HT66	HT66 to HT66 skew, time variant	Measured between rising @ 1.5V	200	ps

Table 15. Loading Table

Clock Name	**Max Load** (in pF)[6]
CPU(0:1)	See *Figure 2*
USB 24_48, REF (0:2)	20
PC133(0:5), PC133_F, PCI33_HT66(0:2)	30

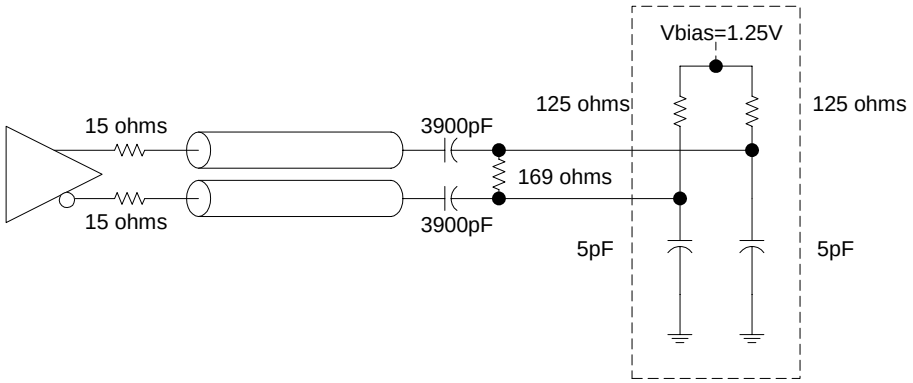


Figure 2. Test Load Configuration

Note:
6. The above loads are positioned near each output pin when tested.

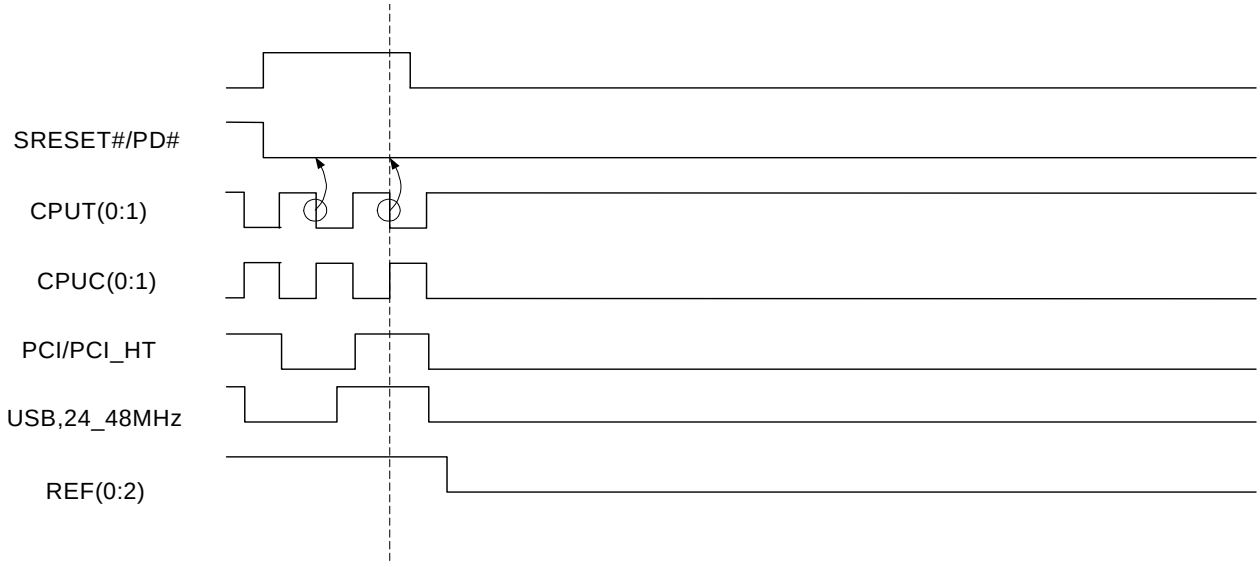


Figure 3. PD# Assertion Waveform

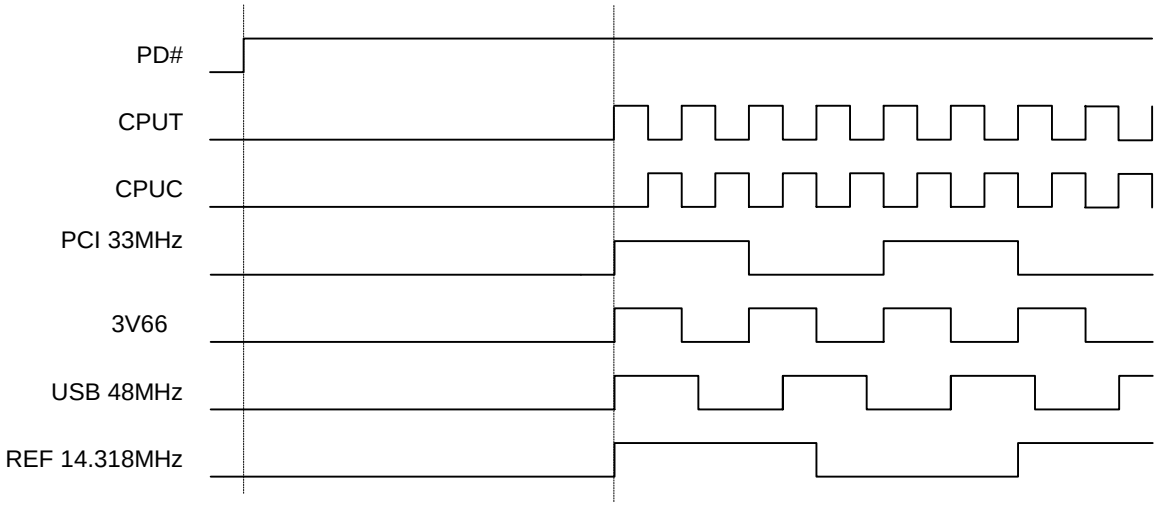


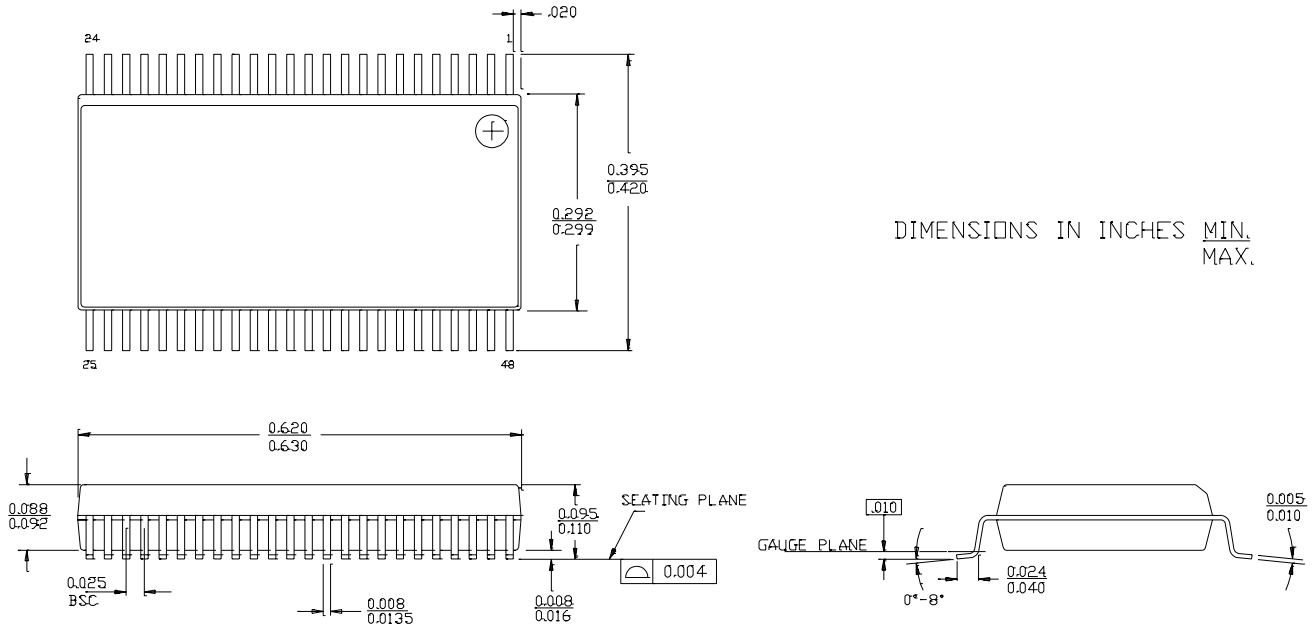
Figure 4. PD# Deassertion Waveform

Ordering Information

Part Number	Package Type	Product Flow
CY28330OC	48-pin SSOP	Commercial, 0° to 70°C
CY28330OCT	48-pin SSOP–Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-pin Shrunk Small Outline Package O48



Document Title:CY28330 Clock Generator for AMD™ Hammer Document #: 38-07366 Rev. *B				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112782	03/01/02	DMG	New Data Sheet
*A	114611	08/01/02	DMG	Added ATPG function on Byte0 bit 5 and Byte 8 bit 7 tables on pages 5 and 9, respectively
*B	122907	12/26/02	RBI	Add power up requirements to operating conditions requirements