ALLEGRO microsystems

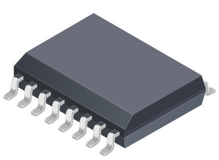
ACS732KMA and ACS733KMA

1 MHz Bandwidth, Galvanically Isolated Current Sensor IC in SOIC-16 Package

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- High bandwidth, 1 MHz analog output
- Differential Hall sensing rejects common-mode fields
- High-isolation SOIC16 wide body package provides galvanic isolation for high-voltage applications
- Industry-leading noise performance with greatly improved bandwidth through proprietary amplifier and filter design
- UL 60950-1 (ed. 2) and UL 62368 (ed. 1) certified
  - □ Dielectric Strength Voltage = 4.8 kV_{RMS}
  - □ Basic Isolation Working Voltage = 1097 V_{RMS}
  - □ Reinforced Isolation Working Voltage = 550 V_{RMS}
- Fast and externally configurable overcurrent fault detection
- 0.85 mΩ primary conductor resistance for low power loss and high inrush current withstand capability
- Options for 3.3 V and 5 V single supply operation
- Output voltage proportional to AC and DC current
- Factory-trimmed sensitivity and quiescent output voltage for improved accuracy
- Ratiometric output from supply voltage

PACKAGE: 16-Pin SOICW (suffix MA)



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CB Certificate Number:
US-32210-M3-UL
US-36315-UL

DESCRIPTION

The ACS732KMA and ACS733KMA are a new generation of high bandwidth current sensor ICs from Allegro™. These devices provide a compact, fast, and accurate solution for measuring high-frequency currents in DC/DC converters and other switching power applications. The ACS732 and ACS733 offer high isolation, high bandwidth Hall-effect-based current sensing with user-configurable overcurrent fault detection. These features make them ideally suited for high-frequency transformer and current transformer replacement in applications running at high voltages.

The ACS732 and ACS733 are suitable for all markets, including automotive, industrial, commercial, and communications systems. They may be used in motor control, load detection and management, switch-mode power supplies, and overcurrent fault protection applications.

The wide body SOIC-16 package allows for easy implementation. Applied current flowing through the copper conduction path generates a magnetic field that is sensed by the IC and converted to a proportional voltage. Current is sensed differentially in order to reject external common-mode fields. Device accuracy is optimized through the close proximity of the magnetic field to the Hall transducers. A precise, proportional voltage is provided by the Hall IC, which is factory-programmed after packaging for high accuracy. The fully integrated package has an internal copper conductive path with a typical resistance of 0.85 mΩ, providing low power loss.

The current-carrying pins (pins 1 through 8) are electrically isolated from the sensor leads (pins 9 through 16). This allows the devices to be used in high-side current sensing applications without the use of high-side differential amplifiers or other costly isolation techniques.

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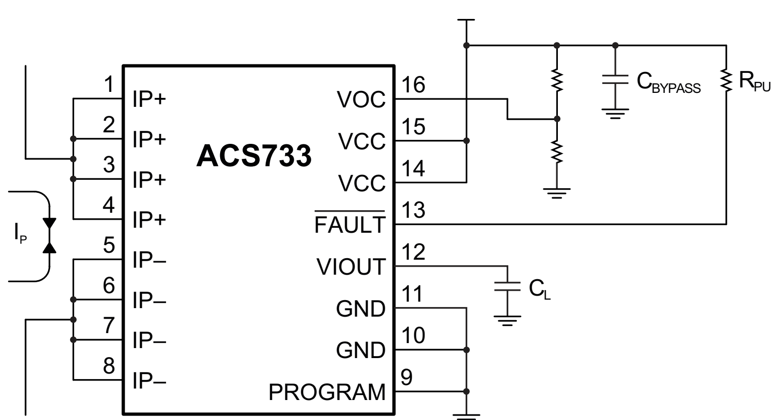

ACS732/ACS733 outputs an analog signal, V_{IOUT}, that changes proportionally with the bidirectional AC or DC primary sensed current, I_P, within the specified measurement range.

The overcurrent threshold may be set with a resistor divider tied to the V_{OC} pin.

Figure 1: Typical Application Circuit

DESCRIPTION (continued)

The ACS732 and ACS733 are provided in a small, low profile, surface-mount SOIC-16 wide-body package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is lead-free. These devices are fully calibrated prior to shipment from the Allegro factory.

SELECTION GUIDE

Part Number	Optimized Range, I_P (A)	Sensitivity [1], Sens(Typ) (mV/A)	Nominal Supply Voltage, V_{CC}, (V)	T_A (°C)	Packing [2]
ACS732KMATR-65AB-T	±65	30.77	5	–40 to 125	Tape and reel, 1000 pieces per reel
ACS732KMATR-75AB-T	±75	26.67	5		
ACS733KMATR-65AB-T	±65	20.3	3.3		

[1] Measured at Nominal Supply Voltage, V_{CC}.
[2] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Output Voltage	V_{IOUT}		6	V
Reverse Output Voltage	V_{RIOUT}		–0.1	V
Fault Output Voltage	V_{FAULT}		6	V
Reverse Fault Output Voltage	V_{RFAULT}		–0.1	V
Forward V_{OC} Voltage	V_{VOC}		6	V
Reverse V_{OC} Voltage	V_{RVOC}		–0.1	V
Output Current	I_{OUT}	Maximum survivable sink or source current on the output	15	mA
Maximum Continuous Current	I_{CMAX}	T_A = 25°C	60	A
Nominal Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

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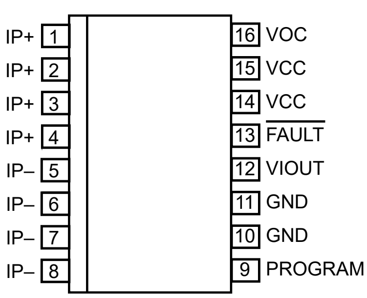
ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}	Per AEC-Q100	±12	kV
Charged Device Model	V_{CDM}	Per AEC-Q100	±1	kV

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage	V_{ISO}	Agency type-tested for 60 seconds per UL 60950-1 (edition 2) and UL 62368 (edition 1). Production tested at 3000 V_{RMS} for 1 second, in accordance with UL 60950-1 (edition 2) and UL 62368 (edition 1).	4800	V_{RMS}
Working Voltage for Basic Isolation	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 60950-1 (edition 2) and UL 62368 (edition 1).	1480	V_{PK}
			1047	V_{RMS} or V_{DC}
Working Voltage for Reinforced Isolation	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 60950-1 (edition 2) and UL 62368 (edition 1).	730	V_{PK}
			517	V_{RMS} or V_{DC}
Clearance	D_{cl}	Minimum distance through air from IP leads to signal leads.	7.5	mm
Creepage	D_{cr}	Minimum distance along package body from IP leads to signal leads	7.9	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	90	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package MA, 16-Pin SOICW Pinout Diagram

Terminal List Table

Number	Name	Description
1,2,3,4	IP+	Positive terminals for current being sensed; fused internally.
5,6,7,8	IP–	Negative terminals for current being sensed; fused internally.
9	PROGRAM	Programming input pin for factory calibration. Connect to ground for best ESD performance.
10, 11	GND	Device ground terminal.
12	VIOUT	Analog output signal.
13	$\overline{\text{FAULT}}$	Overcurrent Fault output. Open drain.
14, 15	VCC	Device power supply terminal.
16	VOC	Set the overcurrent fault threshold via external resistor divider on this pin.

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FUNCTIONAL BLOCK DIAGRAM

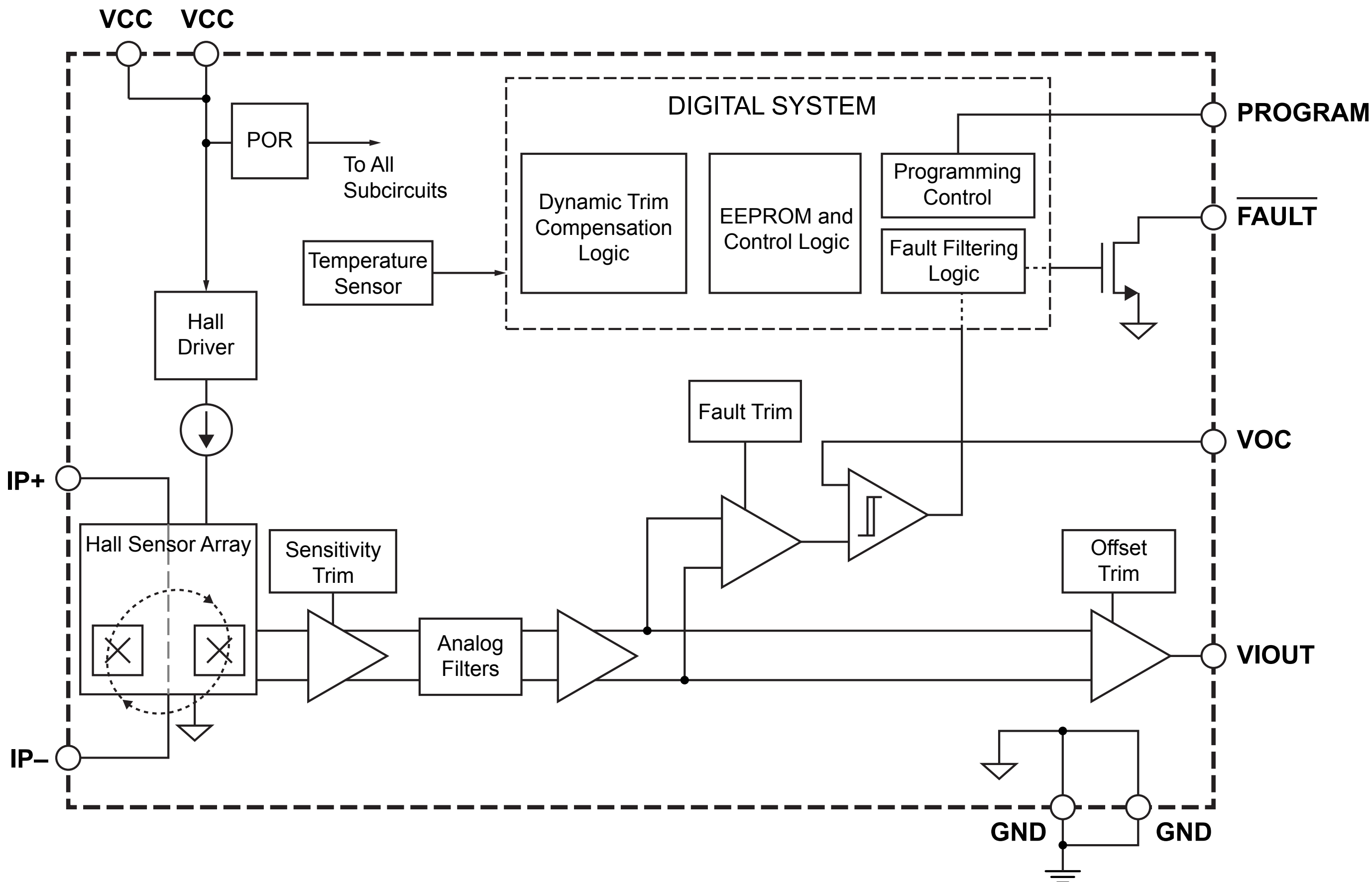

Figure 2: Functional Block Diagram

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COMMON ELECTRICAL CHARACTERISTICS: Over full range of T_A, over supply voltage range $V_{CC(MIN)}$ through $V_{CC(MAX)}$ of a sensor variant, C_{BYPASS} = 0.1 µF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
Supply Voltage	V_{CC}	ACS732	4.75	5.0	5.25	V
		ACS733	3.14	3.3	3.46	V
Supply Current	I_{CC}	ACS732; V_{CC} = 5.0 V	–	24	35	mA
		ACS733; V_{CC} = 3.3 V	–	20	35	mA
Bypass Capacitor [2]	C_{BYPASS}	V_{CC} to GND	0.1	–	–	µF
Output Capacitance Load	C_L	V_{IOUT} to GND	–	–	220	pF
Output Resistive Load	R_L	V_{IOUT} to GND	50	–	–	kΩ
Output Saturation Voltage	$V_{SAT(HIGH)}$	V_{CC} = 5.0 V, T_A = 25°C, $R_{L(PULLDOWN)}$ = 50 kΩ to GND	V_{CC} – 0.3	–	–	V
		V_{CC} = 3.3 V, T_A = 25°C, $R_{L(PULLDOWN)}$ = 50 kΩ to GND	V_{CC} – 0.3	–	–	V
	$V_{SAT(LOW)}$	V_{CC} = 5.0 V, T_A = 25°C, $R_{L(PULLDOWN)}$ = 50 kΩ to VCC	–	–	0.5	V
		V_{CC} = 3.3 V, T_A = 25°C, $R_{L(PULLDOWN)}$ = 50 kΩ to VCC	–	–	0.3	V
Primary Conductor Resistance	R_{IP}	T_A = 25°C	–	0.85	–	mΩ
Primary Hall Coupling Factor	$C_{F(P)}$	T_A = 25°C	–	4	–	G/A
Secondary Hall Coupling Factor	$C_{F(s)}$	T_A = 25°C	–	0.35	–	G/A
Hall Plate Sensitivity Matching	$Sens_{match}$	T_A = 25°C	–	2	–	%
Common Mode Field Rejection Ratio	CMFRR	T_A = 25°C	–	7	–	mA/G
Power On Delay Time	t_{POD}	T_A = 25°C; when $V_{CC} \geq V_{CC(MIN)}$ until V_{IOUT} = 90% of steady state value	–	180	–	µs
Internal Bandwidth	BW	Small signal –3 dB; C_L = 220 pF	–	1	–	MHz
Rise Time [3]	t_r	T_A = 25°C, C_L = 0.22 nF	–	0.5	–	µs
Response Time [3]	$t_{RESPONSE}$	T_A = 25°C, C_L = 0.22 nF	–	0.3	–	µs
Propagation Delay Time [3]	t_{pd}	T_A = 25°C, C_L = 0.22 nF	–	0.2	–	µs
Output Slew Rate	SR	T_A = 25°C, C_L = 0.22 nF	–	3.2	–	V/µs
Zero Current Output Ratiometry Error	$E_{RAT(Q)}$	T_A = 25°C, V_{CC} = ±5 % variation of nominal supply voltage	–16	±10	16	mV
Sensitivity Ratiometry Error	$E_{RAT(SENS)}$	T_A = 25°C, V_{CC} = ±5 % variation of nominal supply voltage	–2	±1.72	2	%
Ratiometry Bandwidth	BW_{RAT}	±100 mV on V_{CC}	–	10	–	kHz
Linearity Error [4]	E_{LIN}	T_A = 25°C, up to full-scale I_P	–	±0.5	–	%
Noise Density	I_{ND}	V_{CC} = 5.0 V, T_A = 25°C, C_L = 220 pF; input referred	–	120	–	µA/√Hz
		V_{CC} = 3.3 V, T_A = 25°C, C_L = 220 pF; input referred	–	160	–	µA/√Hz

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COMMON ELECTRICAL CHARACTERISTICS (continued): Over full range of T_A, over supply voltage range $V_{CC(MIN)}$ through $V_{CC(MAX)}$ of a sensor variant, C_{BYPASS} = 0.1 µF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
OVERCURRENT FAULT CHARACTERISTICS						
$\overline{\text{FAULT}}$ Response Time [5]	$t_{RESPONSE(F)}$	Time from $I_P > I_{\overline{FAULT}}$ to when $\overline{\text{FAULT}}$ pin is pulled below $V_{\overline{FAULT}}$; input current step from 0 to 1.2 × $I_{\overline{FAULT}}$	0.2	0.5	0.75	µs
$\overline{\text{FAULT}}$ Release Time [5]	$t_{C(F)}$	Time from I_P falling below $I_{\overline{FAULT}} - I_{HYS}$ to when $V_{\overline{FAULT}}$ is pulled above $V_{\overline{FAULT}L}$; 100 pF from $\overline{\text{FAULT}}$ to ground	0.1	–	0.45	µs
$\overline{\text{FAULT}}$ Range	$I_{\overline{FAULT}}$	Relative to the full scale of I_{PR}; set via the VOC pin	0.5 × I_{PR}	–	2 × I_{PR}	A
$\overline{\text{FAULT}}$ Output Low Voltage	$V_{\overline{FAULT}}$	In fault condition; $R_{F(PULLUP)}$ = 10 kΩ	–	–	0.4	V
$\overline{\text{FAULT}}$ Pull-Up Resistance	$R_{F(PULLUP)}$		10	–	500	kΩ
$\overline{\text{FAULT}}$ Leakage Current	$I_{\overline{FAULT}(LEAKAGE)}$		–	±5	–	µA
$\overline{\text{FAULT}}$ Hysteresis [6]	I_{HYST}		–	0.05 × I_{PR}	–	A
$\overline{\text{FAULT}}$ Error [7]	$E_{\overline{FAULT}}$	Tested at V_{VOC} = 0.2 × V_{CC} ($I_{\overline{FAULT}}$ threshold = 100% × I_{PR})	–	E_{tot} ±3	–	%
V_{OC} Input Range	V_{VOC}		0.1 × V_{CC}	–	0.4 × V_{CC}	V
V_{OC} Input Current	I_{VOC}		–	10	100	nA

[1] Typical values with ± are ±3 sigma values.
[2] Use of a bypass capacitor is required to increase output stability.
[3] See definitions of Dynamic Response Characteristics section of this datasheet.
[4] The sensor will continue to respond to current beyond the range of I_{PR} until the high or low output saturation voltage. However, the nonlinearity in this region may be worse than the nominal operating range.
[5] Guaranteed by design.
[6] After I_P goes above $I_{\overline{FAULT}}$, tripping the internal comparator, I_P must fall below $I_{\overline{FAULT}} - I_{HYST}$, before the internal comparator will reset.
[7] Fault error is defined as the value at which a fault is reported relative to the desired threshold for $I_{\overline{FAULT}}$.

ACS732KMATR-65AB-T PERFORMANCE CHARACTERISTICS: Valid at T_A = –40°C to 125°C and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–65	–	65	A
Sensitivity	Sens		–	30.77	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0 A, T_A = 25°C	–	0.5 × V_{CC}	–	V
TOTAL OUTPUT ERROR COMPONENTS						
Total Output Error [2]	E_{TOT}	$I_P = I_{PR(max)}$, T_A = 25°C	–4	±2.5	4	%
		$I_P = I_{PR(max)}$, T_A = 125°C	–3	±1	3	%
		$I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–	±5.5	–	%
		$I_P = I_{PR(max)}$, T_A = –40°C	–8	±5	8	%
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = 25°C	–1.5	±0.75	1.5	%
		$I_P = I_{PR(max)}$, T_A = 125°C	–1.5	±0.75	1.5	%
		$I_P = I_{PR(max)}$, T_A = –40°C	–3	±2	3	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C	–90	±57	90	mV
		I_P = 0 A, T_A = 125°C	–60	±15	60	mV
		I_P = 0 A, T_A = 25°C to 125°C	–	±100	–	mV
		I_P = 0 A, T_A = –40°C	–170	±90	170	mV
LIFETIME DRIFT CHARACTERISTICS						
Total Output Error Including Lifetime Drift	$E_{TOT(DRIFT)}$	$I_P = I_{PR(max)}$, T_A = 25°C, 125°C	–	±20	–	%
Sensitivity Error Including Lifetime Drift	$E_{SENS(DRIFT)}$	$I_P = I_{PR(max)}$, T_A = 25°C, 125°C	–	±4.3	–	%
Offset Voltage Error Including Lifetime Drift	$V_{OE(DRIFT)}$	I_P = 0 A, T_A = 25°C, 125°C	–	±284	–	mV

[1] Typical values with ± are ±3 sigma values, except for lifetime drift, which are the average value including drift (from the worst-case stress) after AEC-Q100 qualification.
[2] Percentage of I_P, with $I_P = I_{PR(MAX)}$, output filtered.
[3] Lifetime drift characteristics are based on AEC-Q100 qualification results. Typical values are mean ±3 sigma of worst-case stress testing. Drift is a function of customer application conditions.

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ACS732KMATR-75AB-T PERFORMANCE CHARACTERISTICS: Valid at T_A = –40°C to 125°C and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–75	–	75	A
Sensitivity	Sens		–	26.67	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0 A, T_A = 25°C	–	0.5 × V_{CC}	–	V
TOTAL OUTPUT ERROR COMPONENTS						
Total Output Error [2]	E_{TOT}	$I_P = I_{PR(max)}$, T_A = 25°C	–4	±2.5	4	%
		$I_P = I_{PR(max)}$, T_A = 125°C	–3	±1	3	%
		$I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–	±5.5	–	%
		$I_P = I_{PR(max)}$, T_A = –40°C	–8	±5	8	%
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = 25°C	–1.5	±0.75	1.5	%
		$I_P = I_{PR(max)}$, T_A = 125°C	–1.5	±0.75	1.5	%
		$I_P = I_{PR(max)}$, T_A = –40°C	–3	±2	3	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C	–90	±57	90	mV
		I_P = 0 A, T_A = 125°C	–60	±15	60	mV
		I_P = 0 A, T_A = 25°C to 125°C	–	±100	–	mV
		I_P = 0 A, T_A = –40°C	–170	±90	170	mV
LIFETIME DRIFT CHARACTERISTICS [3]						
Total Output Error Including Lifetime Drift [4]	$E_{TOT(DRIFT)}$	$I_P = I_{PR(max)}$, T_A = 25°C, 125°C	–	±20	–	%
Sensitivity Error Including Lifetime Drift [5]	$E_{SENS(DRIFT)}$	$I_P = I_{PR(max)}$, T_A = 25°C, 125°C	–	±4.3	–	%
Offset Voltage Error Including Lifetime Drift [6]	$V_{OE(DRIFT)}$	I_P = 0 A, T_A = 25°C, 125°C	–	±284	–	mV

[1] Typical values with ± are ±3 sigma values, except for lifetime drift, which are the average value including drift (from the worst-case stress) after AEC-Q100 qualification.
[2] Percentage of I_P, with $I_P = I_{PR(MAX)}$, output filtered.
[3] Lifetime drift characteristics are based on AEC-Q100 qualification results. Typical values are mean ±3 sigma of worst-case stress testing. Drift is a function of customer application conditions.

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ACS733KMATR-65AB-T PERFORMANCE CHARACTERISTICS: Valid at T_A = –40°C to 125°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–65	–	65	A
Sensitivity	Sens		–	20.3	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0 A, T_A = 25°C	–	0.5 × V_{CC}	–	V
TOTAL OUTPUT ERROR COMPONENTS						
Total Output Error [2]	E_{TOT}	$I_P = I_{PR(max)}$, T_A = 25°C	–4.5	±2.5	4.5	%
		$I_P = I_{PR(max)}$, T_A = 125°C	–3	±1	3	%
		$I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–	±5.5	–	%
		$I_P = I_{PR(max)}$, T_A = –40°C	–9	±5	9	%
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = 25°C	–1.5	±1.25	1.5	%
		$I_P = I_{PR(max)}$, T_A = 125°C	–1.5	±0.8	1.5	%
		$I_P = I_{PR(max)}$, T_A = –40°C	–4	±2.5	4	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C	–55	±25	55	mV
		I_P = 0 A, T_A = 125°C	–40	±5	40	mV
		I_P = 0 A, T_A = 25°C to 125°C	–	±70	–	mV
		I_P = 0 A, T_A = –40°C	–110	±60	110	mV
LIFETIME DRIFT CHARACTERISTICS [3]						
Total Output Error Including Lifetime Drift [4]	$E_{TOT(DRIFT)}$	$I_P = I_{PR(max)}$, T_A = 25°C, 125°C	–	±20	–	%
Sensitivity Error Including Lifetime Drift [5]	$E_{SENS(DRIFT)}$	$I_P = I_{PR(max)}$, T_A = 25°C, 125°C	–	±4.3	–	%
Offset Voltage Error Including Lifetime Drift [6]	$V_{OE(DRIFT)}$	I_P = 0 A, T_A = 25°C, 125°C	–	±284	–	mV

[1] Typical values with ± are ±3 sigma values, except for lifetime drift, which are the average value including drift (from the worst-case stress) after AEC-Q100 qualification.
[2] Percentage of I_P, with $I_P = I_{PR(MAX)}$, output filtered.
[3] Lifetime drift characteristics are based on AEC-Q100 qualification results. Typical values are mean ±3 sigma of worst-case stress testing. Drift is a function of customer application conditions.

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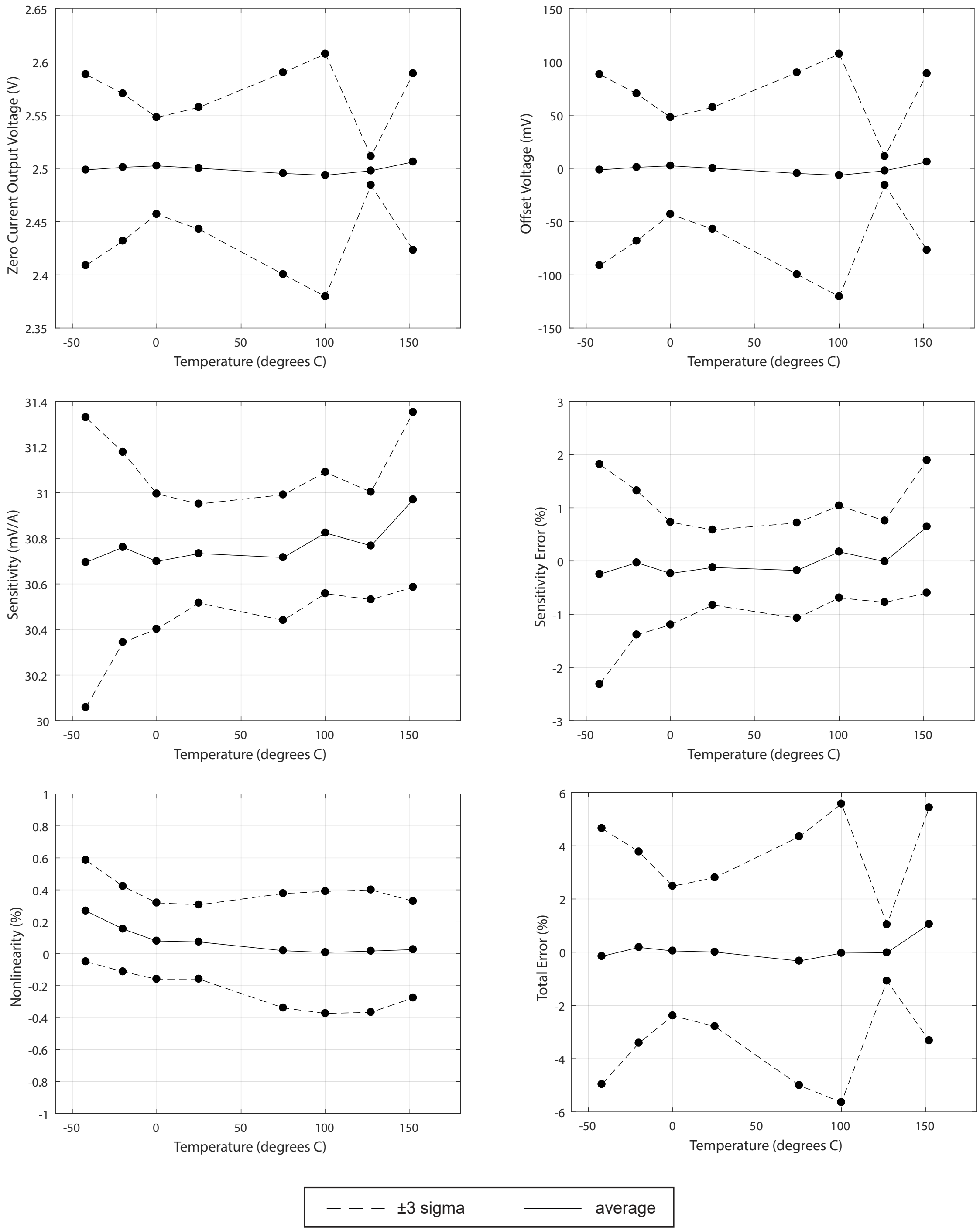
CHARACTERISTIC PERFORMANCE
ACS732KMATR-65AB-T (5 V)

for ~100 parts



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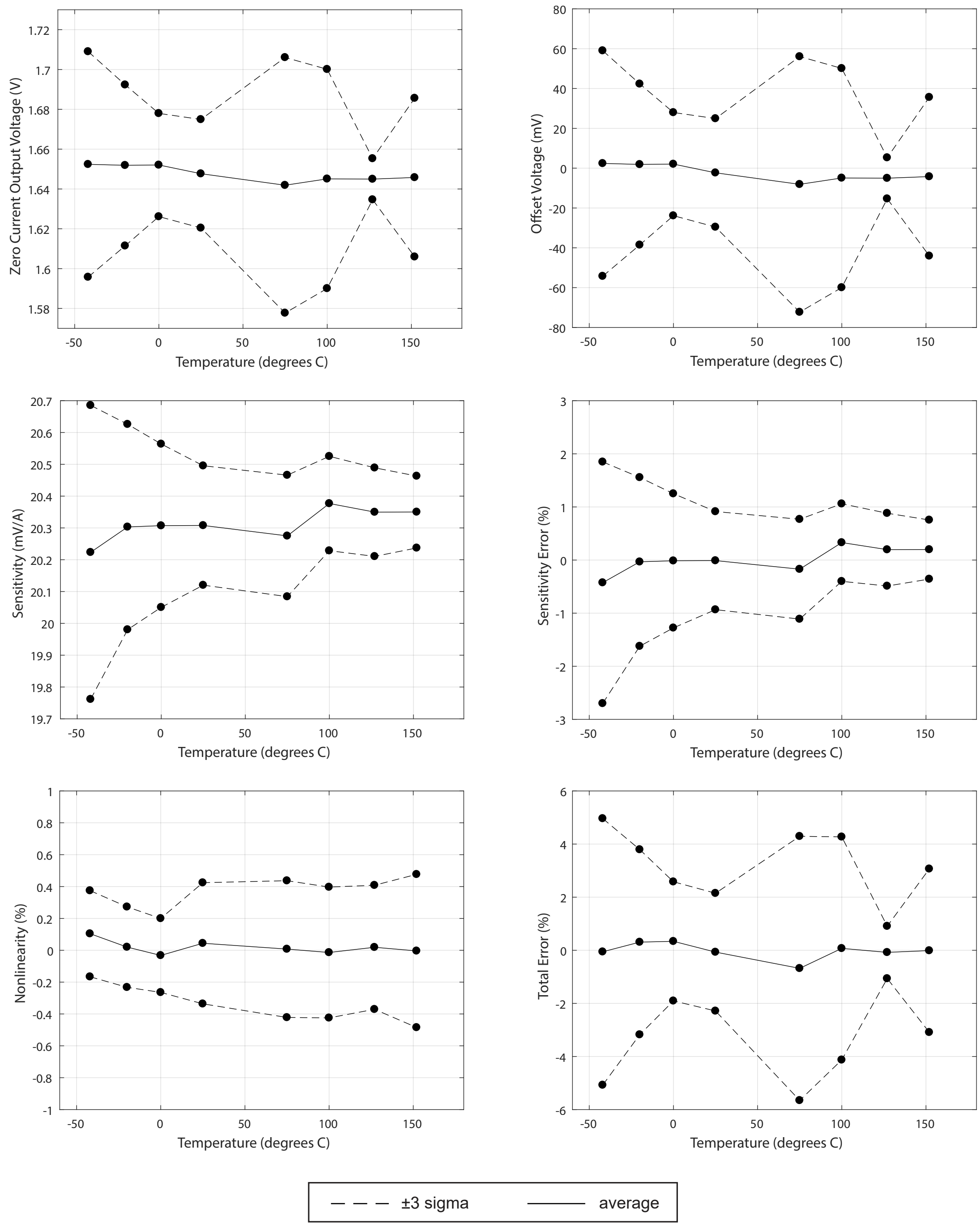
CHARACTERISTIC PERFORMANCE
ACS733KMATR-65AB-T (3.3 V)
for ~100 parts



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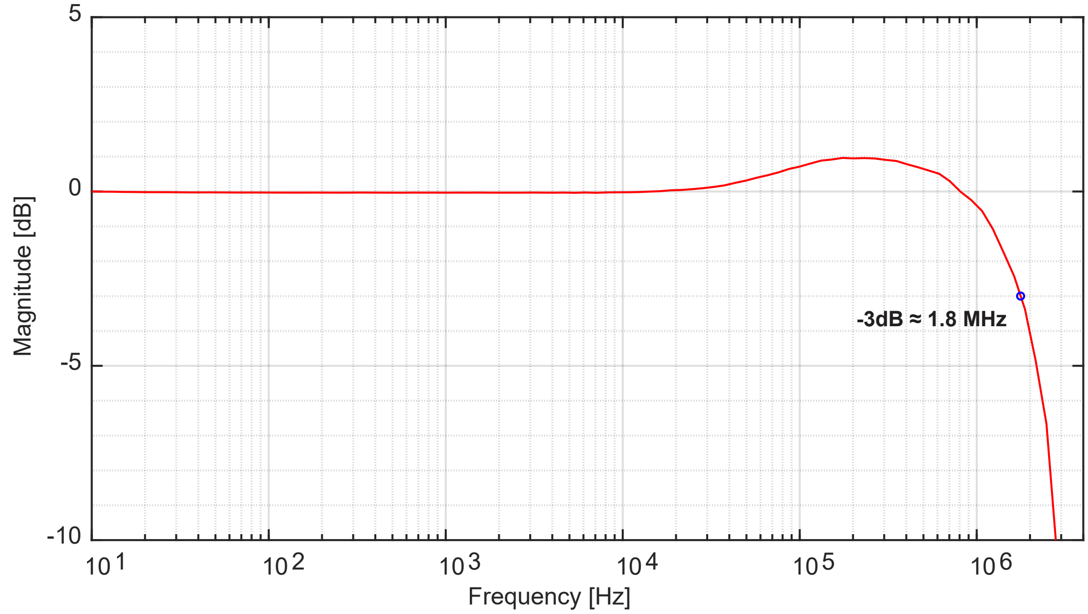
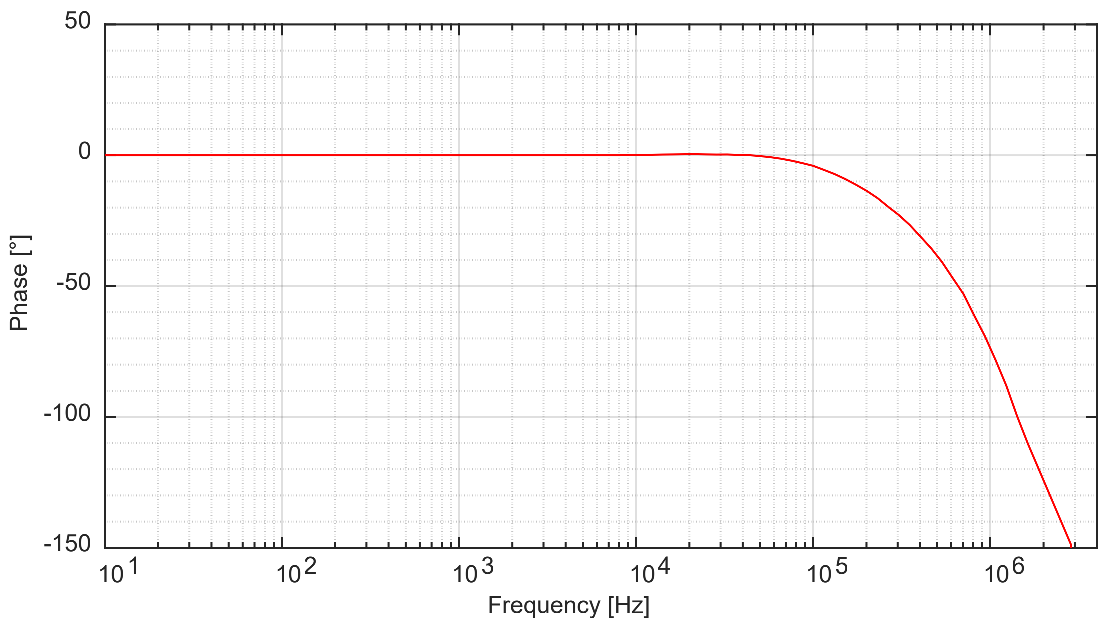
CHARACTERISTIC PERFORMANCE
ACS732 AND ACS733 TYPICAL FREQUENCY RESPONSE





For information regarding bandwidth characterization methods used for the ACS732 and ACS733, see the "Characterizing System Bandwidth" application note (https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296169-acs720-bandwidth-testing) on the Allegro website.

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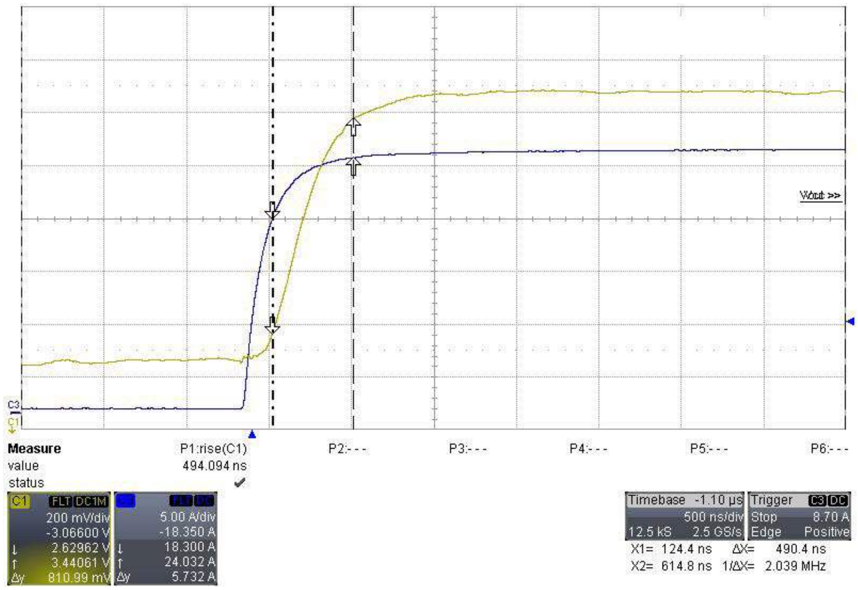
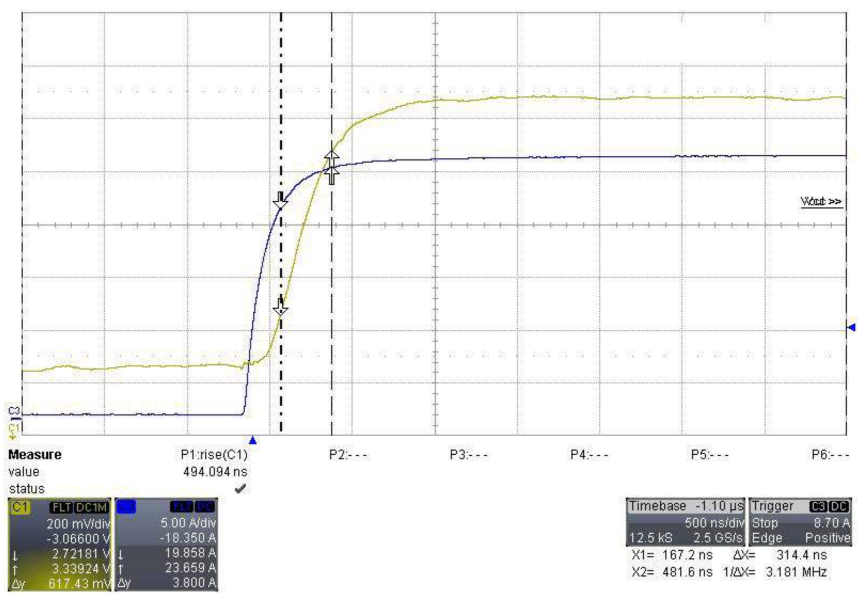
CHARACTERISTIC PERFORMANCE: ACS732 (5 V), Rise Time

Test Conditions: T_A = 25°C, C_{BYPASS} = 0.1 µF, C_{LOAD} = 220 pF. Input Step = 25 A with 0.3 µs rise time.



Response Time

Test Conditions: T_A = 25°C, C_{BYPASS} = 0.1 µF, C_{LOAD} = 220 pF. Input Step = 25 A with 0.3 µs rise time.



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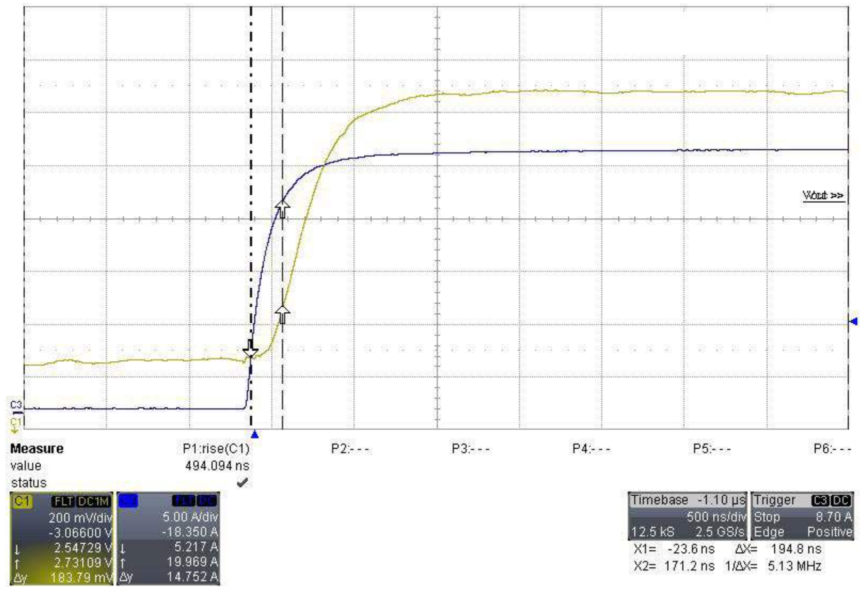
Propagation Delay Time

Test Conditions: T_A = 25°C, C_{BYPASS} = 0.1 µF, C_{LOAD} = 220 pF. Input Step = 25 A with 0.3 µs rise time.



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OVERCURRENT FAULT

Overcurrent Fault

The ACS732 and ACS733 have fast and accurate overcurrent fault detection circuitry. The overcurrent fault threshold ($I_{\overline{FAULT}}$) is user-configurable via an external resistor divider and supports a range of 50% to 200% of the full-scale primary input ($I_{PR(MAX)}$). Fault response and the overcurrent fault thresholds are described in the following sections.

Fault Response

The high bandwidth of the ACS732 and ACS733 devices allow for extremely fast and accurate overcurrent fault detection. An overcurrent event occurs when the magnitude of the input current (I_P) exceeds the user-set threshold ($I_{\overline{FAULT}}$). Fault response time ($t_{RESPONSE(F)}$) is defined from the time I_P goes above $I_{\overline{FAULT}}$ to the time the $\overline{FAULT}$ pin goes below $V_{\overline{FAULT}}$. Overcurrent fault response is illustrated in Figure 3. When I_P goes below $I_{\overline{FAULT}}$ – I_{HYST}, the $\overline{FAULT}$ pin will be released. The rise time of $V_{\overline{FAULT}}$ will depend on the value of the resistor $R_{F(PULLUP)}$ and the capacitance on the pin.

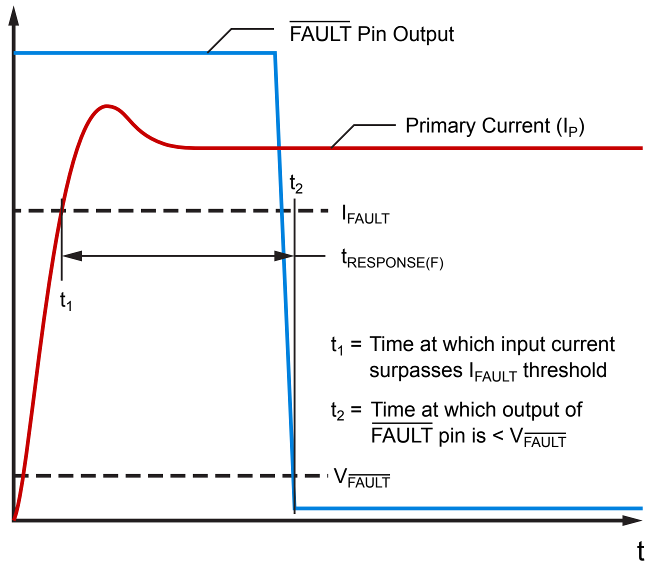

Figure 3: Overcurrent Fault Response

Setting the Overcurrent Fault Threshold

The overcurrent fault threshold (I_{FAULT}) is set via a resistor divider from V_{CC} to ground on the VOC pin. The voltage on the VOC pin, V_{VOC}, may range from $0.1 \times V_{CC}$ to $0.4 \times V_{CC}$. I_{FAULT} may be set anywhere from 50% to 200% $I_{PR(MAX)}$.

Overcurrent fault threshold versus V_{VOC} is shown in Figure 4.

The equation for calculating the trip current is shown below. For bidirectional devices, the fault will trip for both positive and negative currents.

$$I_{FAULT} = I_{PR(MAX)} \left\{ 5 \times \frac{V_{VOC}}{V_{CC}} \right\}$$

This may be rearranged to solve for the appropriate V_{VOC} value based on a desired over current fault threshold, shown by the equation:

$$V_{VOC} = \frac{V_{CC}}{5} \times \frac{I_{FAULT}}{I_{PR(MAX)}}$$

By setting V_{VOC} with a resistor divider from V_{CC}, the ratio of V_{VOC} / V_{CC} will remain constant with changes to V_{CC}. In this regard, the fault trip point will remain constant even as the supply voltage varies.

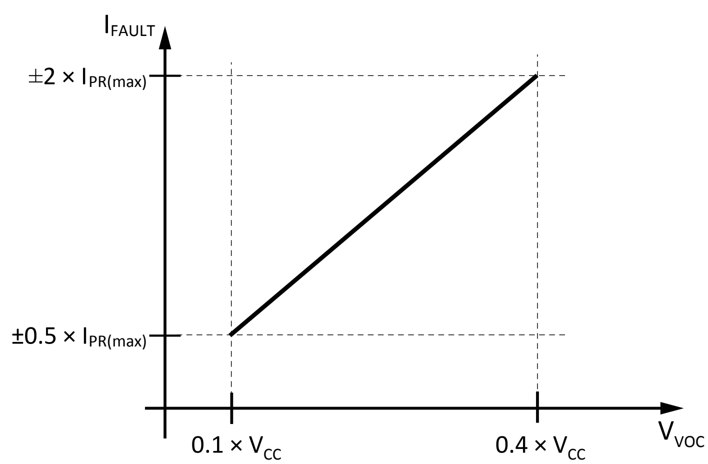

Figure 4: Fault Threshold vs. V_{VOC}

It is best practice to use resistor values < 10 kΩ for setting V_{VOC}. With larger resistor values, the leakage current on VOC may result in errors in the trip point.

DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

Power-On Delay Time (t_{POD})

When the supply is ramped to its operating voltage, the device requires a finite amount of time to power its internal components before responding to an input magnetic field. Power-On Delay Time (t_{POD}) is defined as the time interval between a) the power supply has reached its minimum specified operating voltage ($V_{CC(MIN)}$), and b) when the sensor output has settled within ±10% of its steady-state value under an applied magnetic field. Power-On Delay Time is illustrated in Figure 5.

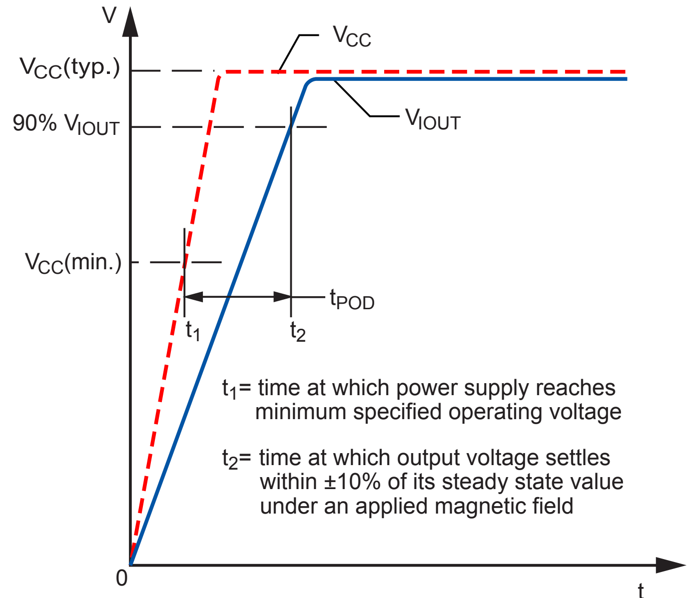

Figure 5: Power-On Delay Time (t_{POD})

Rise Time (t_r)

The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

Propagation Delay (t_{pd})

The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

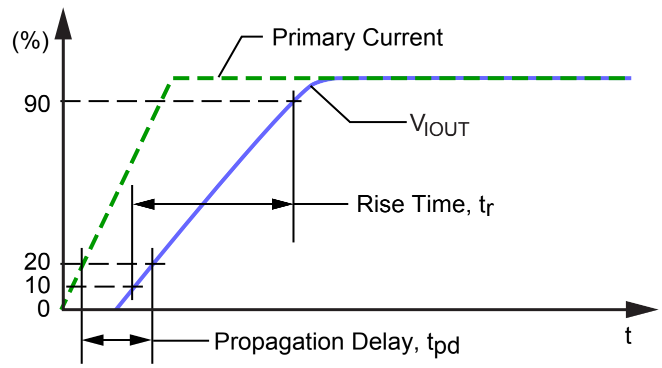

Figure 6: Rise Time (t_r) and Propagation Delay (t_{pd})

Response Time ($t_{RESPONSE}$)

The time interval between a) when the sensed input current reaches 80% of its final value, and b) when the sensor output reaches 80% of its full-scale value.

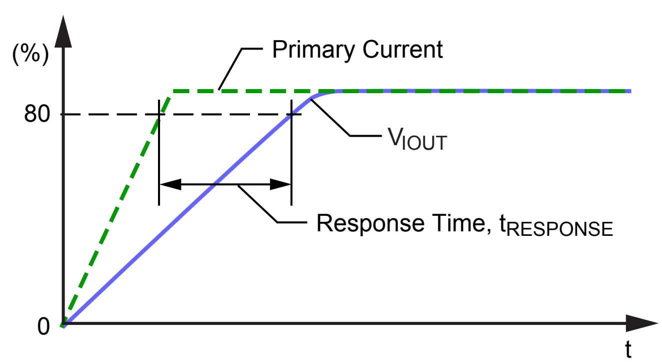

Figure 7: Response Time ($t_{RESPONSE}$)

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DEFINITIONS OF ACCURACY CHARACTERISTICS

Sensitivity (Sens). The change in sensor IC output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) (1 G = 0.1 mT) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Nonlinearity (E_{LIN}). The nonlinearity is a measure of how linear the output of the sensor IC is over the full current measurement range. The nonlinearity is calculated as:

$$E_{LIN} = \left\{ 1 - \left[\frac{V_{IOUT}(I_{PR(max)}) - V_{IOUT(Q)}}{2 \times V_{IOUT}(I_{PR(max)}/2) - V_{IOUT(Q)}} \right] \right\}$$

where $V_{IOUT}(I_{PR(max)})$ is the output of the sensor IC with the maximum measurement current flowing through it and $V_{IOUT}(I_{PR(max)}/2)$ is the output of the sensor IC with half of the maximum measurement current flowing through it.

Zero Current Output Voltage ($V_{IOUT(Q)}$). The output of the sensor when the primary current is zero. For a unipolar supply voltage, it nominally remains at 0.5 × V_{CC} for a bidirectional device and 0.1 × V_{CC} for a unidirectional device. For example, in the case of a bidirectional output device, V_{CC} = 3.3 V translates into $V_{IOUT(Q)}$ = 1.65 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Offset Voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of 0.5 × V_{CC} (bidirectional) or 0.1 × V_{CC} (unidirectional) due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Total Output Error (E_{TOT}). The difference between the current measurement from the sensor IC and the actual current (I_P), relative to the actual current. This is equivalent to the difference between the ideal output voltage and the actual output voltage, divided by the ideal sensitivity, relative to the current flowing through the primary conduction path:

$$E_{TOT}(I_P) = \frac{V_{IOUT_{ideal}}(I_P) - V_{IOUT}(I_P)}{Sens_{ideal}(I_P) \times I_P} \times 100\ (\%)$$

The Total Output Error incorporates all sources of error and is a function of I_P. At relatively high currents, E_{TOT} will be mostly due to sensitivity error, and at relatively low currents, E_{TOT} will be mostly due to Offset Voltage (V_{OE}). In fact, as I_P approaches zero, E_{TOT} approaches infinity due to the offset voltage. This is illustrated in Figure 8 and Figure 9. Figure 8 shows a distribution of output voltages versus I_P at 25°C and across temperature. Figure 9 shows the corresponding E_{TOT} versus I_P.

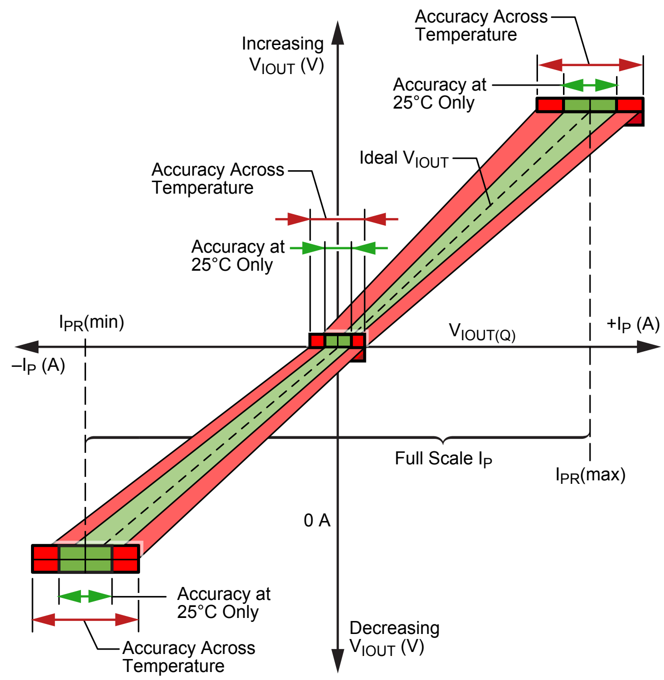

Figure 8: Output Voltage versus Sensed Current

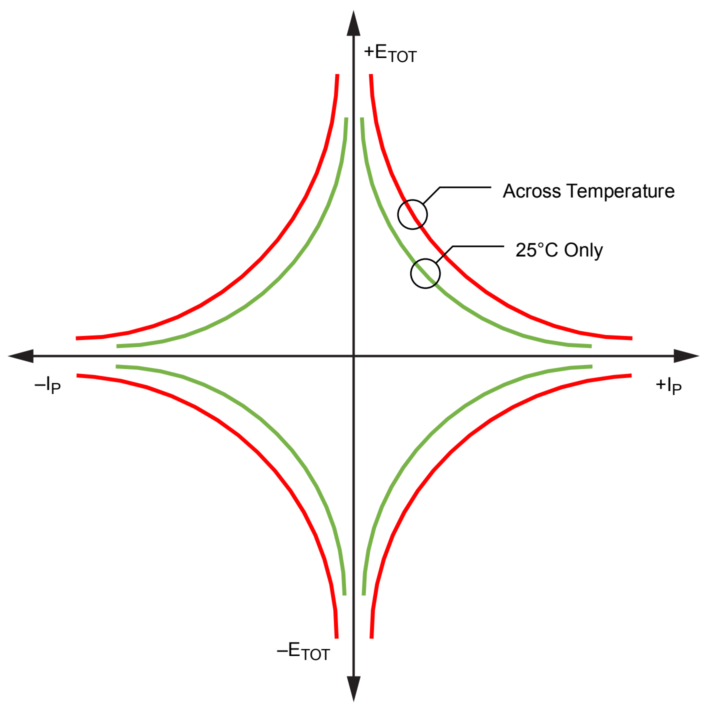

Figure 9: Total Output Error versus Sensed Current

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APPLICATION INFORMATION

Ratiometry

The ACS732 and ACS733 are both ratiometric sensors. This means that for a given change in supply voltage, the device's zero current output voltage and sensitivity will scale proportionally.

Sensitivity Ratiometry

Ideally, a 5% increase in V_{CC} will result in a 5% increase in sensitivity. However, the ratiometric response of any sensor is not ideal. Ratiometric Sensitivity Error $E_{RAT(SENS)}$ is specified by the equation:

$$E_{RAT(SENS)} = 100\% \times \left(1 - \frac{Sensitivity_{VCC}}{Sensitivity_{VCC(N)}} \times \frac{V_{CC(N)}}{V_{CC}}\right)$$

where $V_{CC(N)}$ is equal to the nominal V_{CC} (3.3 V, or 5.0 V) and $Sensitivity_{VCC(N)}$ is the measured sensitivity at nominal V_{CC} for a particular device. The symbol V_{CC} is the measured V_{CC} value in application and $Sensitivity_{VCC}$ is the measured sensitivity at that V_{CC} level for a particular device.

Zero Current Offset Ratiometry

Ratiometric error for Zero Current Offset may be calculated using the following equation:

$$E_{RAT(Q)} = V_{IOUT(Q)VCC} - V_{IOUT(Q)VCC(N)} \times \frac{V_{CC}}{V_{CC(N)}}$$

Where $V_{CC(N)}$ is equal to the nominal V_{CC} (3.3 V, or 5.0 V) and $V_{IOUT(Q)VCC(N)}$ is the measured Zero Current Offset voltage at nominal V_{CC} for a particular device. The symbol V_{CC} is the measured V_{CC} value in application and $V_{IOUT(Q)VCC}$ is the measured zero current offset voltage for a particular device.

Estimating Total Error vs. Sensed Current

The performance characteristics tables give distribution (±3 sigma) values for Total Error at $I_{PR(MAX)}$; however, one may be interested in the expected error at a particular current. This error may be estimated using the distribution data for the components of Total Error, Sensitivity Error, and Offset Voltage. The ±3 sigma value for Total Error (E_{TOT}) as a function if the sensed current is estimated as:

$$E_{TOT}(I_P) = \sqrt{E_{SENS}^2 + \left(\frac{100 \times V_{OE}}{Sens \times I_P}\right)^2}$$

where E_{SENS} and V_{OE} are the ±3 sigma values for those error terms.

If there is an average sensitivity error or average offset voltage, then the average Total Error is estimated as:

$$E_{TOT_{AVG}}(I_P) = E_{SENS_{AVG}} + \frac{100 \times V_{OE_{AVG}}}{Sens \times I_P}$$

Layout Guidelines

There are a few considerations during PCB layout that will help to maintain high accuracy when using Allegro's integrated current sensors. Below is a list of common layout mistakes that should be avoided:

- Extending current carrying traces too far beneath the IC, or injecting current from the side of the IC
- Placing secondary current phase traces too close to or below the IC

Extending the Current Traces

The length of copper trace beneath the IC may impact the path of current flowing through the IP bus. This may cause variation in the coupling factor from the primary current loop of the package to the IC, and may reduce the overall creepage distance in application.

It is best practice for the current to approach the IC parallel to the current-carrying pins, and for the current-carrying trace to not creep towards the center of the package. Refer to Figure 10.

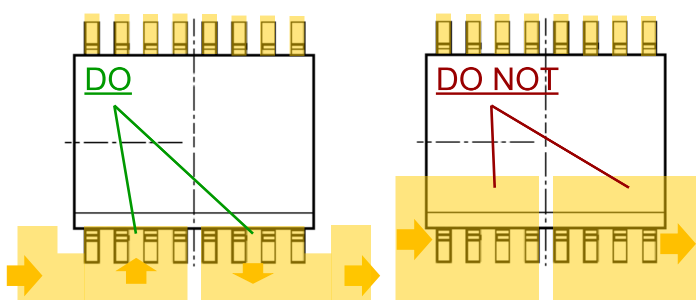

Figure 10: Best Practice Layout Techniques for Current Traces

If current must approach the package from the side, it is recommended to reduce the angle as much as possible. For more information on best current sensor layout practices refer to the application note "Techniques to Minimize Common-Mode Field Interference When Using Allegro Current Sensor ICs" on the Allegro website.

Thermal Rise vs. Primary Current

Self-heating due to the flow of current should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat as current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current, current "on-time", and duty cycle. While the data presented in this section was collected with direct current (DC), these numbers may be used to approximate thermal response for both AC signals and current pulses.

The plot in Figure 11 shows the measured rise in steady-state die temperature of the ACS732/3 versus continuous current at an ambient temperature, T_A, of 25°C. The thermal offset curves may be directly applied to other values of T_A. Conversely, Figure 12 shows the maximum continuous current at a given T_A. Surges beyond the maximum current listed in Figure 12 are allowed given the maximum junction temperature, $T_{J(MAX)}$ (165°C), is not exceeded.

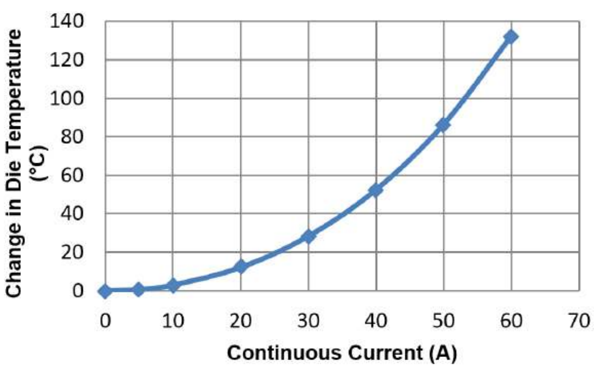

Figure 11: Self Heating in the MA Package Due to Current Flow

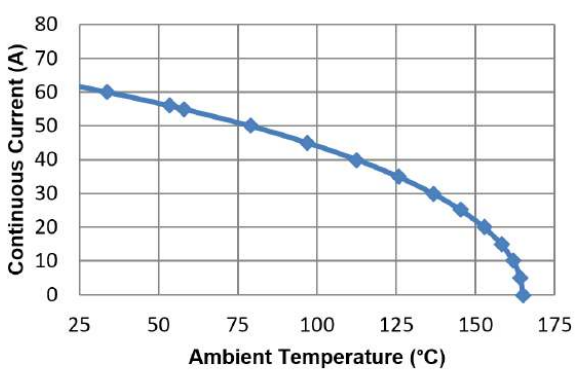

Figure 12: Maximum Continuous Current at a Given T_A

The thermal capacity of the ACS732/3 should be verified by the end user in the application's specific conditions. The maximum junction temperature, $T_{J(MAX)}$, should not be exceeded. Further information on this application testing is available in the DC and Transient Current Capability application note on the Allegro website.

ASEK73x Evaluation Board Layout

Thermal data shown in Figure 11 was collected using the ASEK73x Evaluation Board (TED-0002717). This board includes 1500 mm^2 of 2 oz. (0.0694 mm) copper connected to pins 1 through 4 and pins 5 through 8, with thermal vias connecting the layers. Top and bottom layers of the PCB are shown below in Figure 13.

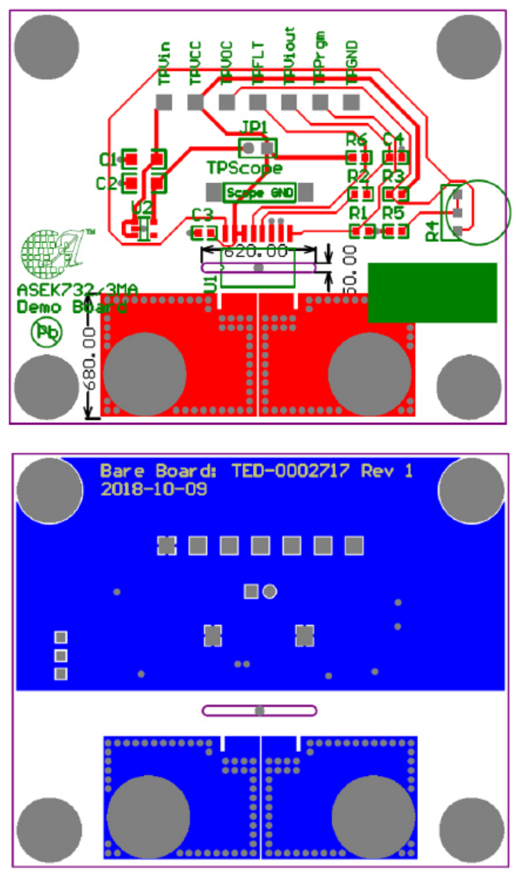

Figure 13: Top and Bottom Layers for ASEK73x Evaluation Board

Gerber files for the ASEK73x evaluation board are available for download from our website. Please see the technical documents section of the ACS733 and ACS732 device webpage.

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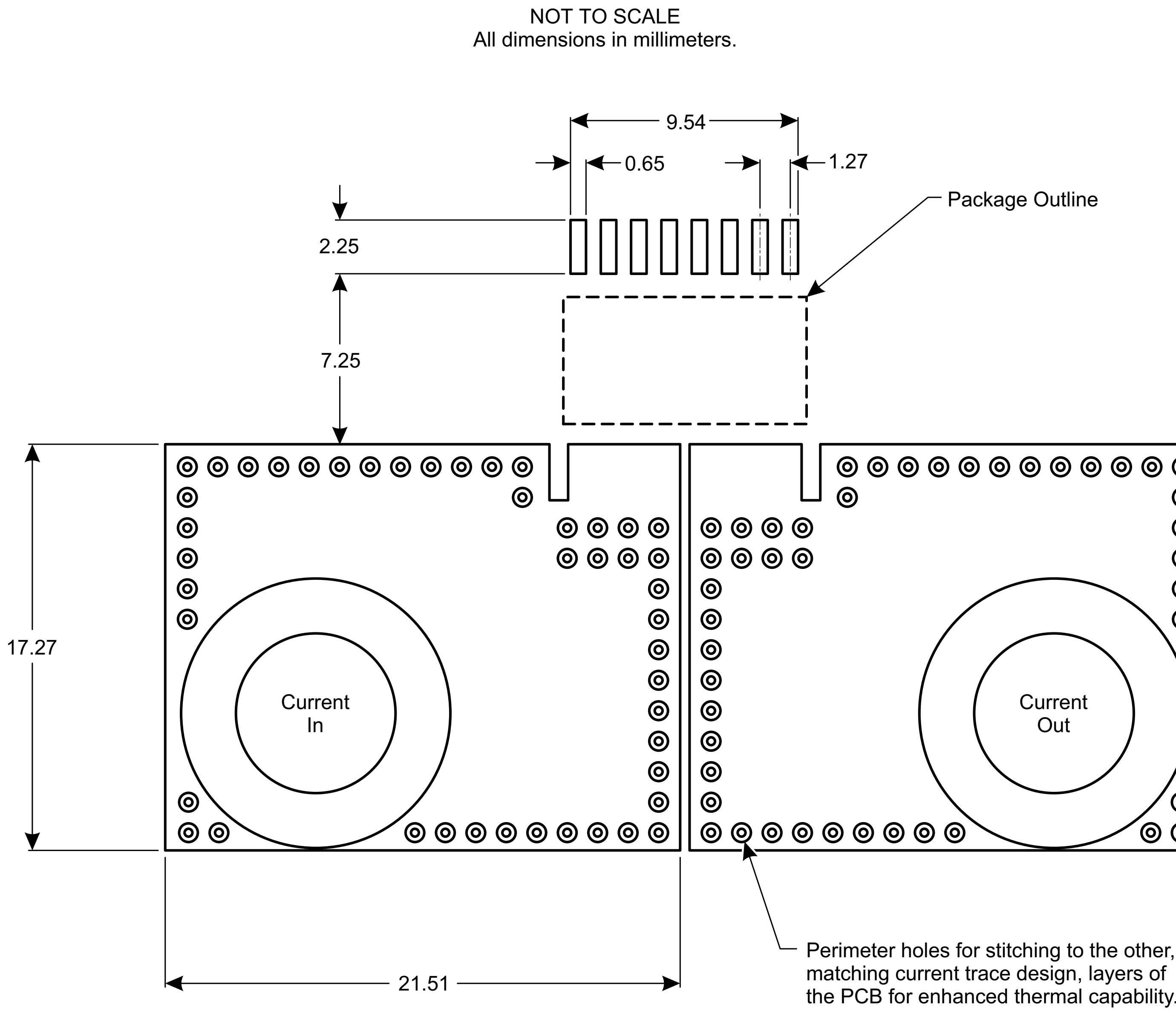

Figure 14: High-Isolation PCB Layout

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

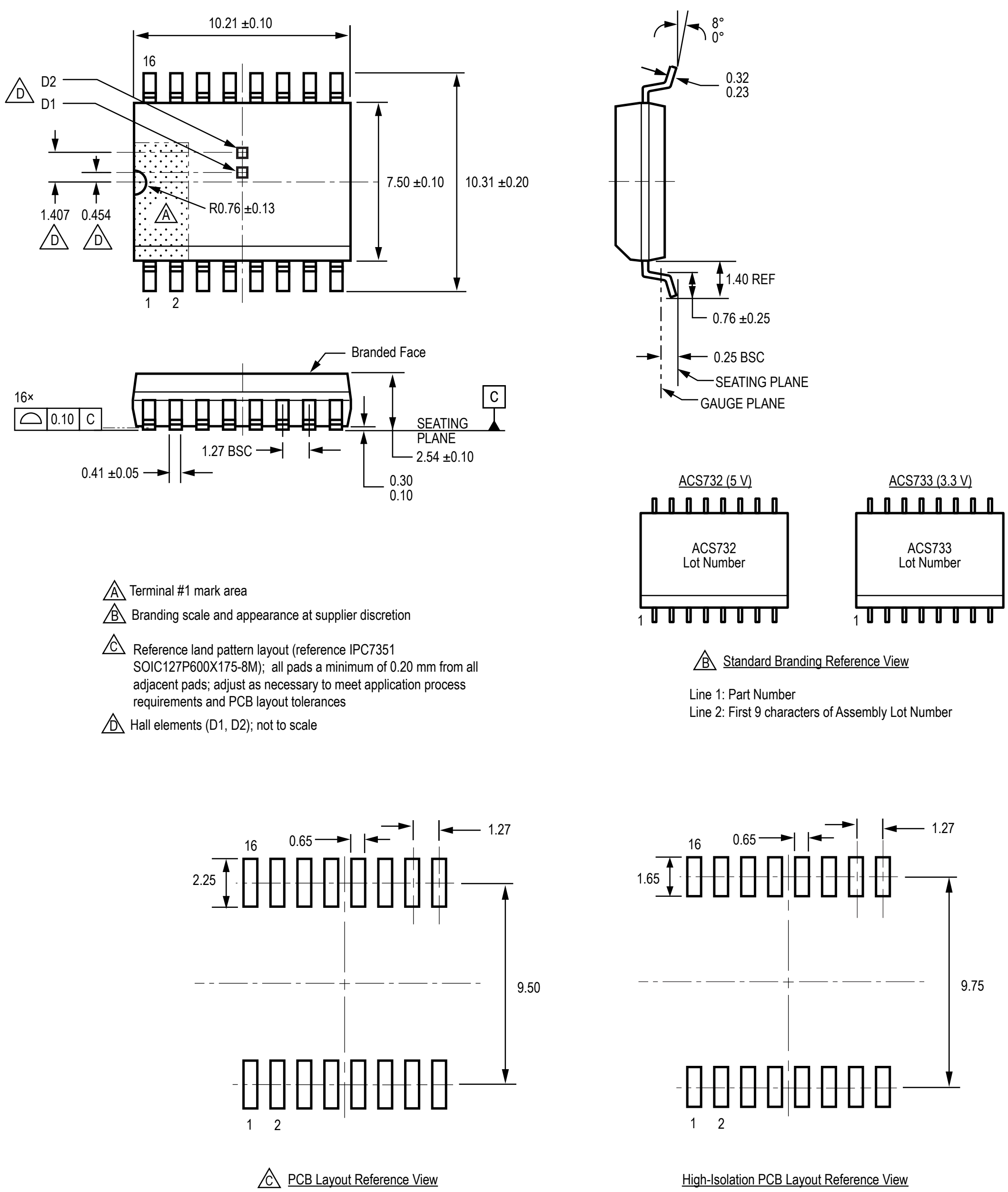

Figure 15: Package MA, 16-Pin SOICW

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Revision History

Number	Date	Description
–	February 8, 2019	Initial release
1	May 13, 2019	Updated Isolation Characteristics table (page 2)
2	August 22, 2019	Added Maximum Continuous Current to Absolute Maximum Ratings table (page 2), ESD ratings table (page 3), and updated thermal data section (page 18)
3	September 10, 2019	Added Hall plate dimensions (page 20).
4	December 20, 2019	Corrected Reverse V_{OC} Voltage value (page 2); added Distance Through Insulation and Comparative Tracking Index to Isolation Characteristics table (page 3); updated Rise Time, Response Time, Propagation Delay, and Output Slew Rate test conditions, and added Output Slew Rate (page 5); updated Typical Frequency Response plots (page 11).
5	September 4, 2020	Updated UL Certificate number (page 1).
6	October 7, 2020	Added ACS732KMATR-75AB-T variant; updated UL certification status and Isolation Characteristics table (pages 1, 3).
7-8	November 18, 2021	Updated package drawing per DWG-0000388, Rev. 1; corrected file submission
9	May 18, 2022	Updated Lifetime Drift Characteristics tables (pages 7-9)

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