STL90N6F7

N-channel 60 V, 0.0046 Ω typ., 90 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

PowerFLAT™ 5x6

Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL90N6F7	60 V	0.0054 Ω	90 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Figure 1: Internal schematic diagram

Table 1: Device summary

Order code	Marking	Package	Packing
STL90N6F7	90N6F7	PowerFLAT™ 5x6	Tape and reel

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Contents

1   Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D[1]	Drain current (continuous) at T_C = 25 °C	90	A
I_D[1]	Drain current (continuous) at T_C = 100 °C	66	A
I_{DM}[1][2]	Drain current (pulsed)	360	A
I_D[3]	Drain current (continuous) at T_{pcb} = 25 °C	21	A
I_D[3]	Drain current (continuous) at T_{pcb} = 100 °C	15	A
I_{DM}[2][3]	Drain current (pulsed)	84	A
P_{TOT}[1]	Total dissipation at T_C = 25 °C	94	W
P_{TOT}[3]	Total dissipation at T_{pcb} = 25 °C	4.8	W
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature	175	°C

Notes:

[1]This value is rated according to R_{thj-c}

[2]Pulse width limited by safe operating area

[3]This value is rated according to $R_{thj-pcb}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$[1]	Thermal resistance junction-pcb max.	31.3	°C/W
$R_{thj-case}$	Thermal resistance junction-case max.	1.6	°C/W

Notes:

[1]When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 60 V			1	μA
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10.5 A		0.0046	0.0054	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1600	-	pF
C_{oss}	Output capacitance		-	880	-	pF
C_{rss}	Reverse transfer capacitance		-	66	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 21 A, V_{GS} = 10 V	-	25	-	nC
Q_{gs}	Gate-source charge		-	7.2	-	nC
Q_{gd}	Gate-drain charge		-	8.1	-	nC

Table 6: Switching times

| Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 10.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	15	-	ns
t_r	Rise time		-	17.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	24.4	-	ns
t_f	Fall time		-	7.8	-	ns

Table 7: Source-drain diode

| Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}[1]	Forward on voltage	I_{SD} = 21 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	I_D = 21 A, di/dt = 100 A/μs V_{DD} = 48 V	-	39.6		ns
Q_{rr}	Reverse recovery charge		-	36		nC
I_{RRM}	Reverse recovery current		-	1.8		A

Notes:

[1]Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2.1 Electrical characteristics

Figure 2: Safe operating area
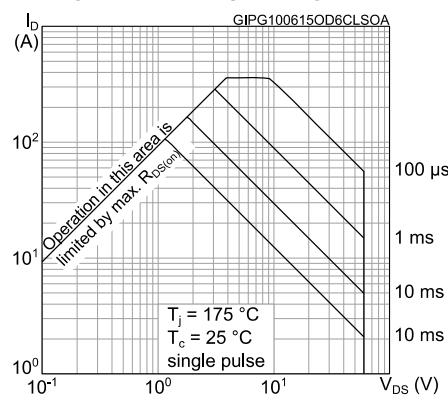
Figure 3: Thermal impedance
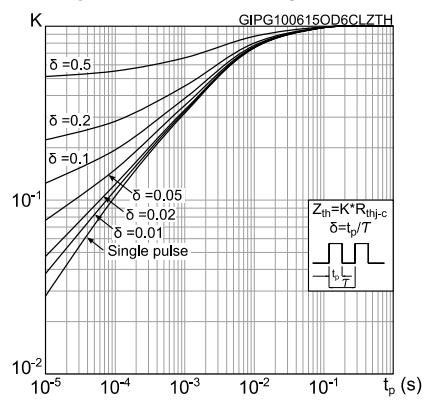
Figure 4: Output characteristics
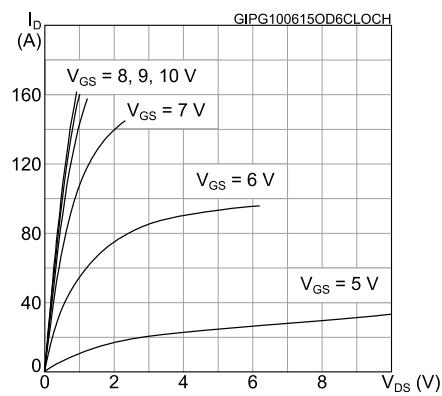
Figure 5: Transfer characteristics
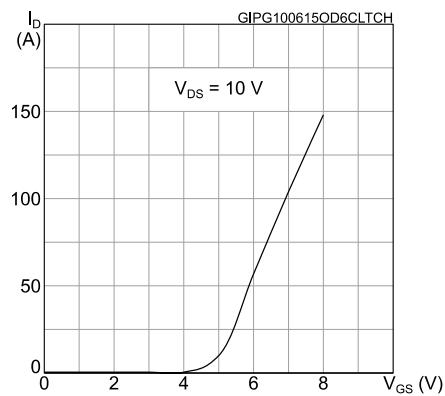
Figure 6: Gate charge vs gate-source voltage
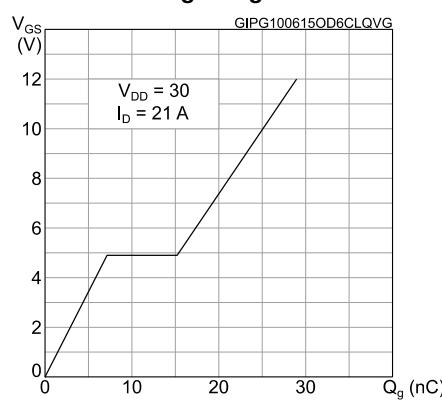
Figure 7: Static drain-source on-resistance
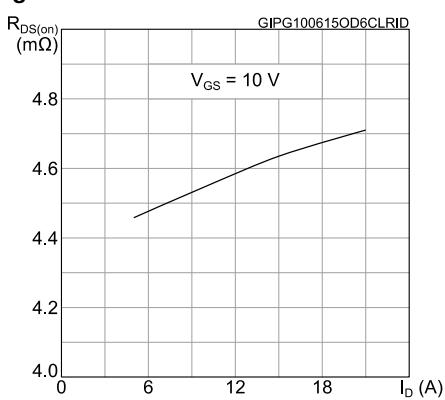
Figure 8: Capacitance variations
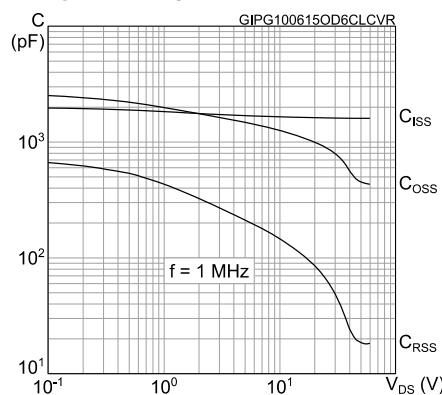
Figure 9: Normalized gate threshold voltage vs temperature
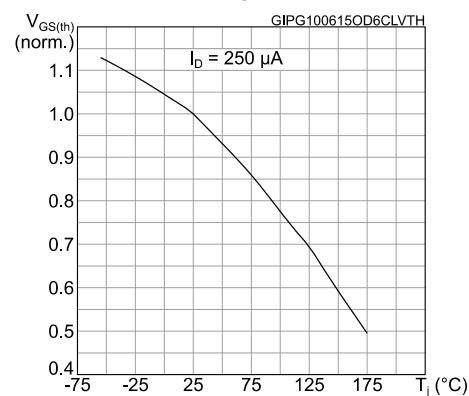
Figure 10: Normalized on-resistance vs temperature
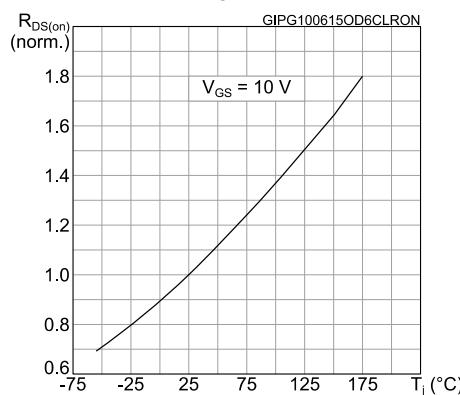
Figure 11: Normalized V(BR)DSS vs temperature
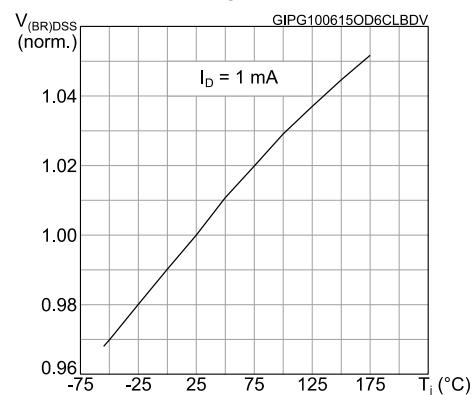
Figure 12: Source-drain diode forward characteristics
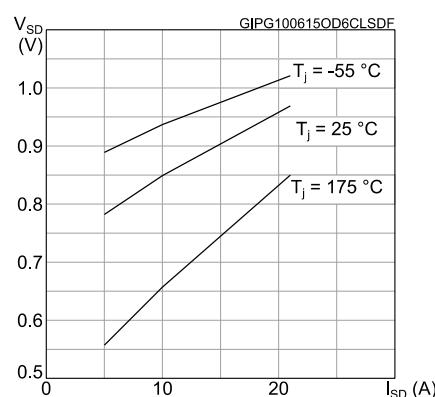
3   Test circuits

Figure 13: Switching times test circuit for resistive load

AM01468v1
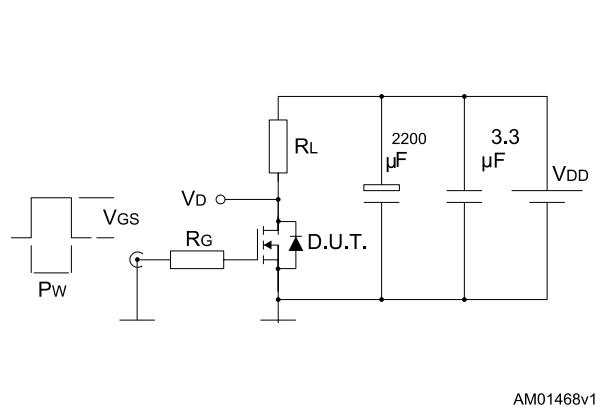
Figure 14: Gate charge test circuit

AM01469v1
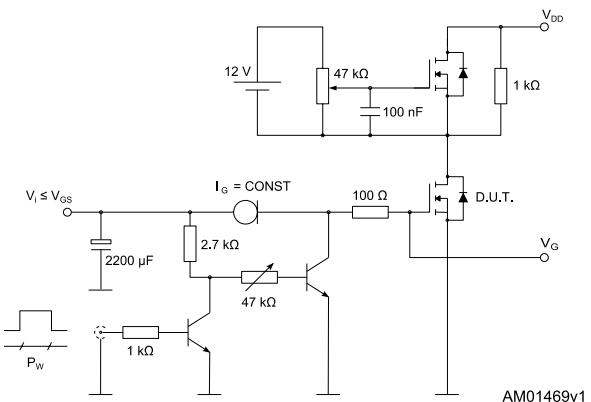
Figure 15: Test circuit for inductive load switching and diode recovery times

AM01470v1
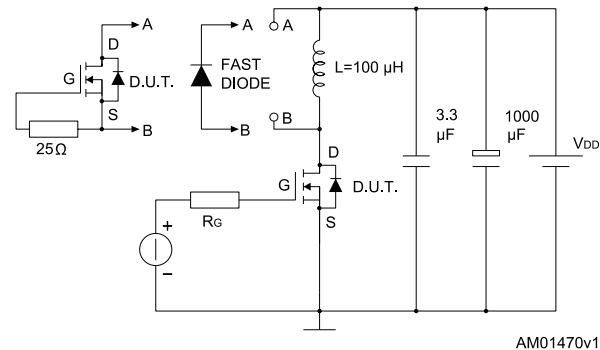
Figure 16: Unclamped inductive load test circuit

AM01471v1
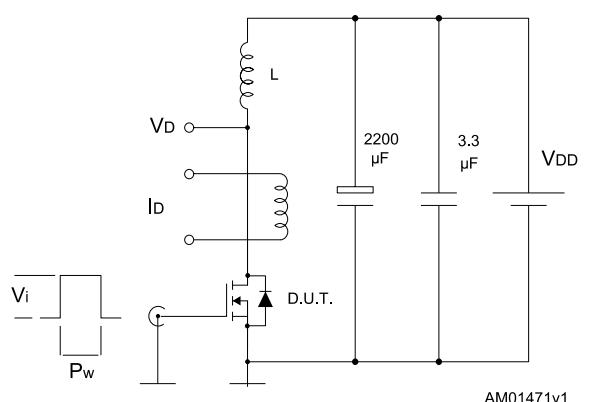
Figure 17: Unclamped inductive waveform

AM01472v1
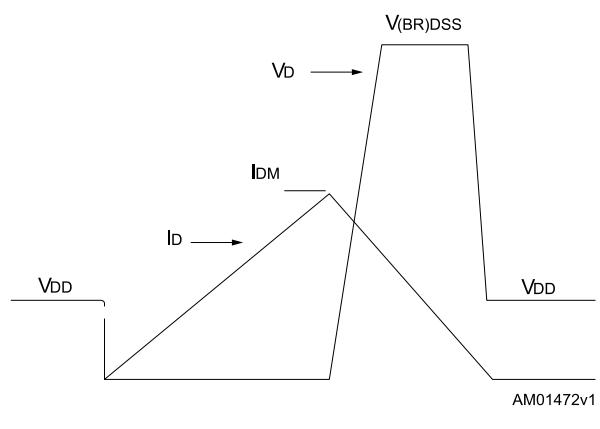
**Figure 18: Switching time waveform**

AM01473v1
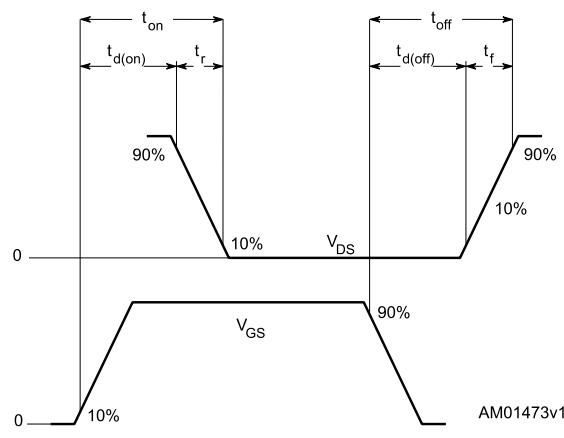
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5X6 package information

Figure 19: PowerFLAT™ 5x6 type R package outline

A0ER_8231817_Rev_10
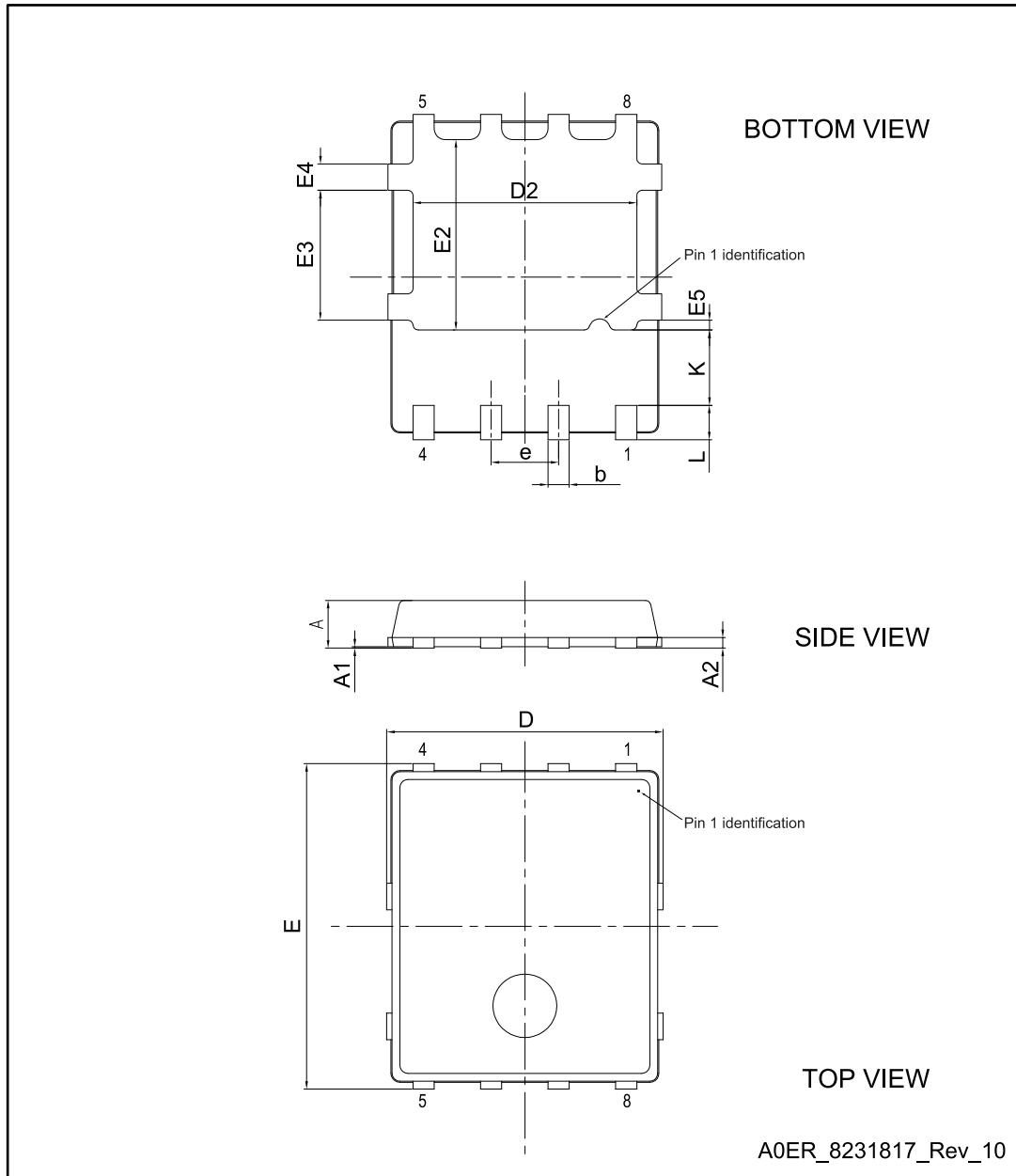
Table 8: PowerFLAT™ 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
e		1.27	
L	0.60		0.80
K	1.275		1.575
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)

8231817_FOOTPRINT_simp_Rev_10
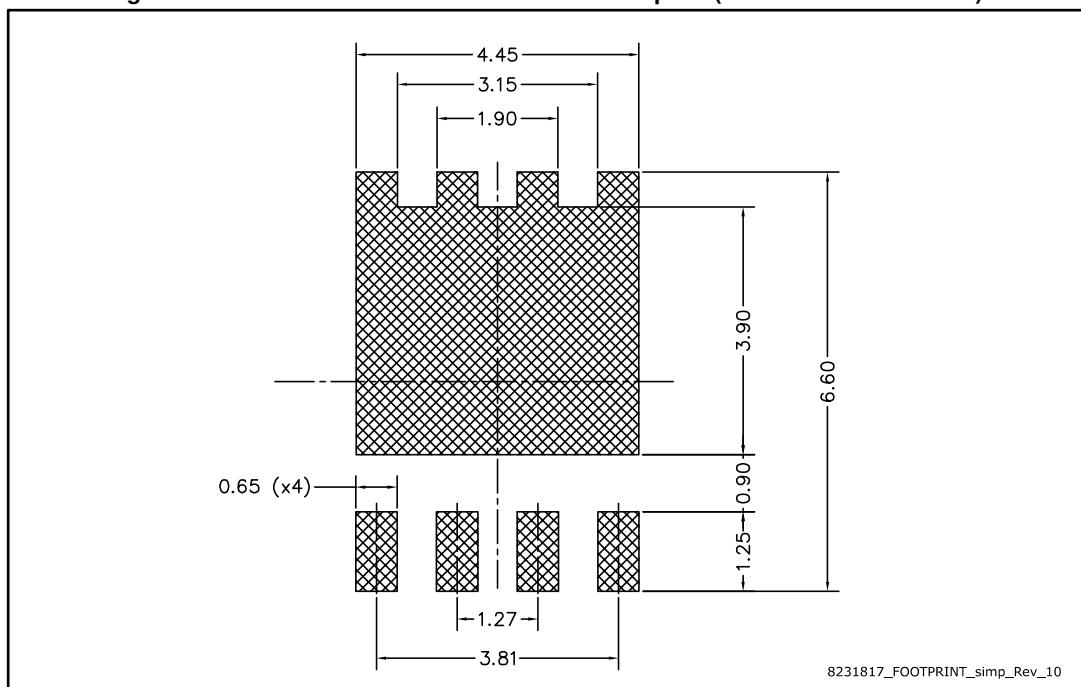
4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape outline (dimensions are in mm)

(I) Measured from centerline of sprocket hole to centerline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centerline of sprocket hole to centerline of pocket.

Base and bulk quantity 3000 pcs

8234350_Tape_rev_C
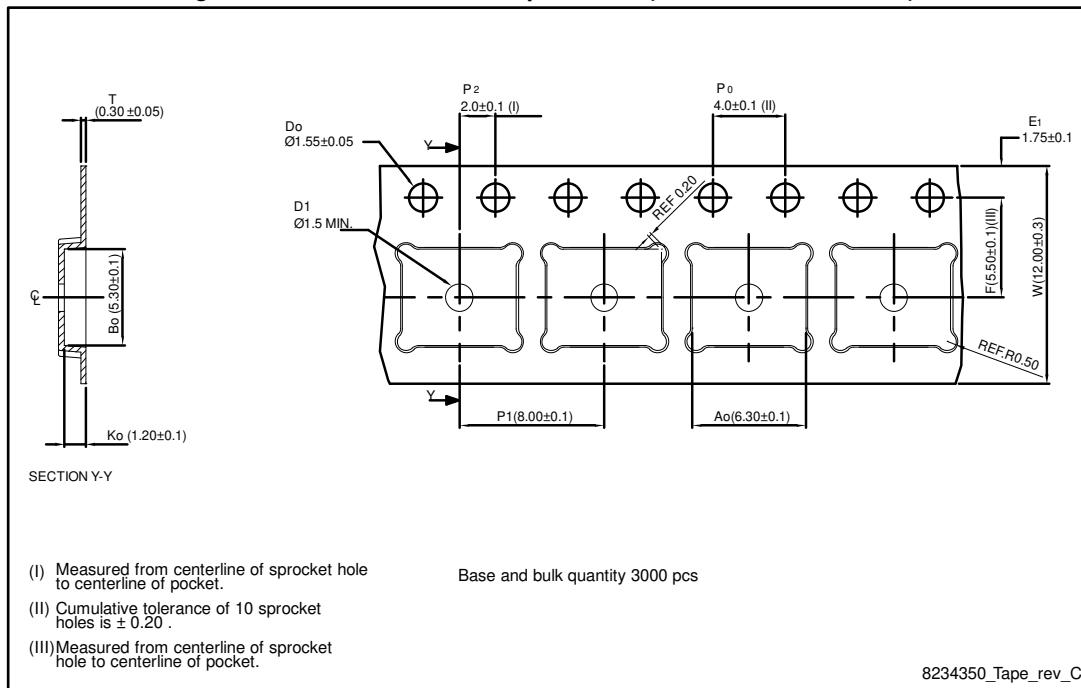
Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape
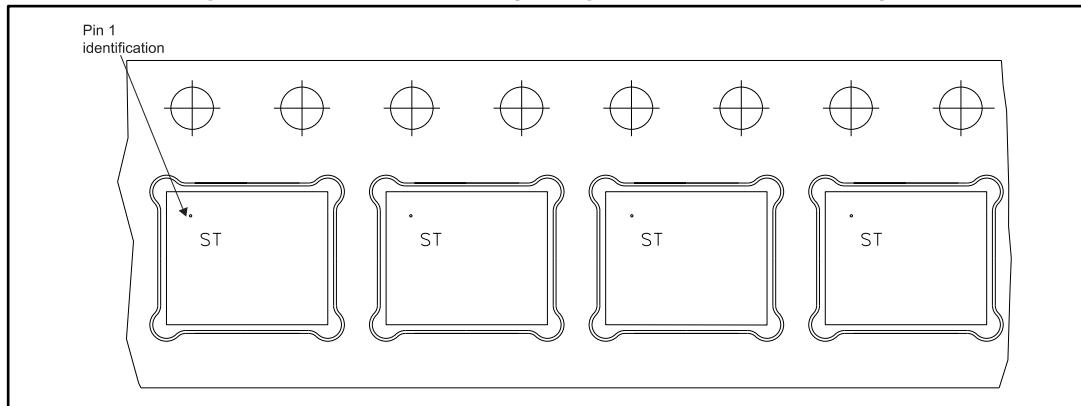
Figure 23: PowerFLAT™ 5x6 reel outline

All dimensions are in millimeters

8234350_Reel_rev_C
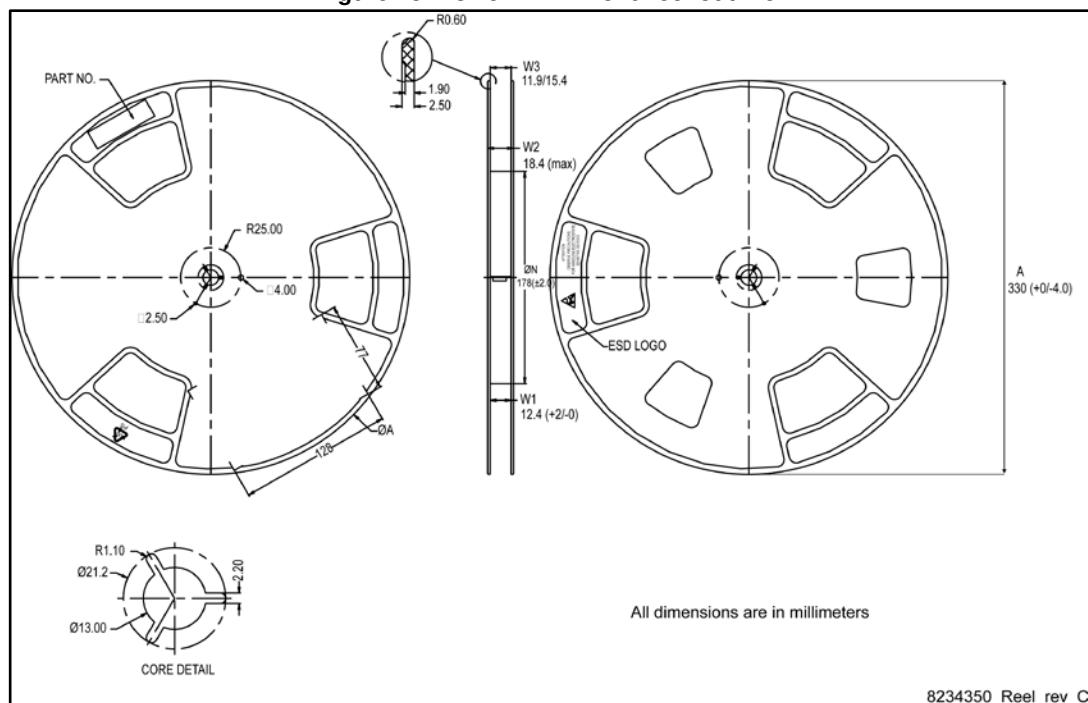
5 Revision history

Table 9: Document revision history

Date	Revision	Changes
03-Mar-2015	1	First release.
10-Jun-2015	2	In Section 2 Electrical characteristics: - updated Table 5: Dynamic - updated Table 6: Switching times - updated Table 7: Source-drain diode Added Section 2.1 Electrical characteristics (curves)

IMPORTANT NOTICE – PLEASE READ CAREFULLY