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User Guide 3.0
Hello Strata Power
LV DC-DC Ecosystem



Hello Strata Power. LV DC-DC Ecosystem. User Guide

Table of Contents

1.	INTRODUCTION.....	3
2.	DESIGN OVERVIEW	4
3.	BLOCK DIAGRAM	5
4.	SCOPE AND PURPOSE	5
5.	PREREQUISITES.....	5
6.	USER GUIDE	6
7.	USER INTERFACE.....	8
8.	SCHEMATIC MODULE EVALUATION BOARD	12

1. Introduction

The Strata low voltage DC-DC evaluation boards series is an evaluation environment for low voltage DC-DC conversion controllers, converters and regulators. The platforms are compatible with the Strata Developer Studio™, providing a Graphical User Interface for a hassle-free and fast device evaluation out of the box. Essential system variables values, such as input and output voltages, currents, power dissipation, temperatures and efficiencies are displayed and plotted on dynamic charts in real time, and can be exported as well. Load transients can be simulated with a signal generator. These Strata platforms can be used for Automotive and Industrial developments.

Features

- **Monitoring and setting of system variables via Strata GUI:**
 - Input and output voltages
 - Input and output currents
 - Power dissipation
 - Switching frequency
 - PWM adjustment
- **Load transient** generation from GUI
- **Fast evaluation with Strata Developer Studio**
- **Hardware**
 - Spacious layout with multiple test points for measurement
 - Operating temperature -40°C or +125°C

Applications

- Audio
- Infotainment
- Vision System
- Instrumentation
- Automotive low voltage DC-DC converters
- ADAS, Infotainment power management.
- Industrial imaging power management
- Industrial low voltage DC-DC conversion

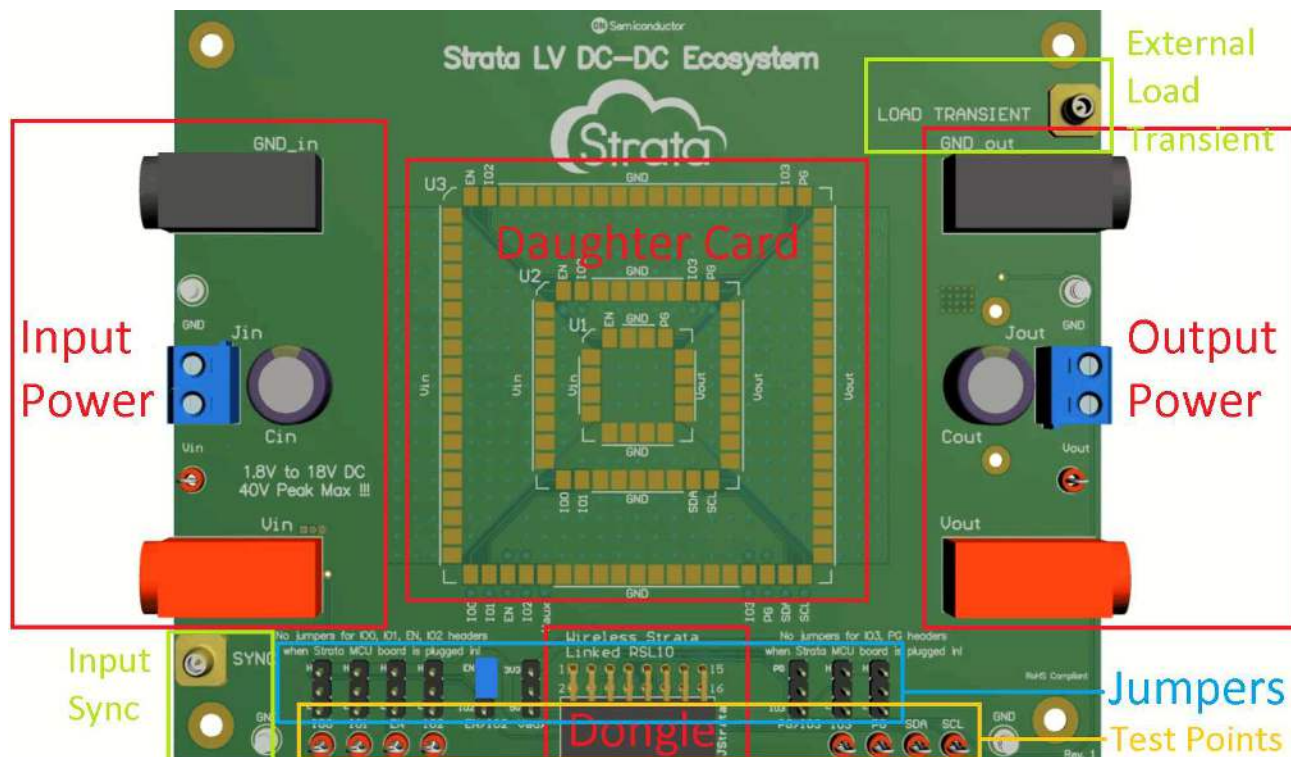
Benefits

- Out of the box and fast evaluation and characterization of DC-DC ICs
- Speeds up development cycles and reduces time-to-market.
- All related collateral available at Strata Developer Studio™
- AEC-Q qualified parts

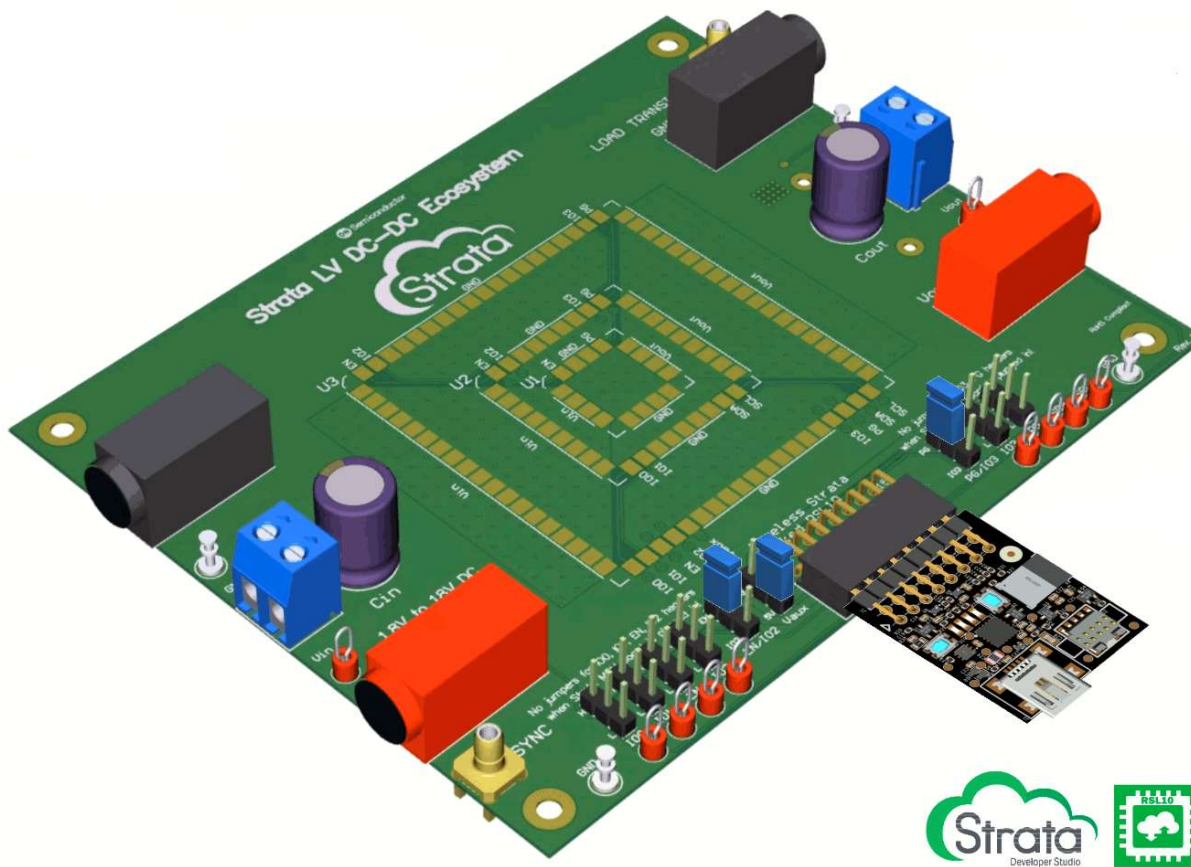
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2. Design Overview

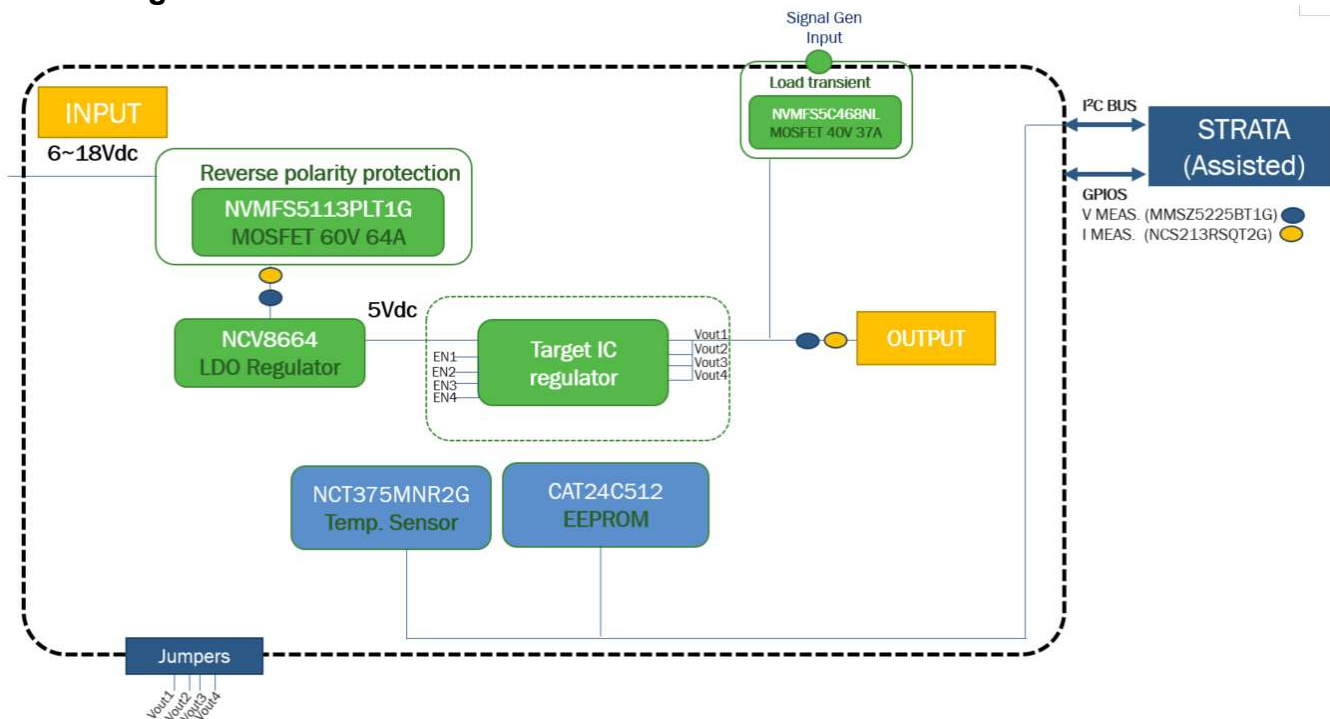
2D View



3D View



3. Block Diagram



4. Scope and Purpose

This user guide provides practical guidelines for using the Strata Low Voltage Ecosystem evaluation boards series. The design was tested as described in this document but not qualified regarding safety requirements or manufacturing and operation over the whole operating temperature range or lifetime. The development board has been layout in a spacious manner so that it facilitates measurements and probing for the evaluation of the system and its components. The hardware is intended for functional testing under laboratory conditions and by trained specialists only.

5. Prerequisites

Hardware

- Strata Low Voltage Ecosystem evaluation boards series – (Strata Low Voltage Ecosystem evaluation kit consists of mother board + daughter card)
- Strata RSL10 Assisted Dongle
- External DC power supply

Software

[Strata Developer Studio™](http://onsemi.com)

6. User Guide

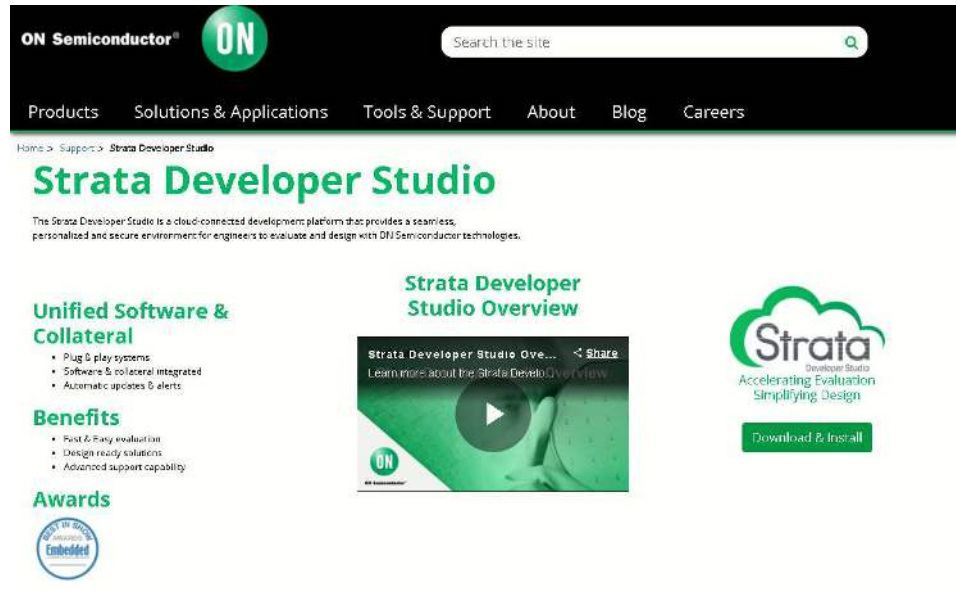
This section will explain how to use in a step by step manner the platform, and will cover both the hardware required as well as how to use the User Interface in Strata.

Hardware Setup

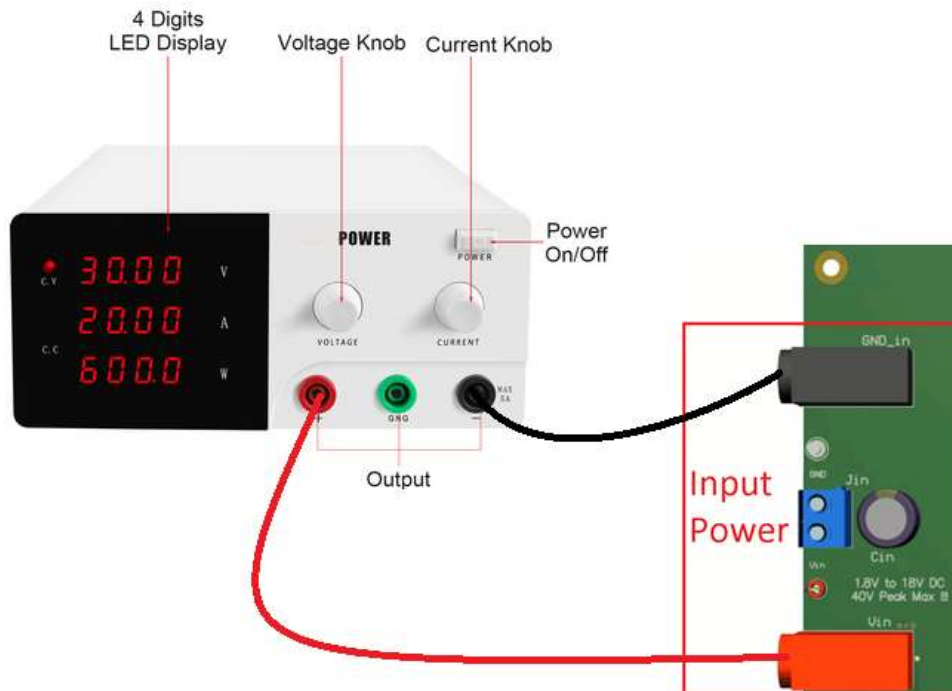
The hardware required for using the platform are a computer (with Windows) and a power supply. Follow the steps below.

1. Download and install the newest Strata Developer Studio:

[Strata Developer Studio™](#)



2. Plug the power supply into the input of the board using the banana plugs **V_{in}** and **GND_{in}**. Do not apply over 5V to the input and limit the output current to 1 Amps.

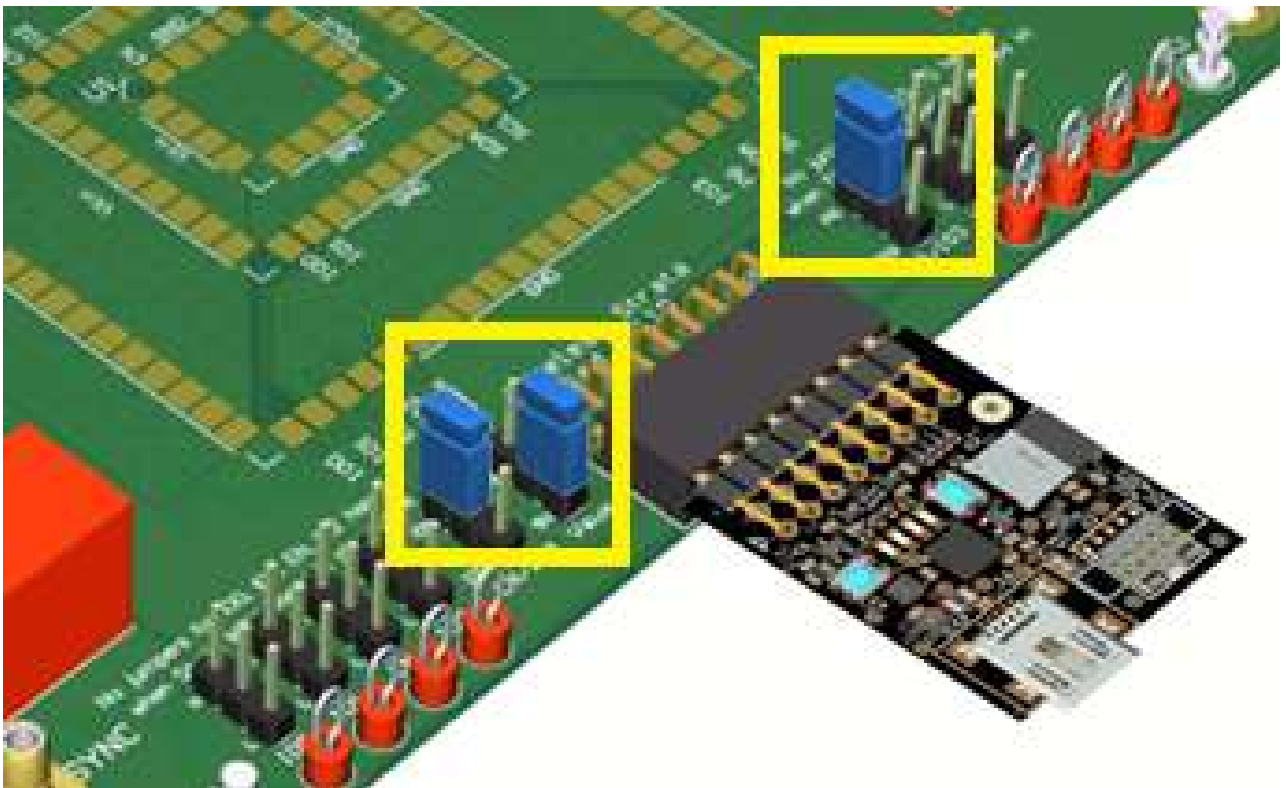


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3. Connect the computer to the **RSL10 Assisted Dongle** using the **mini USB** connector and the **RSL10 Assisted Dongle** to the **Hello Strata LV DC-DC Ecosystem**.



4. Make sure that ALL jumpers are present.



7. User Interface

The UI within the Strata app will allow the user to control the Hello Strata LV DC-DC Ecosystem platform and monitor its telemetry without needing other lab equipment or training to do so. The steps below cover what is in the UI.

1. Open Strata and Login, if necessary Register with your email and Password and Login



2. The view that comes up automatically when you plug in the mini USB is the basic view, which offers basic telemetry, an enable switch for enabling /disabling the switcher.

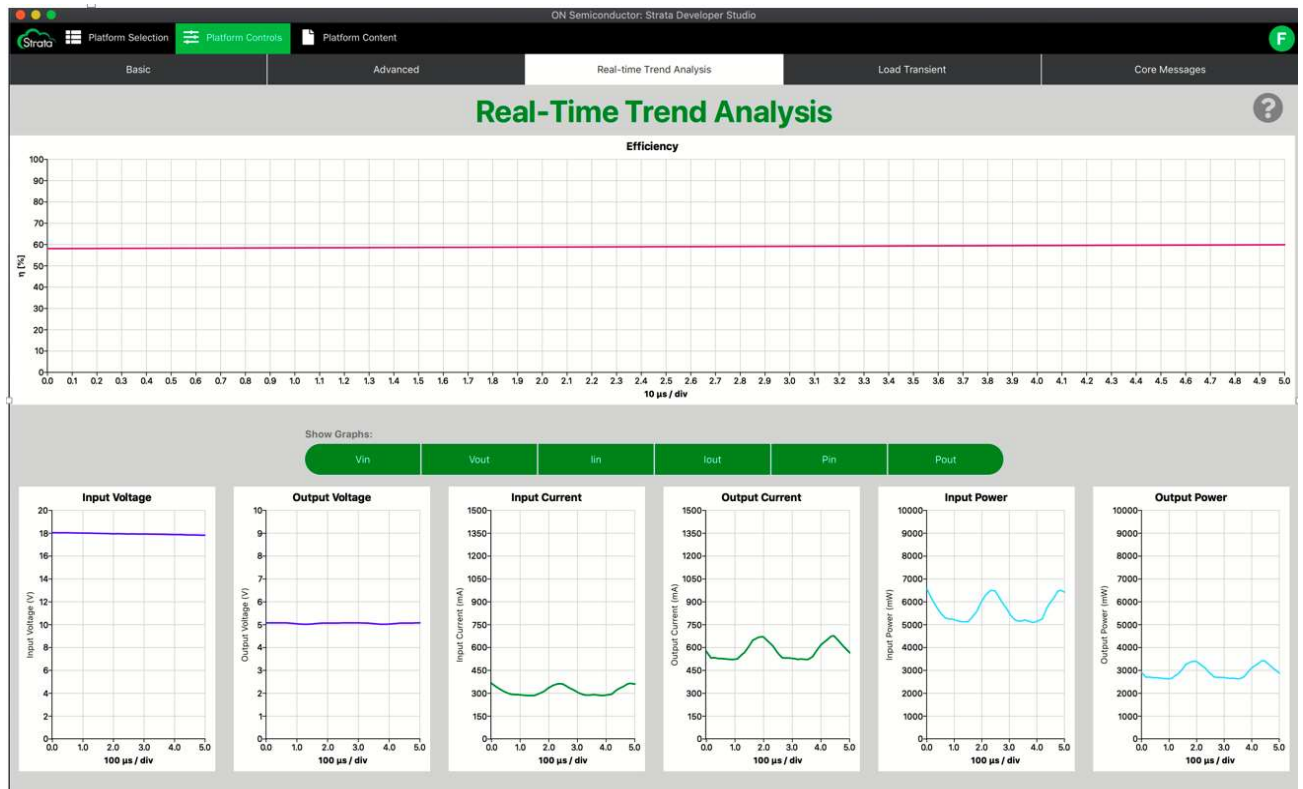


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3. In the top right hand corner the user can switch to the Advanced view. The Advanced view offers more telemetry for the user to monitor, along with many more controls.

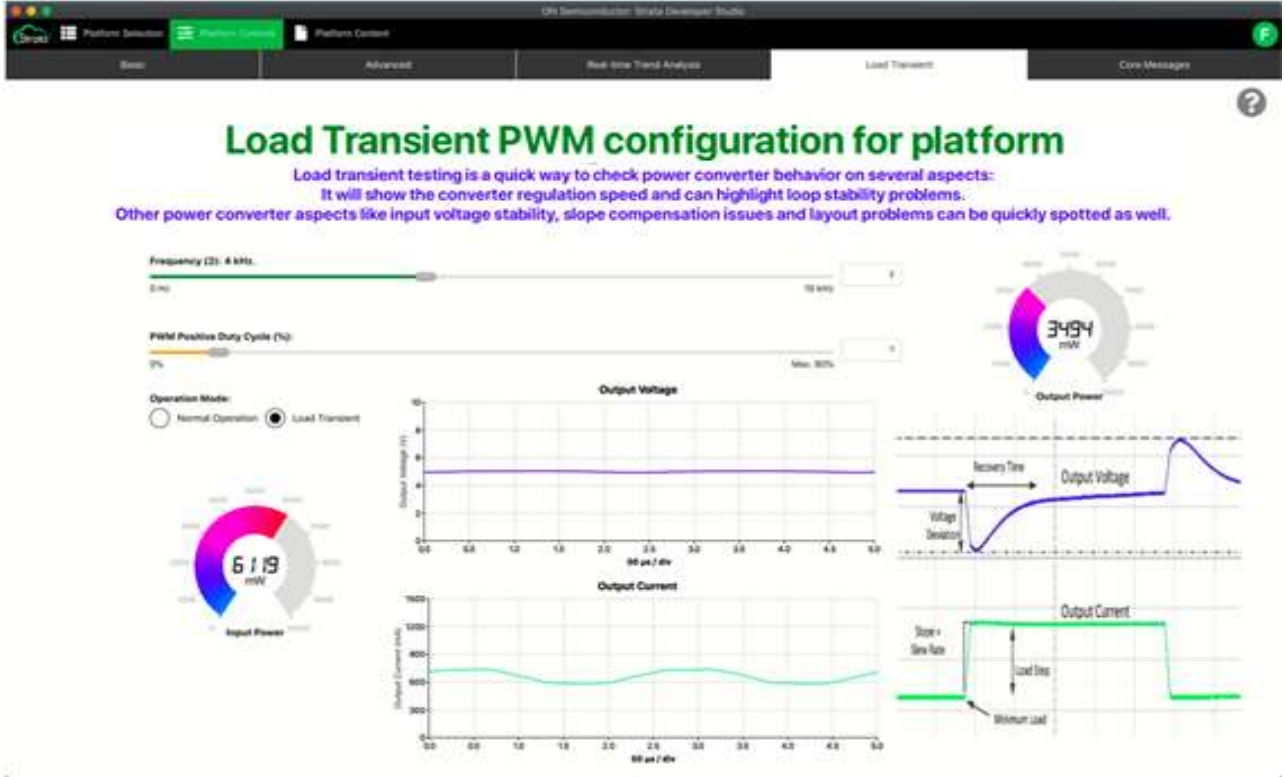


4. Real-Time Trend Analysis: The graph is displayed in below when tab menu is selected. The graph is hidden when tab menu is deselected.



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- The load is controlled from the GUI: We don't need an external electronic load. Please note, only power supply is required.



- Core Control Interface provides the ability to capture notification serial data easily for subsequent analysis and debugging. Every action is logged with all relevant data, which allows users to bring data directly into the cells of an Excel spreadsheet.

Message notifications coming from CoreInterface

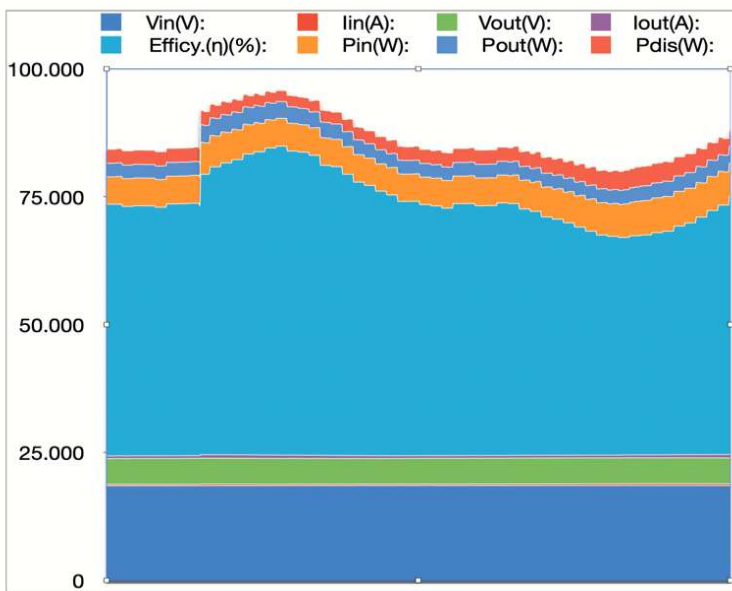
Data Acquisition Clear Data

PID	Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficacy (%)	Temp (°C)	Transient	Freq	Duty (%)	Pin(W)	Pout(W)	Pdis(W)
186: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.976
187: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.866
188: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.866
189: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.866
190: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.866
191: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.866
192: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.866
193: (PID)	18.400	0.354	4.970	0.734	55.042	42	false	0	0	6.514	3.648	2.866
194: (PID)	18.400	0.354	4.970	0.734	56.006	42	false	0	0	6.514	3.648	2.866
195: (PID)	18.400	0.354	4.970	0.734	56.006	42	false	0	0	6.514	3.648	2.866
196: (PID)	18.400	0.354	4.970	0.734	56.006	42	false	0	0	6.514	3.648	2.866
197: (PID)	18.400	0.354	4.970	0.734	56.006	42	false	0	0	6.514	3.648	2.866
198: (PID)	18.400	0.354	4.970	0.734	56.006	42	false	0	0	6.514	3.648	2.866
199: (PID)	18.400	0.348	4.970	0.734	56.006	42	false	0	0	6.514	3.648	2.866
200: (PID)	18.400	0.348	4.970	0.734	56.006	42	false	0	0	6.403	3.648	2.866
201: (PID)	18.400	0.348	4.970	0.734	56.006	42	false	0	0	6.403	3.648	2.755
202: (PID)	18.400	0.348	4.960	0.734	56.006	42	false	0	0	6.403	3.648	2.755
203: (PID)	18.400	0.348	4.960	0.734	56.006	42	false	0	0	6.403	3.641	2.755
204: (PID)	18.400	0.348	4.960	0.734	56.006	42	false	0	0	6.403	3.641	2.762
205: (PID)	18.400	0.348	4.960	0.731	56.006	42	false	0	0	6.403	3.641	2.762
206: (PID)	18.400	0.348	4.960	0.731	56.006	42	false	0	0	6.403	3.626	2.762
207: (PID)	18.400	0.348	4.960	0.731	56.006	42	false	0	0	6.403	3.626	2.777
208: (PID)	18.400	0.348	4.960	0.731	56.624	42	false	0	0	6.403	3.626	2.777
209: (PID)	18.400	0.348	4.960	0.731	56.624	42	false	0	0	6.403	3.626	2.777
210: (PID)	18.390	0.348	4.960	0.731	56.624	42	false	0	0	6.403	3.626	2.777
211: (PID)	18.390	0.348	4.960	0.731	56.624	42	false	0	0	6.400	3.626	2.777
212: (PID)	18.390	0.348	4.960	0.731	56.624	42	false	0	0	6.400	3.626	2.774
213: (PID)	18.390	0.342	4.960	0.731	56.624	42	false	0	0	6.400	3.626	2.774
214: (PID)	18.390	0.342	4.960	0.731	56.624	42	false	0	0	6.289	3.626	2.774
215: (PID)	18.390	0.342	4.960	0.731	56.624	42	false	0	0	6.289	3.626	2.663
216: (PID)	18.390	0.342	4.950	0.731	56.624	42	false	0	0	6.289	3.626	2.663
217: (PID)	18.390	0.342	4.950	0.731	56.624	42	false	0	0	6.289	3.618	2.663
218: (PID)	18.390	0.342	4.950	0.731	56.624	42	false	0	0	6.289	3.618	2.671
219: (PID)	18.390	0.342	4.950	0.728	56.624	42	false	0	0	6.289	3.618	2.671
220: (PID)	18.390	0.342	4.950	0.728	56.624	42	false	0	0	6.289	3.604	2.671
221: (PID)	18.390	0.342	4.950	0.728	56.624	42	false	0	0	6.289	3.604	2.685
222: (PID)	18.390	0.342	4.950	0.728	57.297	42	false	0	0	6.289	3.604	2.685
223: (PID)	18.390	0.342	4.950	0.728	57.297	42	false	0	0	6.289	3.604	2.685

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Table 1

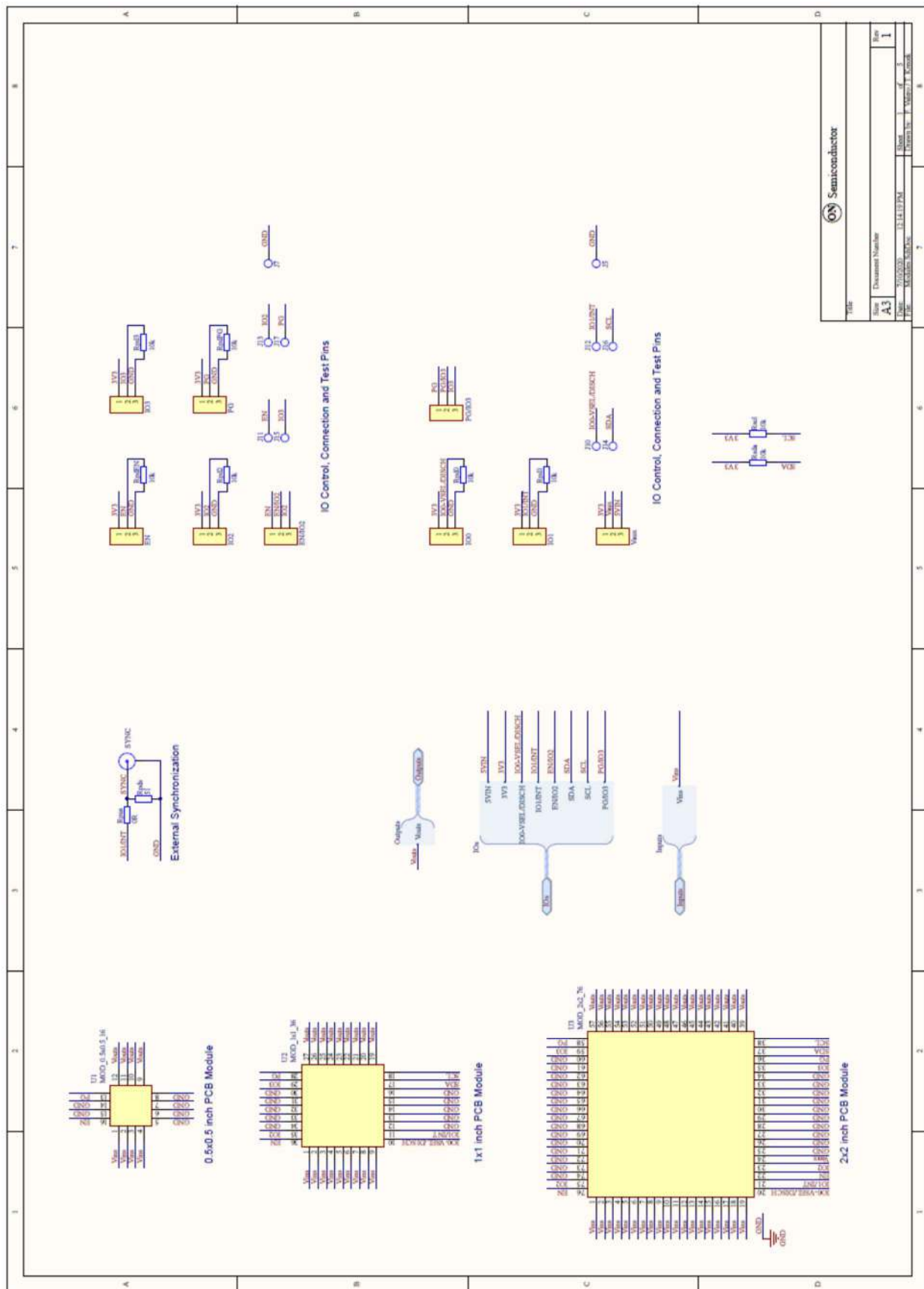
Vin(V):	Iin(A):	Vout(V):	Iout(A):	Efficy.(η)(%)	Pin(W):	Pout(W):	Pdis(W):
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.480	291	5.040	525	49.203	5.378	2.646	2.732
18.490	291	5.040	525	49.203	5.378	2.646	2.732
18.490	291	5.040	525	49.203	5.381	2.646	2.732
18.490	291	5.040	525	49.203	5.381	2.646	2.735
18.490	294	5.040	525	49.203	5.436	2.646	2.735
18.490	294	5.040	525	49.203	5.436	2.646	2.790
18.490	294	5.050	525	49.203	5.436	2.646	2.790
18.490	294	5.050	525	49.203	5.436	2.651	2.790
18.490	294	5.050	525	49.203	5.436	2.651	2.785
18.490	294	5.050	525	49.203	5.436	2.651	2.785
18.490	294	5.050	525	49.203	5.436	2.651	2.785
18.490	294	5.050	525	48.772	5.436	2.651	2.785
18.490	294	5.050	525	48.772	5.436	2.651	2.785
18.480	294	5.050	525	48.772	5.433	2.651	2.785
18.480	294	5.050	525	48.772	5.433	2.651	2.782
18.480	294	5.050	525	48.772	5.433	2.651	2.782
18.480	294	5.050	525	48.772	5.433	2.651	2.782
18.480	294	5.060	525	48.772	5.433	2.651	2.782
18.480	294	5.060	525	48.772	5.433	2.656	2.782
18.480	294	5.060	525	48.772	5.433	2.656	2.777
18.480	294	5.060	525	48.772	5.433	2.656	2.777
18.480	294	5.060	525	48.772	5.433	2.656	2.777
18.480	294	5.060	525	48.772	5.433	2.656	2.777
18.480	294	5.060	525	48.895	5.433	2.656	2.777
18.480	294	5.060	525	48.895	5.433	2.656	2.777
18.490	294	5.060	525	48.895	5.436	2.656	2.780
18.490	294	5.060	525	48.895	5.436	2.656	2.780
18.490	294	5.060	525	48.895	5.436	2.656	2.780
18.490	294	5.060	525	48.895	5.436	2.656	2.780
18.490	294	5.060	525	48.895	5.436	2.656	2.780
18.490	294	5.060	525	48.895	5.436	2.656	2.780
18.490	294	5.060	525	48.895	5.436	2.656	2.780
18.490	294	5.060	525	48.868	5.436	2.656	2.780
18.490	294	5.060	525	48.868	5.436	2.656	2.780
18.490	294	5.060	525	48.868	5.436	2.656	2.780
18.490	294	5.060	525	48.868	5.436	2.656	2.780

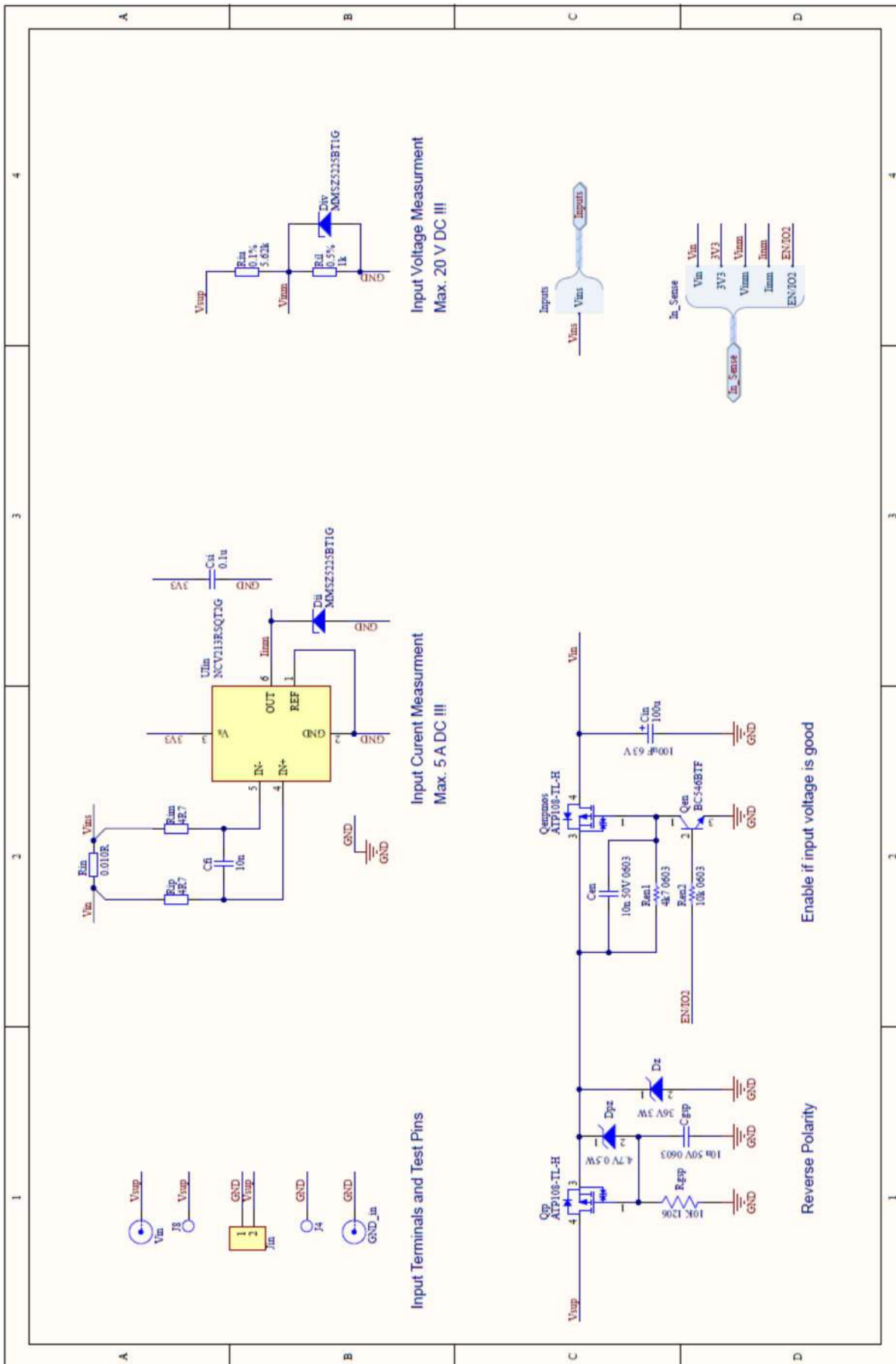


7. To look at the collateral provided with the EVB, click on the “Platform Content” tab at the top of the screen.

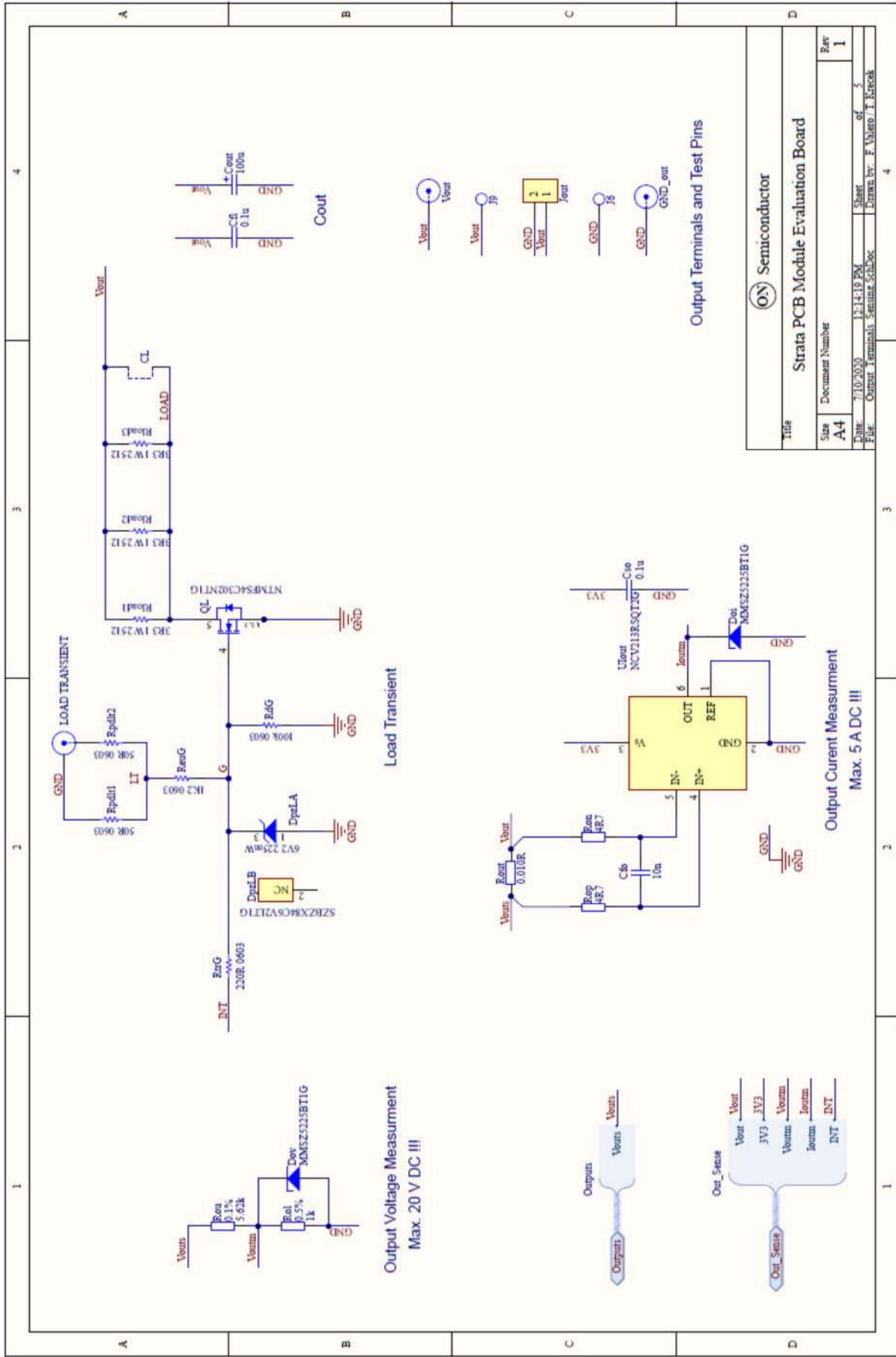


8. Schematic Module Evaluation Board

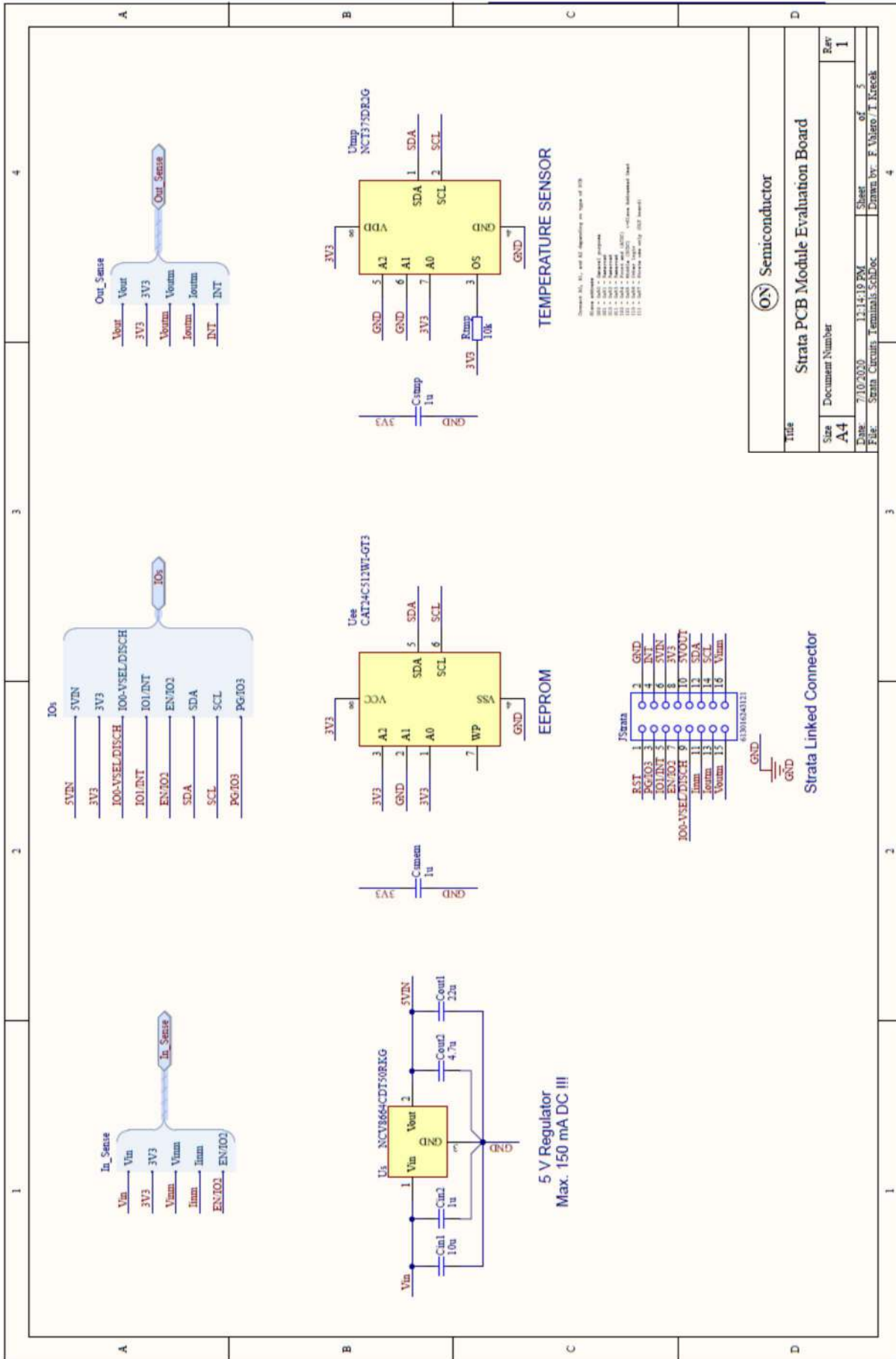


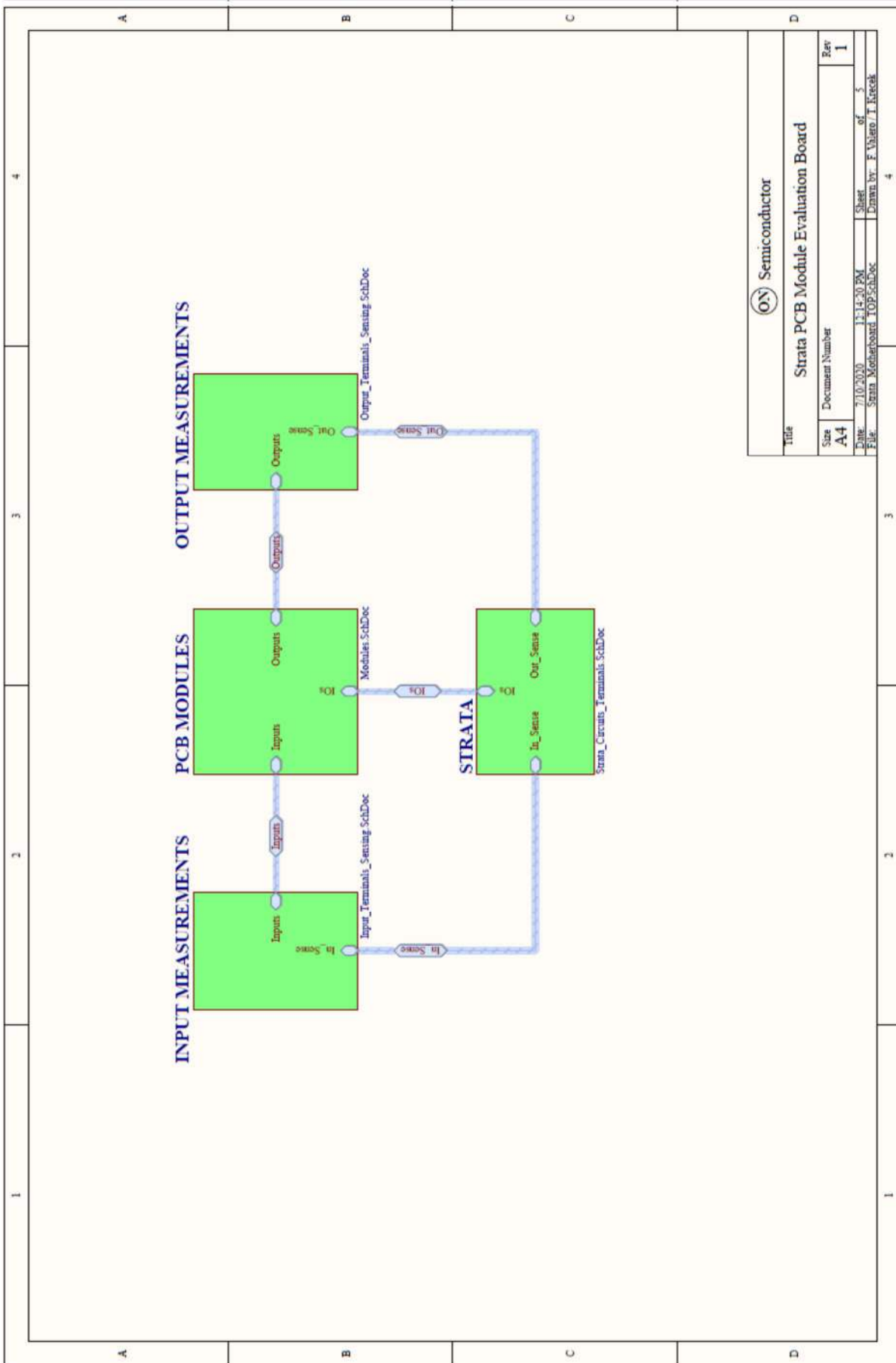


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Title Strata PCB Module Evaluation Board	
Size A4	Document Number
Date 7/10/2010 12:14:20 PM	Rev 1
File Strata_Motherboard_TOP.SchDoc	Sheet 5 of 5
Drawn by: F. Valero / T. Kreck	

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