19-3034; Rev 0; 10/03

MAXIM

# Dual-Phase, Parallelable, Average-Current-Mode Controllers



## General Description

The MAX5038A/MAX5041A dual-phase, PWM controllers provide high-output-current capability in a compact package with a minimum number of external components. The MAX5038A/MAX5041A utilize a dual-phase, average-current-mode control that enables optimal use of low $R_{DS(ON)}$ MOSFETs, eliminating the need for external heatsinks even when delivering high output currents.

Differential sensing enables accurate control of the output voltage, while adaptive voltage positioning provides optimum transient response. An internal regulator enables operation with input voltage ranges of +4.75V to +5.5V or +8V to +28V. The high switching frequency, up to 500kHz per phase, and dual-phase operation allow the use of low-output inductor values and input capacitor values. This accommodates the use of PC board-embedded planar magnetics achieving superior reliability, current sharing, thermal management, compact size, and low system cost.

The MAX5038A/MAX5041A also feature a clock input (CLKIN) for synchronization to an external clock, and a clock output (CLKOUT) with programmable phase delay (relative to CLKIN) for paralleling multiple phases. The MAX5038A/MAX5041A also limit the reverse current in case the bus voltage becomes higher than the regulated output voltage. The MAX5038A offers a variety of factory-trimmed preset output voltages (see *Selector Guide*) and the MAX5041A offers an adjustable output voltage between +1.0V to +3.3V.

The MAX5038A/MAX5041A operate over the extended temperature range (-40°C to +85°C) and are available in a 28-pin SSOP package. Refer to the MAX5037A and MAX5065/MAX5067 data sheets for a VRM 9.0/VRM 9.1-compatible, VID-controlled, adjustable output voltage controller in a 44-pin MQFP/thin QFN or 28-pin SSOP package.

## Applications

Servers and Workstations

Point-of-Load High-Current/High-Density Telecom DC-DC Regulators

Networking Systems

Large-Memory Arrays

RAID Systems

High-End Desktop Computers

## Features

- **+4.75V to +5.5V or +8V to +28V Input Voltage Range**
- **Up to 60A Output Current**
- **Internal Voltage Regulator for a +12V or +24V Power Bus**
- **True Differential Remote Output Sensing**
- **Two Out-Of-Phase Controllers Reduce Input Capacitance Requirement and Distribute Power Dissipation**
- **Average-Current-Mode Control**
  - **Superior Current Sharing Between Individual Phases and Paralleled Modules**
  - **Accurate Current Limit Eliminates MOSFET and Inductor Derating**
- **Limits Reverse-Current Sinking in Paralleled Modules**
- **Integrated 4A Gate Drivers**
- **Selectable Fixed Frequency 250kHz or 500kHz per Phase (Up to 1MHz for Two Phases)**
- **Fixed (MAX5038A) or Adjustable (MAX5041A) Output Voltages**
- **External Frequency Synchronization from 125kHz to 600kHz**
- **Internal PLL with Clock Output for Paralleling Multiple DC-DC Converters**
- **Thermal Protection**
- **28-Pin SSOP Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | OUTPUT VOLTAGE (V) |
|---|---|---|---|
| **MAX5038A**EAI12 | -40°C to +85°C | 28 SSOP | Fixed +1.2 |
| MAX5038AEAI15 | -40°C to +85°C | 28 SSOP | Fixed +1.5 |
| MAX5038AEAI18 | -40°C to +85°C | 28 SSOP | Fixed +1.8 |
| MAX5038AEAI25 | -40°C to +85°C | 28 SSOP | Fixed +2.5 |
| MAX5038AEAI33 | -40°C to +85°C | 28 SSOP | Fixed +3.3 |
| **MAX5041A**EAI | -40°C to +85°C | 28 SSOP | Adj +1.0 to +3.3 |

***Pin Configuration appears at end of data sheet.***

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

## ABSOLUTE MAXIMUM RATINGS

IN to SGND .....-0.3V to +30V
BST_ to SGND .....-0.3V to +35V
DH_ to LX_ .....-0.3V to [($V_{BST\_}$ - $V_{LX\_}$) + 0.3V]
DL_ to PGND .....-0.3V to ($V_{CC}$ + 0.3V)
BST_ to LX_ .....-0.3V to +6V
$V_{CC}$ to SGND .....-0.3V to +6V
$V_{CC}$ to PGND .....-0.3V to +6V
SGND to PGND .....-0.3V to +0.3V
All Other Pins to SGND .....-0.3V to ($V_{CC}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
28-Pin SSOP (derate 9.5mW/°C above +70°C) .....762mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +5V, circuit of Figure 1, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical specifications are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SYSTEM SPECIFICATIONS** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 8 | | 28 | V |
| | | Short IN and $V_{CC}$ together for +5V input operation | 4.75 | | 5.5 | |
| Quiescent Supply Current | $I_Q$ | EN = $V_{CC}$ or SGND | | 4 | 10 | mA |
| Efficiency | $\eta$ | $I_{LOAD}$ = 52A (26A per phase) | | 90 | | % |
| **OUTPUT VOLTAGE** | | | | | | |
| Nominal Output Voltage Accuracy (Note 4) | | MAX5038A only, no load | -0.8 | | +0.8 | % |
| | | MAX5038A only, no load, $V_{IN}$ = $V_{CC}$ = +4.75V to +5.5V or $V_{IN}$ = +8V to +28V (Note 2) | -1 | | +1 | |
| SENSE+ to SENSE- Voltage Accuracy (Note 4) | | MAX5041A only, no load | 0.992 | | 1.008 | V |
| | | MAX5041A only, no load, $V_{IN}$ = $V_{CC}$ = +4.75V to +5.5V or $V_{IN}$ = +8V to +28V | 0.990 | | 1.010 | |
| **STARTUP/INTERNAL REGULATOR** | | | | | | |
| $V_{CC}$ Undervoltage Lockout | UVLO | $V_{CC}$ rising | 4.0 | 4.15 | 4.5 | V |
| $V_{CC}$ Undervoltage Lockout Hysteresis | | | | 200 | | mV |
| $V_{CC}$ Output Accuracy | | $V_{IN}$ = +8V to +28V, $I_{SOURCE}$ = 0 to 80mA | 4.85 | 5.1 | 5.30 | V |
| **MOSFET DRIVERS** | | | | | | |
| Output Driver Impedance | $R_{ON}$ | Low or high output | | 1 | 3 | Ω |
| Output Driver Source/Sink Current | $I_{DH\_}$, $I_{DL\_}$ | | | 4 | | A |
| Nonoverlap Time | $t_{NO}$ | $C_{DH\_/DL\_}$ = 5nF | | 60 | | ns |
| **OSCILLATOR AND PLL** | | | | | | |
| Switching Frequency | $f_{SW}$ | CLKIN = SGND | 238 | 250 | 262 | kHz |
| | | CLKIN = $V_{CC}$ | 475 | 500 | 525 | |
| PLL Lock Range | $f_{PLL}$ | | 125 | | 600 | kHz |
| PLL Locking Time | $t_{PLL}$ | | | 200 | | µs |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +5V, circuit of Figure 1, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical specifications are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| CLKOUT Phase Shift (at $f_{SW}$ = 125kHz) | $\phi_{CLKOUT}$ | PHASE = $V_{CC}$ | 115 | 120 | 125 | Degrees |
| | | PHASE = unconnected | 85 | 90 | 95 | |
| | | PHASE = SGND | 55 | 60 | 65 | |
| CLKIN Input Pulldown Current | $I_{CLKIN}$ | | 3 | 5 | 7 | µA |
| CLKIN High Threshold | $V_{CLKINH}$ | | 2.4 | | | V |
| CLKIN Low Threshold | $V_{CLKINL}$ | | | | 0.8 | V |
| CLKIN High Pulse Width | $t_{CLKIN}$ | | 200 | | | ns |
| PHASE High Threshold | $V_{PHASEH}$ | | 4 | | | V |
| PHASE Low Threshold | $V_{PHASEL}$ | | | | 1 | V |
| PHASE Input Bias Current | $I_{PHASEBIA}$ | | -50 | | +50 | µA |
| CLKOUT Output Low Level | $V_{CLKOUTL}$ | $I_{SINK}$ = 2mA (Note 2) | | | 100 | mV |
| CLKOUT Output High Level | $V_{CLKOUTH}$ | $I_{SOURCE}$ = 2mA (Note 2) | 4.5 | | | V |
| **CURRENT LIMIT** | | | | | | |
| Average Current-Limit Threshold | $V_{CL}$ | CSP_ to CSN_ | 45 | 48 | 51 | mV |
| Reverse Current-Limit Threshold | $V_{CLR}$ | CSP_ to CSN_ | -3.9 | | -0.2 | mV |
| Cycle-by-Cycle Current Limit | $V_{CLPK}$ | CSP_ to CSN_ (Note 3) | 90 | 112 | 130 | mV |
| Cycle-by-Cycle Overload Response Time | $t_R$ | $V_{CSP\_}$ to $V_{CSN\_}$ = +150mV | | 260 | | ns |
| **CURRENT-SENSE AMPLIFIER** | | | | | | |
| CSP_ to CSN_ Input Resistance | $R_{CS\_}$ | | | 4 | | kΩ |
| Common-Mode Range | $V_{CMR(CS)}$ | | -0.3 | | +3.6 | V |
| Input Offset Voltage | $V_{OS(CS)}$ | | -1 | | +1 | mV |
| Amplifier Gain | $A_{V(CS)}$ | | | 18 | | V/V |
| 3dB Bandwidth | $f_{3dB}$ | | | 4 | | MHz |
| **CURRENT-ERROR AMPLIFIER (TRANSCONDUCTANCE AMPLIFIER)** | | | | | | |
| Transconductance | $gm_{ca}$ | | | 550 | | µS |
| Open-Loop Gain | $A_{VOL(CE)}$ | No load | | 50 | | dB |
| **DIFFERENTIAL VOLTAGE AMPLIFIER (DIFF)** | | | | | | |
| Common-Mode Voltage Range | $V_{CMR(DIFF)}$ | | -0.3 | | +1.0 | V |
| DIFF Output Voltage | $V_{CM}$ | $V_{SENSE+}$ = $V_{SENSE-}$ = 0 | | 0.6 | | V |
| Input Offset Voltage | $V_{OS(DIFF)}$ | | -1 | | +1 | mV |
| Amplifier Gain | $A_{V(DIFF)}$ | MAX5038A (+1.2V, +1.5V, +1.8V output versions), MAX5041A | 0.997 | 1 | 1.003 | V/V |
| | | MAX5038A (+2.5V and +3.3V output versions) | 0.495 | 0.5 | 0.505 | |
| 3dB Bandwidth | $f_{3dB}$ | $C_{DIFF}$ = 20pF | | 3 | | MHz |
| Minimum Output Current Drive | $I_{OUT(DIFF)}$ | | 1.0 | | | mA |
| SENSE+ to SENSE- Input Resistance | $R_{VS\_}$ | | 50 | 100 | | kΩ |

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +5V, circuit of Figure 1, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical specifications are at $T_A$ = +25°C.) (Note 1)

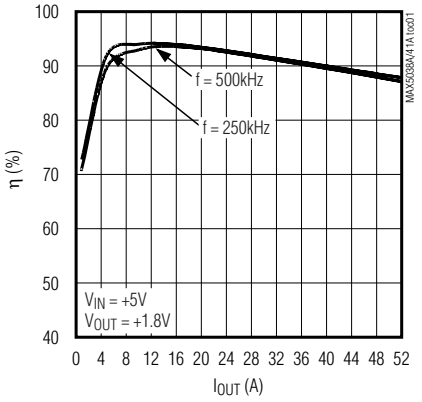
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **VOLTAGE-ERROR AMPLIFIER (EAOUT)** | | | | | | |
| Open-Loop Gain | $A_{VOL(EA)}$ | | | 70 | | dB |
| Unity-Gain Bandwidth | $f_{UGEA}$ | | | 3 | | MHz |
| EAN Input Bias Current | $I_{B(EA)}$ | $V_{EAN}$ = +2.0V | -100 | | +100 | nA |
| Error-Amplifier Output Clamping Voltage | $V_{CLAMP(EA)}$ | With respect to $V_{CM}$ | 810 | | 918 | mV |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown | $T_{SHDN}$ | | | 150 | | °C |
| Thermal-Shutdown Hysteresis | | | | 8 | | °C |
| **EN INPUT** | | | | | | |
| EN Input Low Voltage | $V_{ENL}$ | | | | 1 | V |
| EN Input High Voltage | $V_{ENH}$ | | 3 | | | V |
| EN Pullup Current | $I_{EN}$ | | 4.5 | 5 | 5.5 | µA |

**Note 1:** Specifications from -40°C to 0°C are guaranteed by characterization but not production tested.
**Note 2:** Guaranteed by design. Not production tested.
**Note 3:** See *Peak-Current Comparator* section.
**Note 4:** Does not include an error due to finite error amplifier gain (see the *Voltage-Error Amplifier* section).

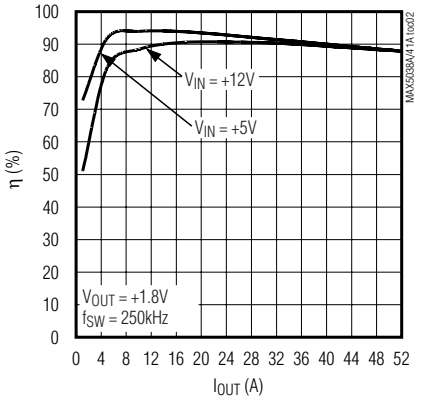
## Typical Operating Characteristics

(Circuit of Figure 1. $T_A$ = +25°C, unless otherwise noted.)

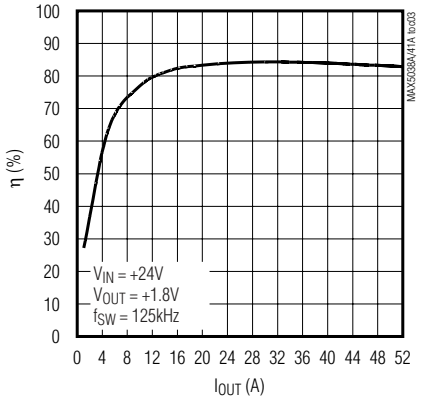
**EFFICIENCY vs. OUTPUT CURRENT AND INTERNAL OSCILLATOR FREQUENCY**



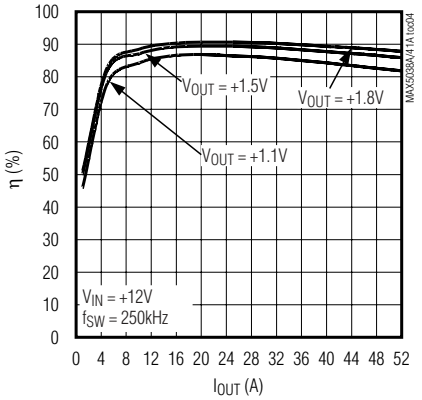

**EFFICIENCY vs. OUTPUT CURRENT AND INPUT VOLTAGE**



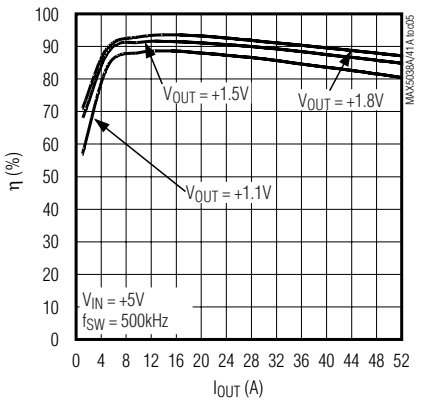

**EFFICIENCY vs. OUTPUT CURRENT**



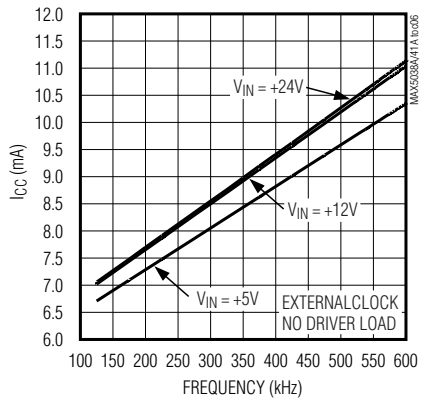

**EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE**



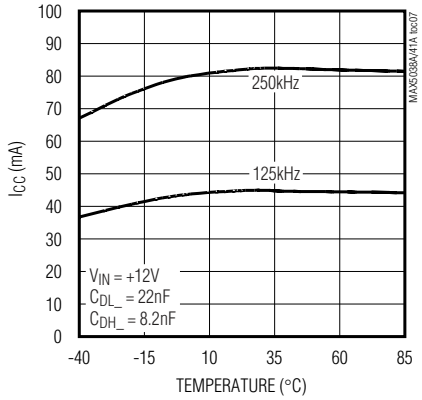

**EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE**



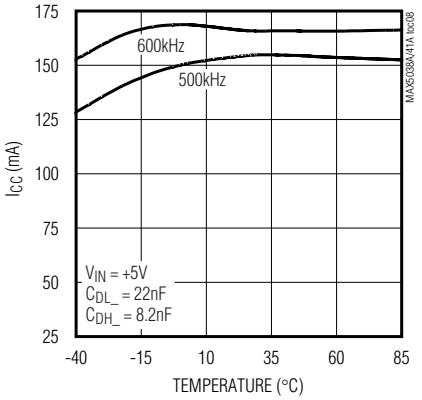

**SUPPLY CURRENT vs. FREQUENCY AND INPUT VOLTAGE**



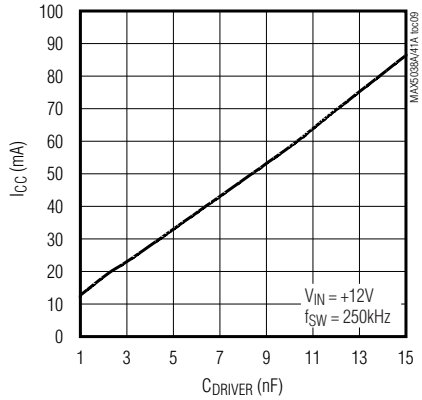

**SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY**




**SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY**




**SUPPLY CURRENT vs. LOAD CAPACITANCE PER DRIVER**

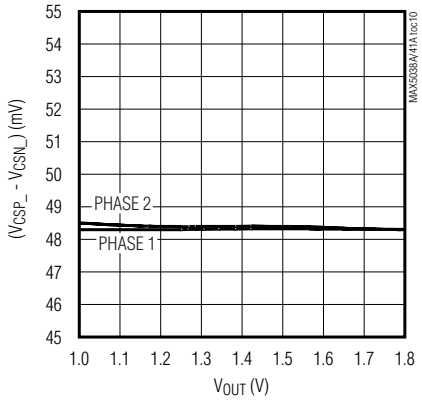


# Dual-Phase, Parallelable, Average-Current-Mode Controllers

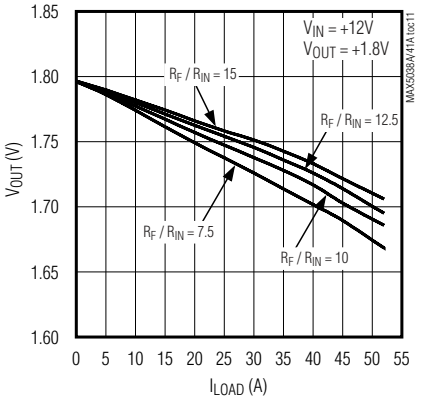
## Typical Operating Characteristics (continued)

(Circuit of Figure 1, $T_A$ = +25°C, unless otherwise noted.)

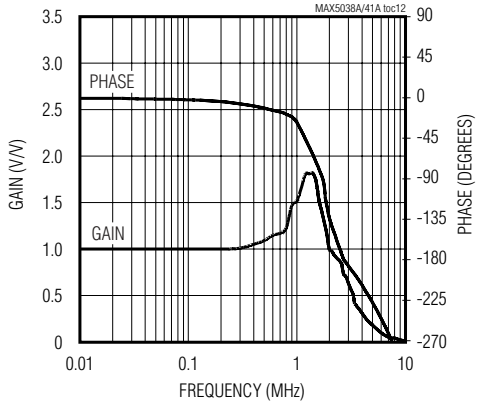
**CURRENT-SENSE THRESHOLD vs. OUTPUT VOLTAGE**



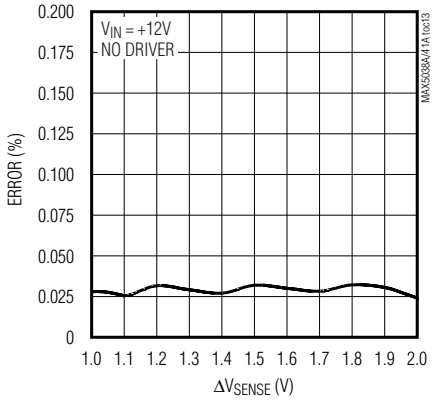

**OUTPUT VOLTAGE vs. OUTPUT CURRENT AND ERROR AMP GAIN ($R_F$ / $R_{IN}$)**



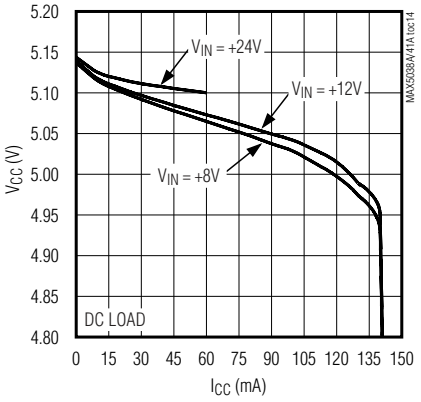

**DIFFERENTIAL AMPLIFIER BANDWIDTH**



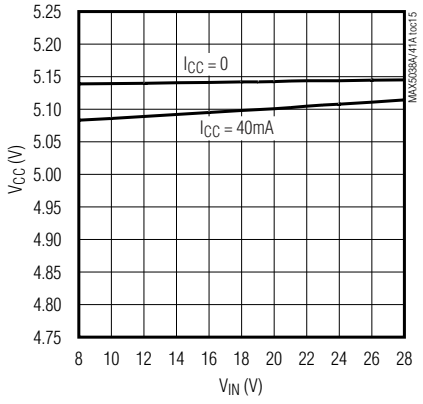

**DIFF OUTPUT ERROR vs. SENSE+ TO SENSE- VOLTAGE**



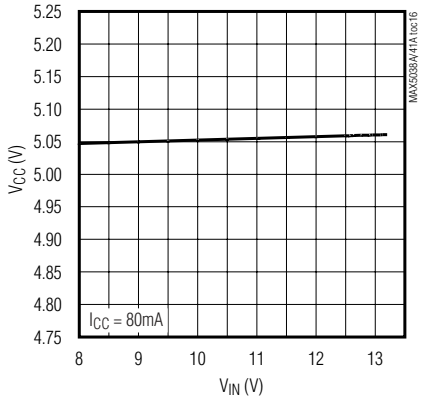

**VCC LOAD REGULATION vs. INPUT VOLTAGE**



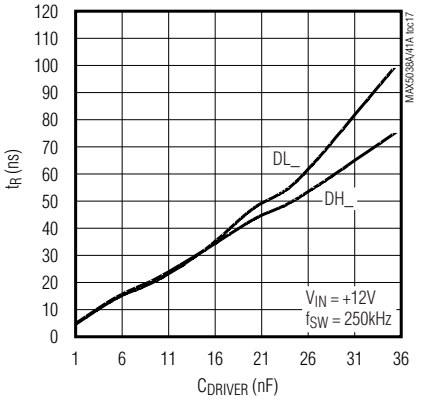

**VCC LINE REGULATION**



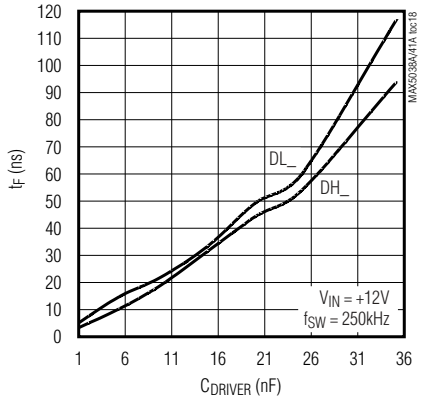

**VCC LINE REGULATION**




**DRIVER RISE TIME vs. DRIVER LOAD CAPACITANCE**



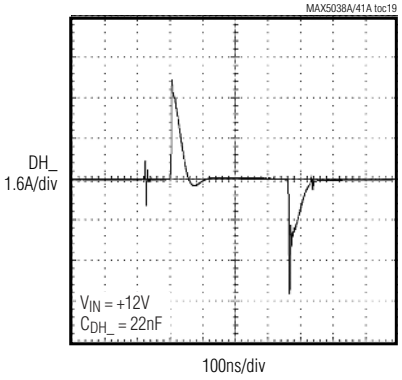

**DRIVER FALL TIME vs. DRIVER LOAD CAPACITANCE**



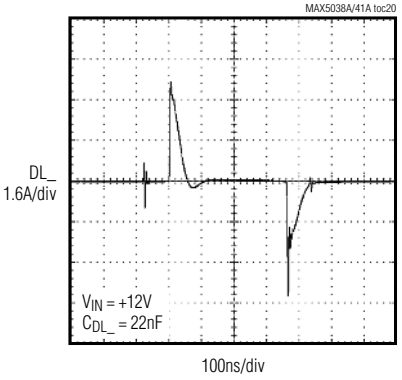
## Typical Operating Characteristics (continued)

(Circuit of Figure 1, $T_A$ = +25°C, unless otherwise noted.)

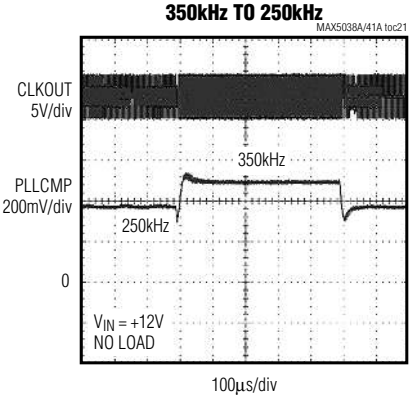
**HIGH-SIDE DRIVER (DH_) SINK AND SOURCE CURRENT**



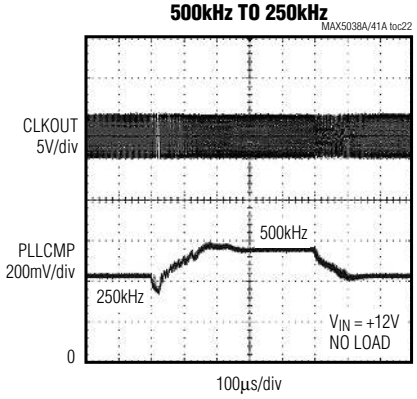

**LOW-SIDE DRIVER (DL_) SINK AND SOURCE CURRENT**



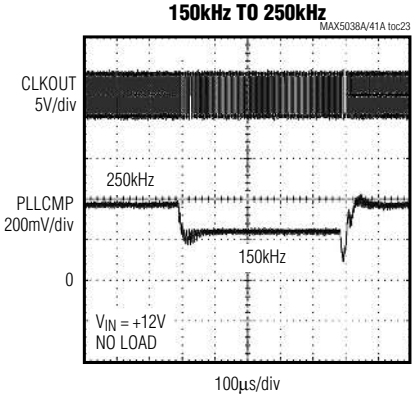

**PLL LOCKING TIME 250kHz TO 350kHz AND 350kHz TO 250kHz**



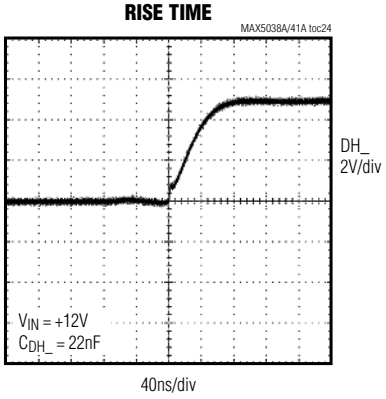

**PLL LOCKING TIME 250kHz TO 500kHz AND 500kHz TO 250kHz**



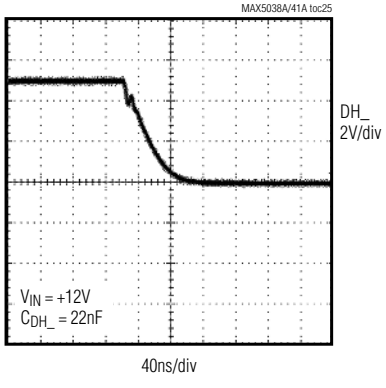

**PLL LOCKING TIME 250kHz TO 150kHz AND 150kHz TO 250kHz**



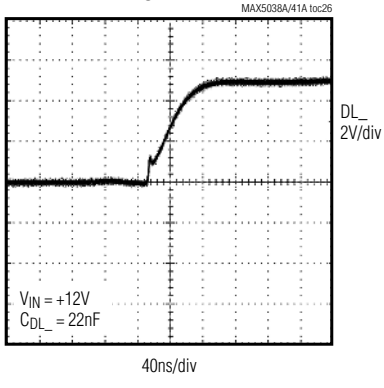

**HIGH-SIDE DRIVER (DH_) RISE TIME**



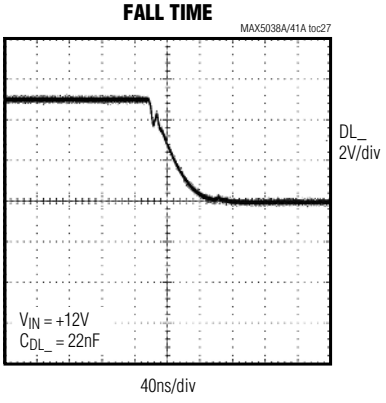

**HIGH-SIDE DRIVER (DH_) FALL TIME**




**LOW-SIDE DRIVER (DL_) RISE TIME**




**LOW-SIDE DRIVER (DL_) FALL TIME**

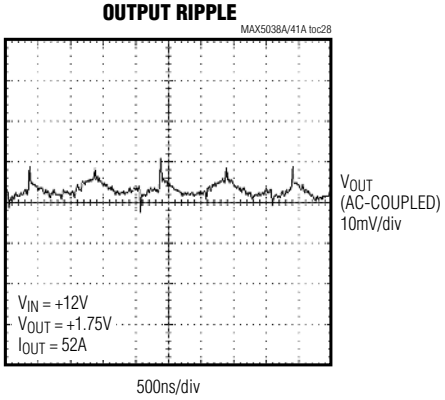


# Dual-Phase, Parallelable, Average-Current-Mode Controllers

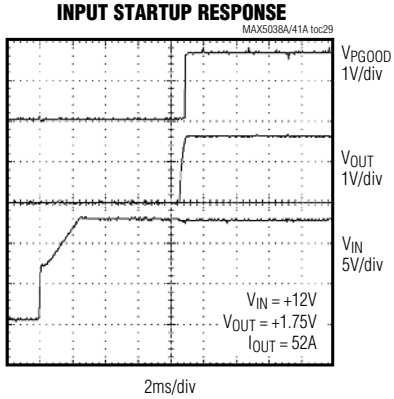
## Typical Operating Characteristics (continued)

(Circuit of Figure 1, $T_A$ = +25°C, unless otherwise noted.)

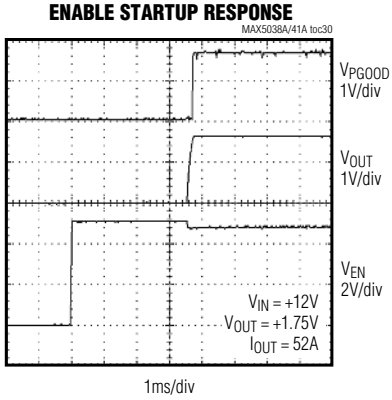
**OUTPUT RIPPLE**



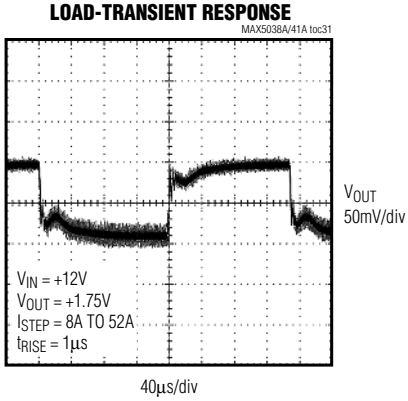

**INPUT STARTUP RESPONSE**



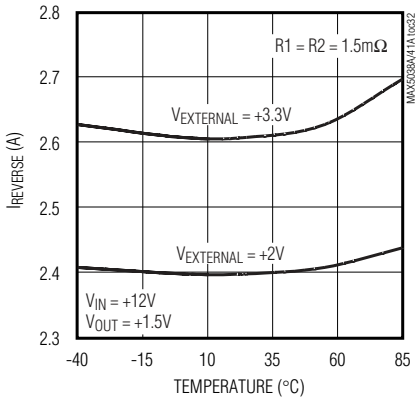

**ENABLE STARTUP RESPONSE**



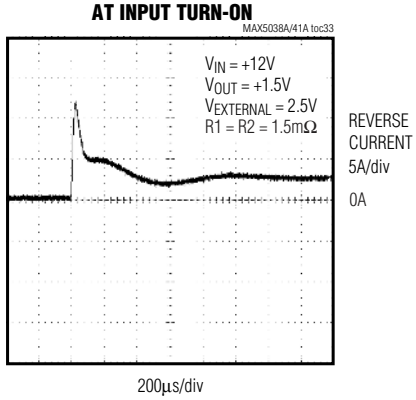

**LOAD-TRANSIENT RESPONSE**



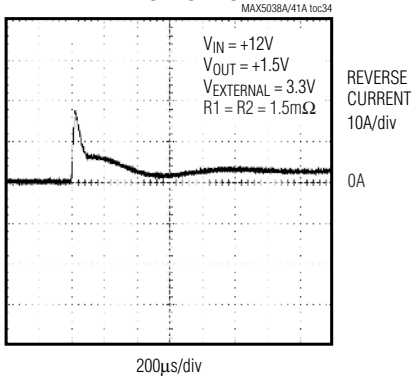

**REVERSE-CURRENT SINK vs. TEMPERATURE**



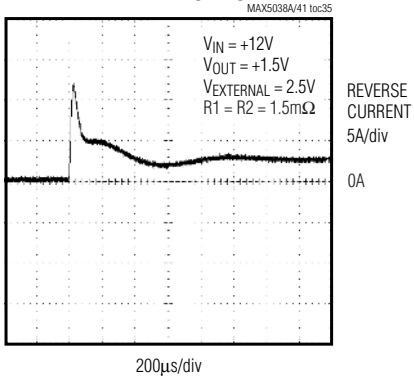

**REVERSE-CURRENT SINK AT INPUT TURN-ON**



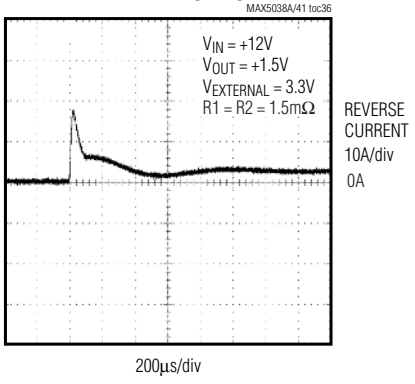

**REVERSE-CURRENT SINK AT INPUT TURN-ON**




**REVERSE-CURRENT SINK AT ENABLE TURN-ON**




**REVERSE-CURRENT SINK AT ENABLE TURN-ON**

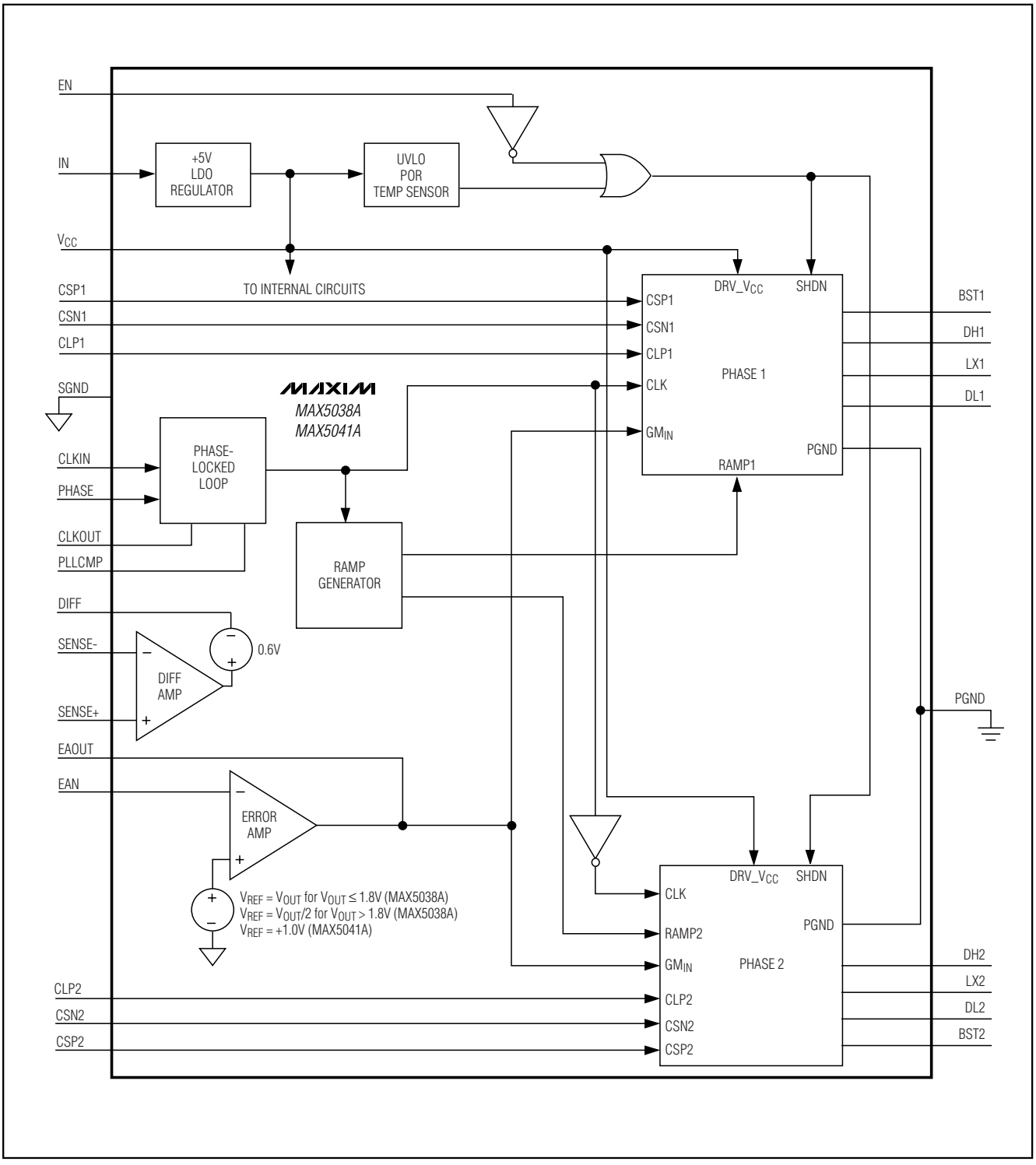


## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 13 | CSP2, CSP1 | Current-Sense Differential Amplifier Positive Input. Senses the inductor current. The differential voltage between CSP_ and CSN_ is amplified internally by the current-sense amplifier gain of 18. |
| 2, 14 | CSN2, CSN1 | Current-Sense Differential Amplifier Negative Input. Together with CSP_, senses the inductor current. |
| 3 | PHASE | Phase-Shift Setting Input. Connect PHASE to $V_{CC}$ for 120°, leave PHASE unconnected for 90°, or connect PHASE to SGND for 60° of phase shift between the rising edges of CLKOUT and CLKIN/DH1. |
| 4 | PLLCMP | External Loop-Compensation Input. Connect compensation network for the phase-locked loop (see *Phase-Locked Loop* section). |
| 5, 7 | CLP2, CLP1 | Current-Error Amplifier Output. Compensate the current loop by connecting an RC network to ground. |
| 6 | SGND | Signal Ground. Ground connection for the internal control circuitry. |
| 8 | SENSE+ | Differential Output Voltage-Sensing Positive Input. Used to sense a remote load. Connect SENSE+ to $V_{OUT+}$ at the load. The MAX5038A regulates the difference between SENSE+ and SENSE- according to the factory preset output voltage. The MAX5041A regulates the SENSE+ to SENSE- difference to +1.0V. |
| 9 | SENSE- | Differential Output Voltage-Sensing Negative Input. Used to sense a remote load. Connect SENSE- to $V_{OUT-}$ or PGND at the load. |
| 10 | DIFF | Differential Remote-Sense Amplifier Output. DIFF is the output of a precision unity-gain amplifier. |
| 11 | EAN | Voltage-Error Amplifier Inverting Input. Receives the output of the differential remote-sense amplifier. Referenced to SGND. |
| 12 | EAOUT | Voltage-Error Amplifier Output. Connect to the external gain-setting feedback resistor. The external error amplifier gain-setting resistors determine the amount of adaptive voltage positioning |
| 15 | EN | Output Enable. A logic low shuts down the power drivers. EN has an internal 5µA pullup current. |
| 16, 26 | BST1, BST2 | Boost Flying-Capacitor Connection. Reservoir capacitor connection for the high-side FET driver supply. Connect a 0.47µF ceramic capacitor between BST_ and LX_. |
| 17, 25 | DH1, DH2 | High-Side Gate Driver Output. Drives the gate of the high-side MOSFET. |
| 18, 24 | LX1, LX2 | Inductor Connection. Source connection for the high-side MOSFETs. Also serves as the return terminal for the high-side driver. |
| 19, 23 | DL1, DL2 | Low-Side Gate Driver Output. Synchronous MOSFET gate drivers for the two phases. |
| 20 | $V_{CC}$ | Internal +5V Regulator Output. $V_{CC}$ is derived internally from the IN voltage. Bypass to SGND with 4.7µF and 0.1µF ceramic capacitors. |
| 21 | IN | Supply Voltage Connection. Connect IN to $V_{CC}$ for a +5V system. Connect the VRM input to IN through an RC lowpass filter, a 2.2Ω resistor, and a 0.1µF ceramic capacitor. |
| 22 | PGND | Power Ground. Connect PGND, low-side synchronous MOSFET's source, and $V_{CC}$ bypass capacitor returns together. |
| 27 | CLKOUT | Oscillator Output. CLKOUT is phase shifted from CLKIN by the amount specified by PHASE. Use CLKOUT to parallel additional MAX5038A/MAX5041As. |
| 28 | CLKIN | CMOS Logic Clock Input. Drive the internal oscillator with a frequency range between 125kHz and 600kHz, or connect to $V_{CC}$ or SGND. Connect CLKIN to SGND to set the internal oscillator to 250kHz or connect to $V_{CC}$ to set the internal oscillator to 500kHz. CLKIN has an internal 5µA pulldown current. |

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

## Functional Diagram



## Detailed Description

The MAX5038A/MAX5041A (Figures 1 and 2) average-current-mode PWM controllers drive two out-of-phase buck converter channels. Average-current-mode control improves current sharing between the channels while minimizing component derating and size. Parallel multiple MAX5038A/MAX5041A regulators to increase the output current capacity. For maximum ripple rejection at the input, set the phase shift between phases to 90° for two paralleled converters, or 60° for three paralleled converters. The paralleling capability of the MAX5038A/MAX5041A improves design flexibility in applications requiring upgrades (higher load).

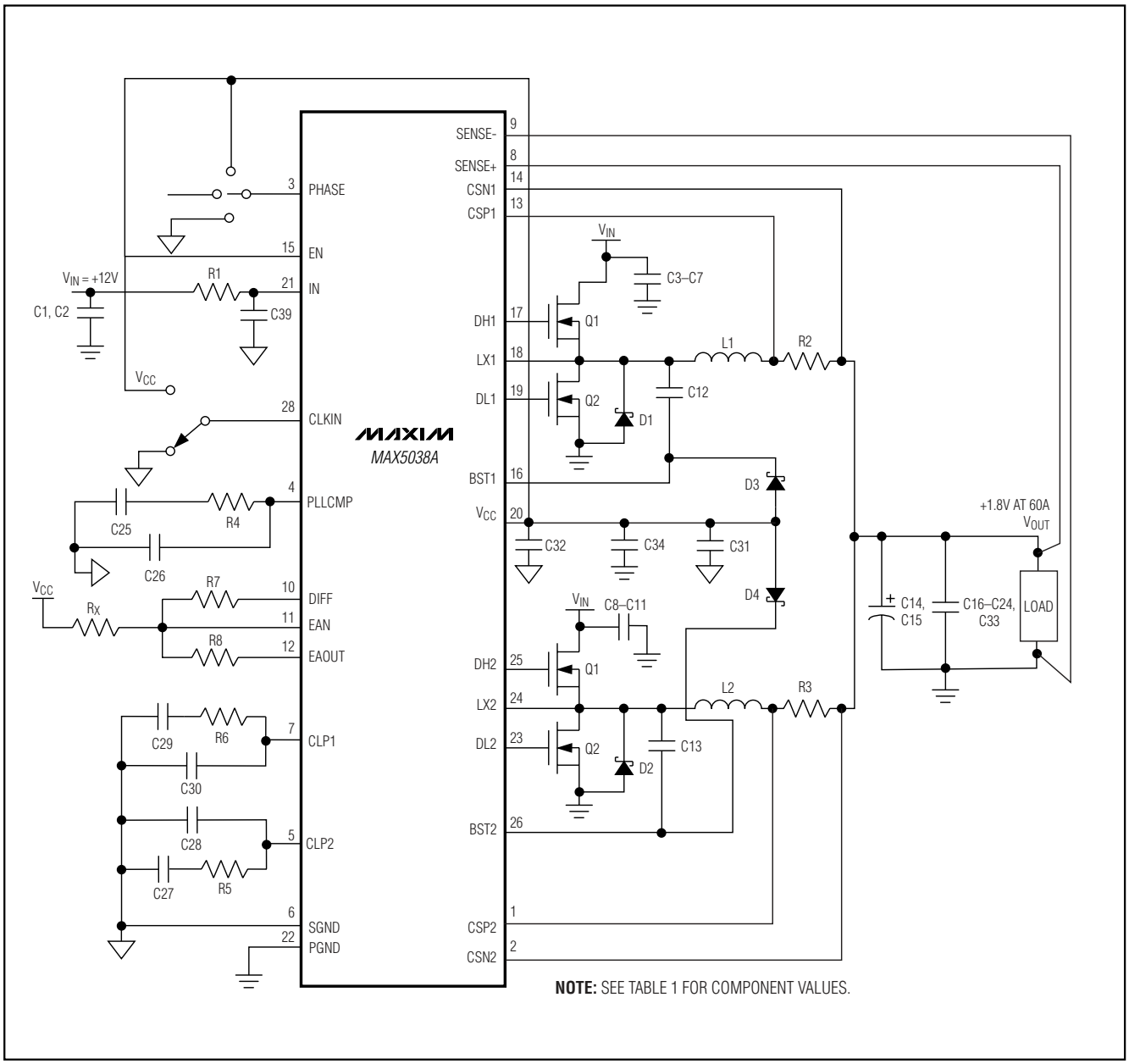



*Figure 1. MAX5038A Typical Application Circuit, $V_{IN}$ = +12V*

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

Dual-phase converters with an out-of-phase locking arrangement reduce the input and output capacitor ripple current, effectively multiplying the switching frequency by the number of phases. Each phase of the MAX5038A/MAX5041A consists of an inner average current loop controlled by a common outer-loop voltage-error amplifier (VEA). The combined action of the two inner current loops and the outer voltage loop corrects the output voltage errors and forces the phase currents to be equal.

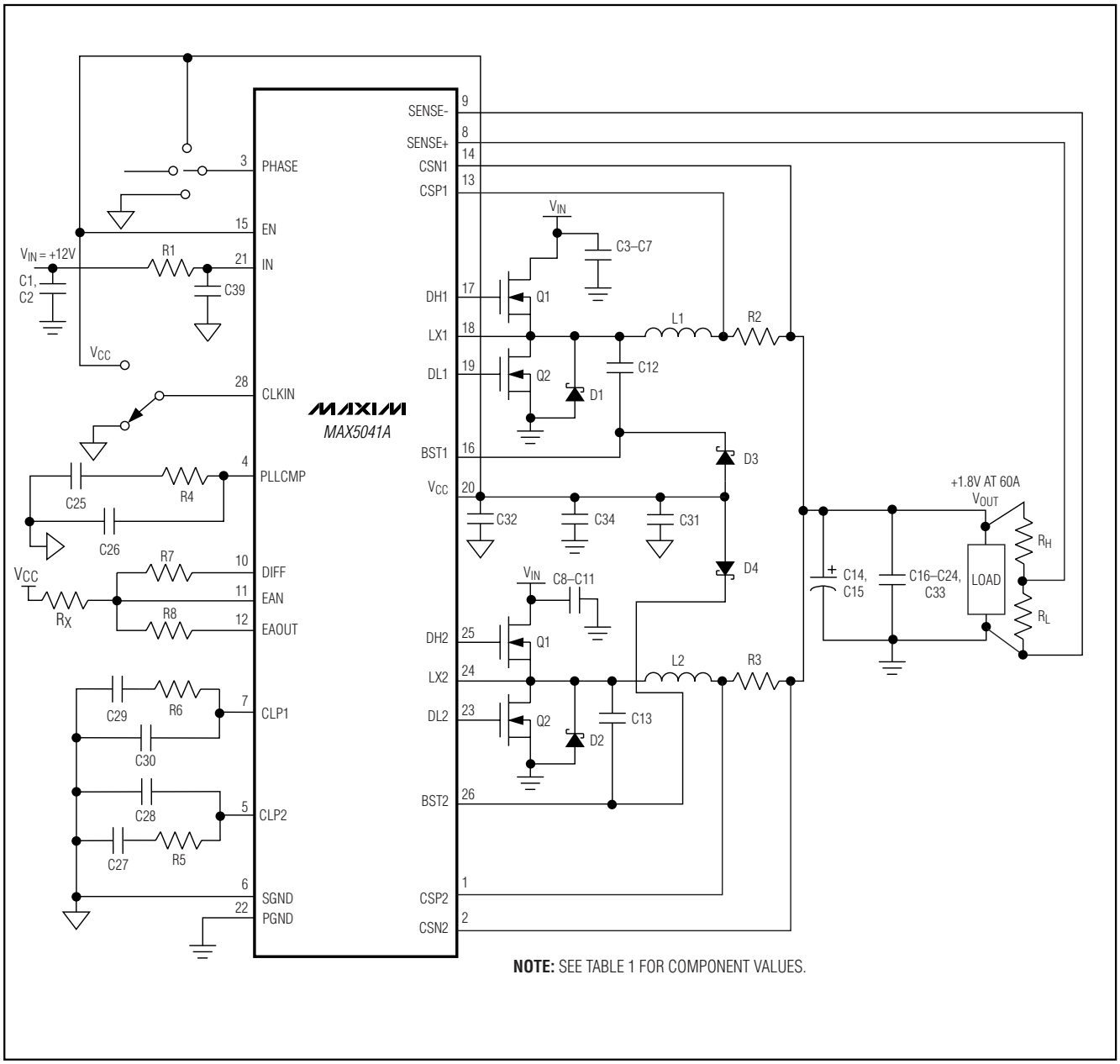



*Figure 2. MAX5041A Typical Application Circuit, $V_{IN}$ = +12V*

### $V_{IN}$ and $V_{CC}$

The MAX5038A/MAX5041A accept an input voltage range of +4.75V to +5.5V or +8V to +28V. All internal control circuitry operates from an internally regulated nominal voltage of +5V ($V_{CC}$). For input voltages of +8V or greater, the internal $V_{CC}$ regulator steps the voltage down to +5V. The $V_{CC}$ output voltage is a regulated +5V output capable of sourcing up to 80mA. Bypass $V_{CC}$ to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors in parallel for high-frequency noise rejection and stable operation (Figures 1 and 2).

Calculate power dissipation in the MAX5038A/MAX5041A as a product of the input voltage and the total $V_{CC}$ regulator output current ($I_{CC}$). $I_{CC}$ includes quiescent current ($I_Q$) and gate drive current ($I_{DD}$):

$$P_D = V_{IN} \times I_{CC} \quad (1)$$

$$I_{CC} = I_Q + f_{SW} \times (Q_{G1} + Q_{G2} + Q_{G3} + Q_{G4}) \quad (2)$$

where $Q_{G1}$, $Q_{G2}$, $Q_{G3}$, and $Q_{G4}$ are the total gate charge of the low-side and high-side external MOSFETs, $I_Q$ is 4mA (typ), and $f_{SW}$ is the switching frequency of each individual phase.

For applications utilizing a +5V input voltage, disable the $V_{CC}$ regulator by connecting IN and $V_{CC}$ together.

### Undervoltage Lockout (UVLO)/Soft-Start

The MAX5038A/MAX5041A include an undervoltage lockout with hysteresis and a power-on reset circuit for converter turn-on and monotonic rise of the output voltage. The UVLO threshold is internally set between +4.0V and +4.5V with a 200mV hysteresis. Hysteresis at UVLO eliminates “chattering” during startup.

Most of the internal circuitry, including the oscillator, turns on when the input voltage reaches +4V. The MAX5038A/MAX5041A draw up to 4mA of current before the input voltage reaches the UVLO threshold.

The compensation network at the current-error amplifiers (CLP1 and CLP2) provides an inherent soft-start of the output voltage. It includes a parallel combination of capacitors (C28, C30) and resistors (R5, R6) in series with other capacitors (C27, C29) (see Figures 1 and 2). The voltage at CLP_ limits the maximum current available to charge output capacitors. The capacitor on CLP_ in conjunction with the finite output-drive current of the current-error amplifier yields a finite rise time for the output current and thus the output voltage.

### Internal Oscillator

The internal oscillator generates the 180° out-of-phase clock signals required by the pulse-width modulation (PWM) circuits. The oscillator also generates the $2V_{P-P}$ voltage ramp signals necessary for the PWM comparators. Connect CLKIN to SGND to set the internal oscillator frequency to 250kHz or connect CLKIN to $V_{CC}$ to set the internal oscillator to 500kHz.

CLKIN is a CMOS logic clock input for the phase-locked loop (PLL). When driven externally, the internal oscillator locks to the signal at CLKIN. A rising edge at CLKIN starts the ON cycle of the PWM. Ensure that the external clock pulse width is at least 200ns. CLKOUT provides a phase-shifted output with respect to the rising edge of the signal at CLKIN. PHASE sets the amount of phase shift at CLKOUT. Connect PHASE to $V_{CC}$ for 120° of phase shift, leave PHASE unconnected for 90° of phase shift, or connect PHASE to SGND for 60° of phase shift with respect to CLKIN.

The MAX5038A/MAX5041A require compensation on PLLCMP even when operating from the internal oscillator. The device requires an active PLL in order to generate the proper clock signal required for PWM operation.

### Control Loop

The MAX5038A/MAX5041A use an average-current-mode control scheme to regulate the output voltage (Figures 3a and 3b). The main control loop consists of an inner current loop and an outer voltage loop. The inner loop controls the output currents ($I_{PHASE1}$ and $I_{PHASE2}$) while the outer loop controls the output voltage. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

The current loop consists of a current-sense resistor ($R_S$), a current-sense amplifier (CA_), a current-error amplifier (CEA_), an oscillator providing the carrier ramp, and a PWM comparator (CPWM_). The precision CA_ amplifies the sense voltage across $R_S$ by a factor of 18. The inverting input to the CEA_ senses the CA_ output. The CEA_ output is the difference between the voltage-error amplifier output (EAOUT) and the amplified voltage from the CA_. The RC compensation network connected to CLP1 and CLP2 provides external frequency compensation for the respective CEA_. The start of every clock cycle enables the high-side drivers and initiates a PWM ON cycle. Comparator CPWM_ compares the output voltage from the CEA_ with a 0 to +2V ramp from the oscillator. The PWM ON cycle terminates when the ramp voltage exceeds the error voltage.

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

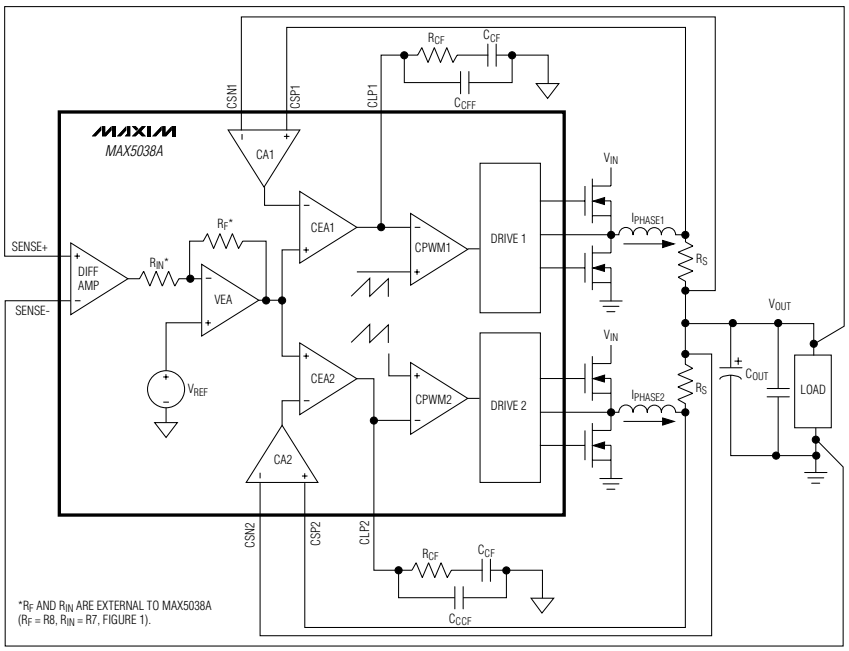



*Figure 3a. MAX5038A Control Loop*

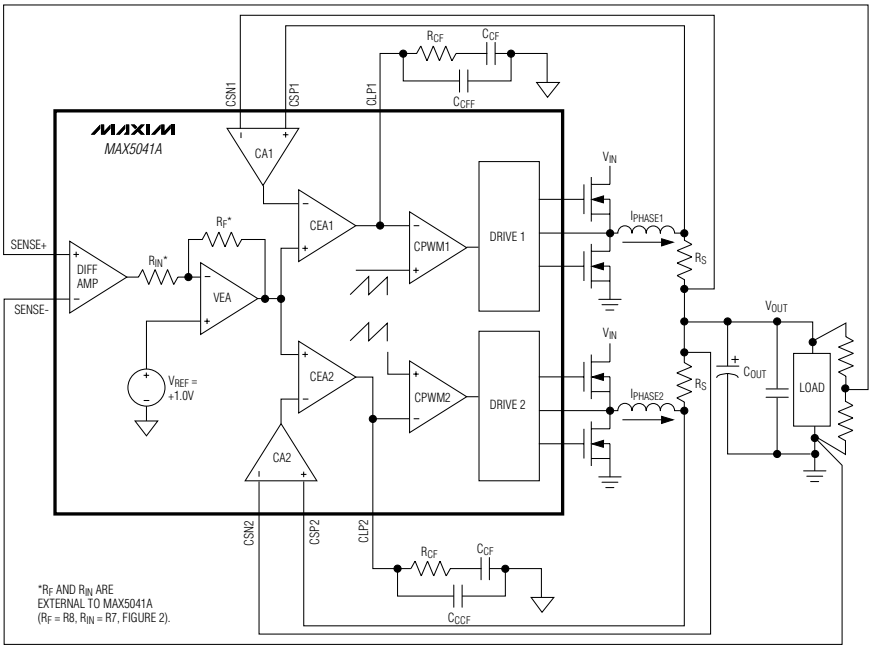



*Figure 3b. MAX5041A Control Loop*

The outer voltage control loop consists of the differential amplifier (DIFF AMP), reference voltage, and VEA. The unity-gain differential amplifier provides true differential remote sensing of the output voltage. The differential amplifier output connects to the inverting input (EAN) of the VEA. The noninverting input of the VEA is internally connected to an internal precision reference voltage. The MAX5041A reference voltage is set to +1.0V and the MAX5038A reference is set to the preset output voltage. The VEA controls the two inner current loops (Figures 3a and 3b). Use a resistive feedback network to set the VEA gain as required by the adaptive voltage-positioning circuit (see the *Adaptive Voltage Positioning* section).

### Current-Sense Amplifier

The differential current-sense amplifier (CA_) provides a DC gain of 18. The maximum input offset voltage of the current-sense amplifier is 1mV and the common-mode voltage range is -0.3V to +3.6V. The current-sense amplifier senses the voltage across a current-sense resistor.

### Peak-Current Comparator

The peak-current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions such as an output inductor malfunction (Figure 4). Note that the average-current-limit threshold of 48mV still limits the output current during short-circuit conditions. To prevent inductor saturation, select an output inductor with a saturation current specification greater than the average current limit (48mV). Proper inductor selection ensures that only extreme conditions trip the peak-current comparator, such as a broken output inductor. The 112mV voltage threshold for triggering the peak-current limit is twice the full-scale average current-limit voltage threshold. The peak-current comparator has a delay of only 260ns.

### Current-Error Amplifier

Each phase of the MAX5038A/MAX5041A has a dedicated transconductance current-error amplifier (CEA_) with a typical $g_m$ of 550µS and 320µA output sink and source current capability. The current-error amplifier outputs, CLP1 and CLP2, serve as the inverting input to the PWM comparator. CLP1 and CLP2 are externally accessible to provide frequency compensation for the inner current loops (Figures 3a and 3b). Compensate CEA_ such that the inductor current down slope, which becomes the up slope to the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section).

### PWM Comparator and R-S Flip-Flop

The PWM comparator (CPWM) sets the duty cycle for each cycle by comparing the output of the current-error amplifier to a $2V_{P-P}$ ramp. At the start of each clock cycle, an R-S flip-flop resets and the high-side driver (DH_) turns on. The comparator sets the flip-flop as soon as the ramp voltage exceeds the CLP_ voltage, thus terminating the ON cycle (Figure 4).

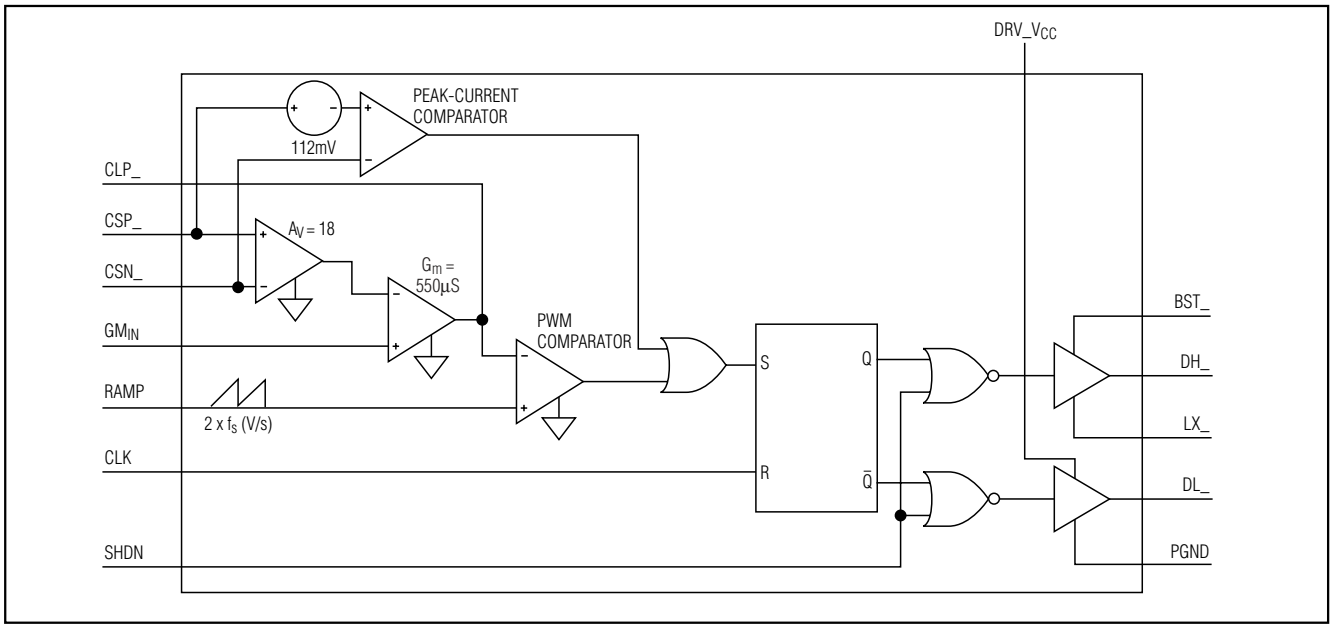



*Figure 4. Phase Circuit (Phase 1/Phase 2)*

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

### Differential Amplifier

The differential amplifier (DIFF AMP) facilitates output voltage remote sensing at the load (Figures 3a and 3b). It provides true differential output voltage sensing while rejecting the common-mode voltage errors due to high-current ground paths. Sensing the output voltage directly at the load provides accurate load voltage sensing in high-current environments. The VEA provides the difference between the differential amplifier output (DIFF) and the desired output voltage. The differential amplifier has a bandwidth of 3MHz. The difference between SENSE+ and SENSE- regulates to the preset output voltage for the MAX5038A and regulates to +1V for the MAX5041A.

### Voltage-Error Amplifier

The VEA sets the gain of the voltage control loop and determines the error between the differential amplifier output and the internal reference voltage ($V_{REF}$).

$V_{REF}$ equals $V_{OUT(NOM)}$ for the +1.8V or lower voltage versions of the MAX5038A and $V_{REF}$ equals $V_{OUT(NOM)}/2$ for the +2.5V and +3.3V versions. For MAX5041A, $V_{REF}$ equals +1V.

An offset is added to the output voltage of the MAX5038A/MAX5041A with a finite gain ($R_F/R_{IN}$) of the VEA such that the no-load output voltage is higher than the nominal value. Choose $R_F$ and $R_{IN}$ from the *Adaptive Voltage Positioning* section and use the following equations to calculate the no-load output voltage.

MAX5038A:

$$V_{OUT(NL)} = \left(1 + \frac{R_{IN}}{R_F}\right) \times V_{OUT(NOM)} \quad (3)$$

MAX5041A:

$$V_{OUT(NL)} = \left(1 + \frac{R_{IN}}{R_F}\right) \times \left(\frac{R_H + R_L}{R_L}\right) \times V_{REF} \quad (4)$$

where $R_H$ and $R_L$ are the feedback resistor network (Figure 2).

Some applications require $V_{OUT}$ equal to $V_{OUT(NOM)}$ at no load. To ensure that the output voltage does not exceed the nominal output voltage ($V_{OUT(NOM)}$), add a resistor $R_X$ from $V_{CC}$ to EAN.

Use the following equations to calculate the value of $R_X$.

For MAX5038A versions of $V_{OUT(NOM)} \le +1.8V$:

$$R_X = [V_{CC} - (V_{NOM} + 0.6)] \times \frac{R_F}{V_{NOM}} \quad (5)$$

For MAX5038A versions of $V_{OUT(NOM)} > +1.8V$:

$$R_X = [2V_{CC} - (V_{NOM} + 1.2)] \times \frac{R_F}{V_{NOM}} \quad (6)$$

For MAX5041A:

$$R_X = [V_{CC} - 1.6] \times \frac{R_F}{V_{REF}} \quad (7)$$

The VEA output clamps to +0.9V (plus the common-mode voltage of +0.6V), thus limiting the average maximum current from individual phases. The maximum average-current-limit threshold for each phase is equal to the maximum clamp voltage of the VEA divided by the gain (18) of the current-sense amplifier. This allows for accurate settings for the average maximum current for each phase. Set the VEA gain using $R_F$ and $R_{IN}$ for the amount of output voltage positioning required as discussed in the *Adaptive Voltage Positioning* section (Figures 3a and 3b).

### Adaptive Voltage Positioning

Powering new-generation processors requires new techniques to reduce cost, size, and power dissipation. Voltage positioning reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher than the output voltage during nominally loaded conditions allows a larger downward voltage excursion when the output current suddenly increases. Regulating at a lower output voltage under a heavy load allows a larger upward-voltage excursion when the output current suddenly decreases. A larger allowed, voltage-step excursion reduces the required number of output capacitors or allows for the use of higher ESR capacitors.

Voltage positioning and the ability to operate with multiple reference voltages may require the output to regulate away from a center value. Define the center value as the voltage where the output drops ($\Delta V_{OUT}/2$) at one half the maximum output current (Figure 5).

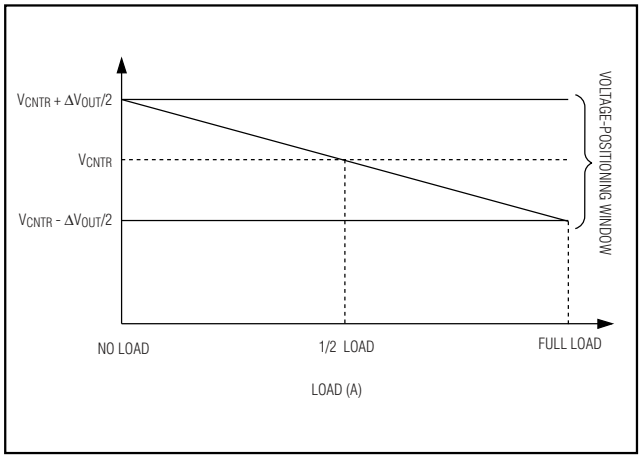



*Figure 5. Defining the Voltage-Positioning Window*

Set the voltage-positioning window ($\Delta V_{OUT}$) using the resistive feedback of the VEA. Use the following equations to calculate the voltage-positioning window for the MAX5038A:

$$\Delta V_{OUT} = \frac{I_{OUT} \times R_{IN}}{2 \times G_C \times R_F} \quad (8)$$

$$G_C = \frac{0.05}{R_S} \quad (9)$$

Use the following equation to calculate the voltage-positioning window for the MAX5041A:

$$\Delta V_{OUT} = \frac{I_{OUT} \times R_{IN}}{(2 \times G_C \times R_F)} \times \frac{R_H + R_L}{R_L} \quad (10)$$

$$G_C = \frac{0.05}{R_S} \quad (11)$$

where $R_{IN}$ and $R_F$ are the input and feedback resistors of the VEA, $G_C$ is the current-loop transconductance, and $R_S$ is the current-sense resistor or, if using lossless inductor current sensing, the DC resistance of the inductor.

### Phase-Locked Loop: Operation and Compensation

The PLL synchronizes the internal oscillator to the external frequency source when driving CLKIN. Connecting CLKIN to $V_{CC}$ or SGND forces the PWM frequency to default to the internal oscillator frequency of 500kHz or 250kHz, respectively. The PLL uses a conventional architecture consisting of a phase detector and a charge pump capable of providing 20µA of output current. Connect an external series combination capacitor (C25) and resistor (R4) and a parallel capacitor (C26) from PLLCMP to SGND to provide frequency compensation for the PLL (Figure 1). The pole-zero pair compensation provides a zero at $f_Z$ defined by 1 / [R4 x (C25 + C26)] and a pole at $f_P$ defined by 1 / (R4 x C26). Use the following typical values for compensating the PLL: R4 = 7.5kΩ, C25 = 4.7nF, C26 = 470pF. If changing the PLL frequency, expect a finite locking time of approximately 200µs.

The MAX5038A/MAX5041A require compensation on PLLCMP even when operating from the internal oscillator. The device requires an active PLL in order to generate the proper internal PWM clocks.

### MOSFET Gate Drivers (DH_, DL_)

The high-side (DH_) and low-side (DL_) drivers drive the gates of external N-channel MOSFETs (Figures 1 and 2). The drivers' high-peak sink and source current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced cross-conduction losses. For modern CPU voltage-regulating module applications where the duty cycle is less than 50%, choose high-side MOSFETs (Q1 and Q3) with a moderate $R_{DS(ON)}$ and a very low gate charge. Choose low-side MOSFETs (Q2 and Q4) with very low $R_{DS(ON)}$ and moderate gate charge.

The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The typical nonoverlap time is 60ns between the high-side and low-side MOSFETs.

### BST_

$V_{CC}$ powers the low- and high-side MOSFET drivers. Connect a 0.47µF low-ESR ceramic capacitor between BST_ and LX_. Bypass $V_{CC}$ to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors. For high-current applications, bypass $V_{CC}$ to PGND with one or more 0.1µF, low-ESR ceramic capacitor(s). Reduce the PC board area formed by these capacitors, the rectifier diodes between $V_{CC}$ and the boost capacitor, the MAX5038A/MAX5041A, and the switching MOSFETs.

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

### Overload Conditions

Average-current-mode control has the ability to limit the average current sourced by the converter during a fault condition. When a fault condition occurs, the VEA output clamps to +0.9V with respect to the common-mode voltage ($V_{CM}$ = +0.6V) and is compared with the output of the current-sense amplifiers (CA1 and CA2) (see Figures 3a and 3b). The current-sense amplifier's gain of 18 limits the maximum current in the inductor or sense resistor to $I_{LIMIT}$ = 50mV/$R_S$.

### Parallel Operation

For applications requiring large output current, parallel up to three MAX5038A/MAX5041As (six phases) to triple the available output current. The paralleled converters operate at the same switching frequency but different phases keep the capacitor ripple RMS currents to a minimum. Three parallel MAX5038A/MAX5041A converters deliver up to 180A of output current. To set the phase shift of the on-board PLL, leave PHASE unconnected for 90° of phase shift (two paralleled converters), or connect PHASE to SGND for 60° of phase shift (three converters in parallel). Designate one converter as master and the remaining converters as slaves. Connect the master and slave controllers in a daisy-chain configuration as shown in Figure 6. Connect CLKOUT from the master controller to CLKIN of the first slaved controller, and CLKOUT from the first slaved controller to CLKIN of the second slaved controller. Choose the appropriate phase shift for minimum ripple currents at the input and output capacitors. The master controller senses the output differential voltage through SENSE+ and SENSE- and generates the DIFF voltage. Disable the voltage sensing of the slaved controllers by leaving DIFF unconnected (floating). Figure 7 shows a detailed typical parallel application circuit using two MAX5038As. This circuit provides four phases at an input voltage of +12V and an output voltage range of +1V to +3.3V at 104A.

## Applications Information

Each MAX5038A/MAX5041A circuit drives two 180° out-of-phase channels. Parallel two or three MAX5038A/MAX5041A circuits to achieve four- or six-phase operation, respectively. Figure 1 shows the typical application circuit for a two-phase operation. The design criteria for a two-phase converter includes frequency selection, inductor value, input/output capacitance, switching MOSFETs, sense resistors, and the compensation network. Follow the same procedure for the four- and six-phase converter design, except for the input and output capacitance. The input and output capacitance requirements vary depending on the operating duty cycle.

The examples discussed in this data sheet pertain to a typical application with the following specifications:

$V_{IN}$ = +12V

$V_{OUT}$ = +1.8V

$I_{OUT(MAX)}$ = 52A

$f_{SW}$ = 250kHz

Peak-to-Peak Inductor Current ($\Delta I_L$) = 10A

Table 1 shows a list of recommended external components (Figure 1) and Table 2 provides component supplier information.

### Number of Phases

Selecting the number of phases for a voltage regulator depends mainly on the ratio of input-to-output voltage (operating duty cycle). Optimum output-ripple cancellation depends on the right combination of operating duty cycle and the number of phases. Use the following equation as a starting point to choose the number of phases:

$$N_{PH} \approx K/D \quad (12)$$

where K = 1, 2, or 3 and the duty cycle is $D = V_{OUT}/V_{IN}$.

Choose K to make $N_{PH}$ an integer number. For example, converting $V_{IN}$ = +12V to $V_{OUT}$ = +1.8V yields better ripple cancellation in the six-phase converter than in the four-phase converter. Ensure that the output load justifies the greater number of components for multiphase conversion. Generally limiting the maximum output current to 25A per phase yields the most cost-effective solution. The maximum ripple cancellation occurs when $N_{PH}$ = K/D.

Single-phase conversion requires greater size and power dissipation for external components such as the switching MOSFETs and the inductor. Multiphase conversion eliminates the heatsink by distributing the power dissipation in the external components. The multiple phases operating at given phase shifts effectively increase the switching frequency seen by the input/output capacitors, thereby reducing the input/output capacitance requirement for the same ripple performance. The lower inductance value improves the large-signal response of the converter during a transient load at the output. Consider all these issues when determining the number of phases necessary for the voltage regulator application.

### Inductor Selection

The switching frequency per phase, peak-to-peak ripple current in each phase, and allowable ripple at the output determine the inductance value.

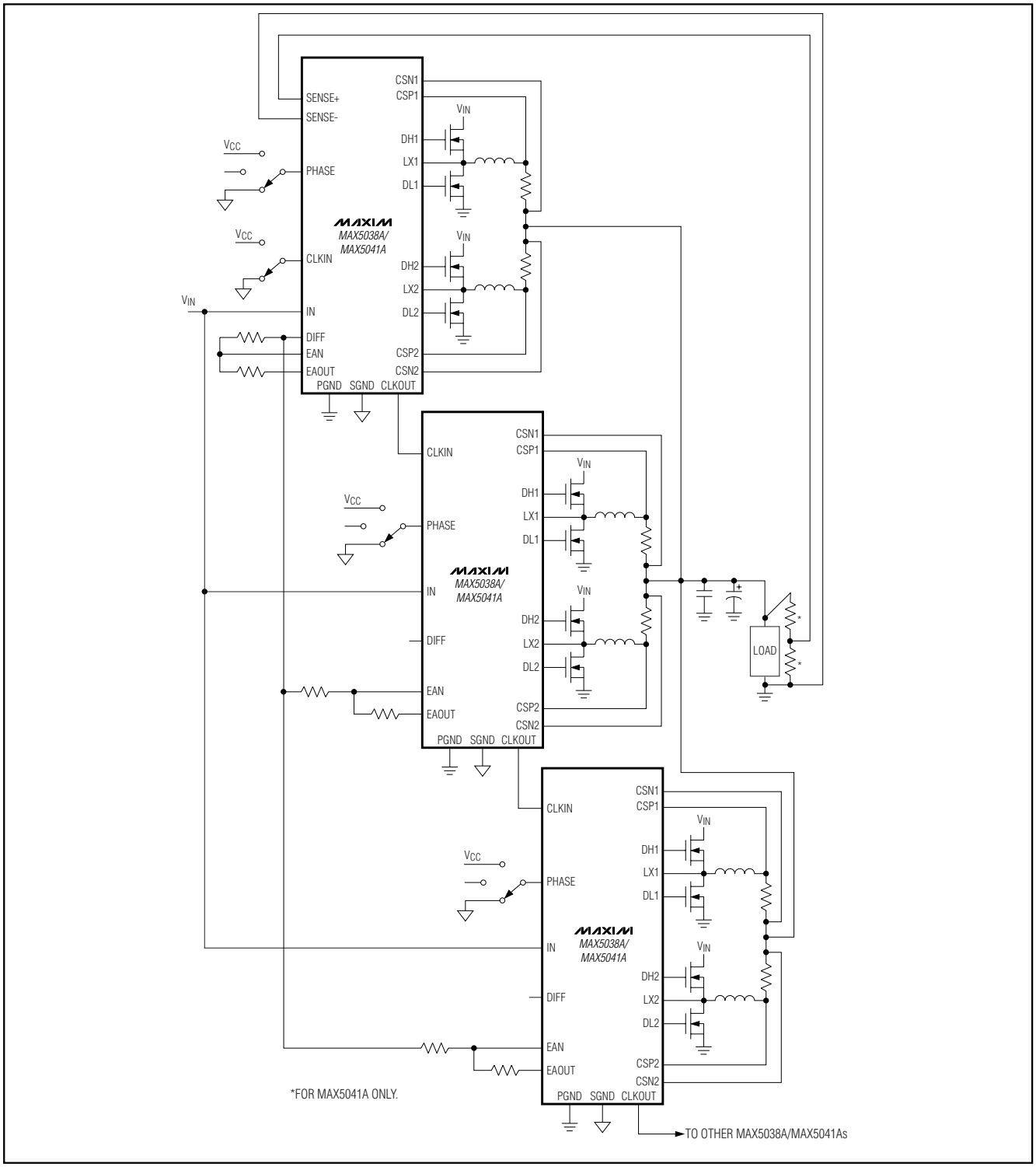



*Figure 6. Parallel Configuration of Multiple MAX5038A/MAX5041As*

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

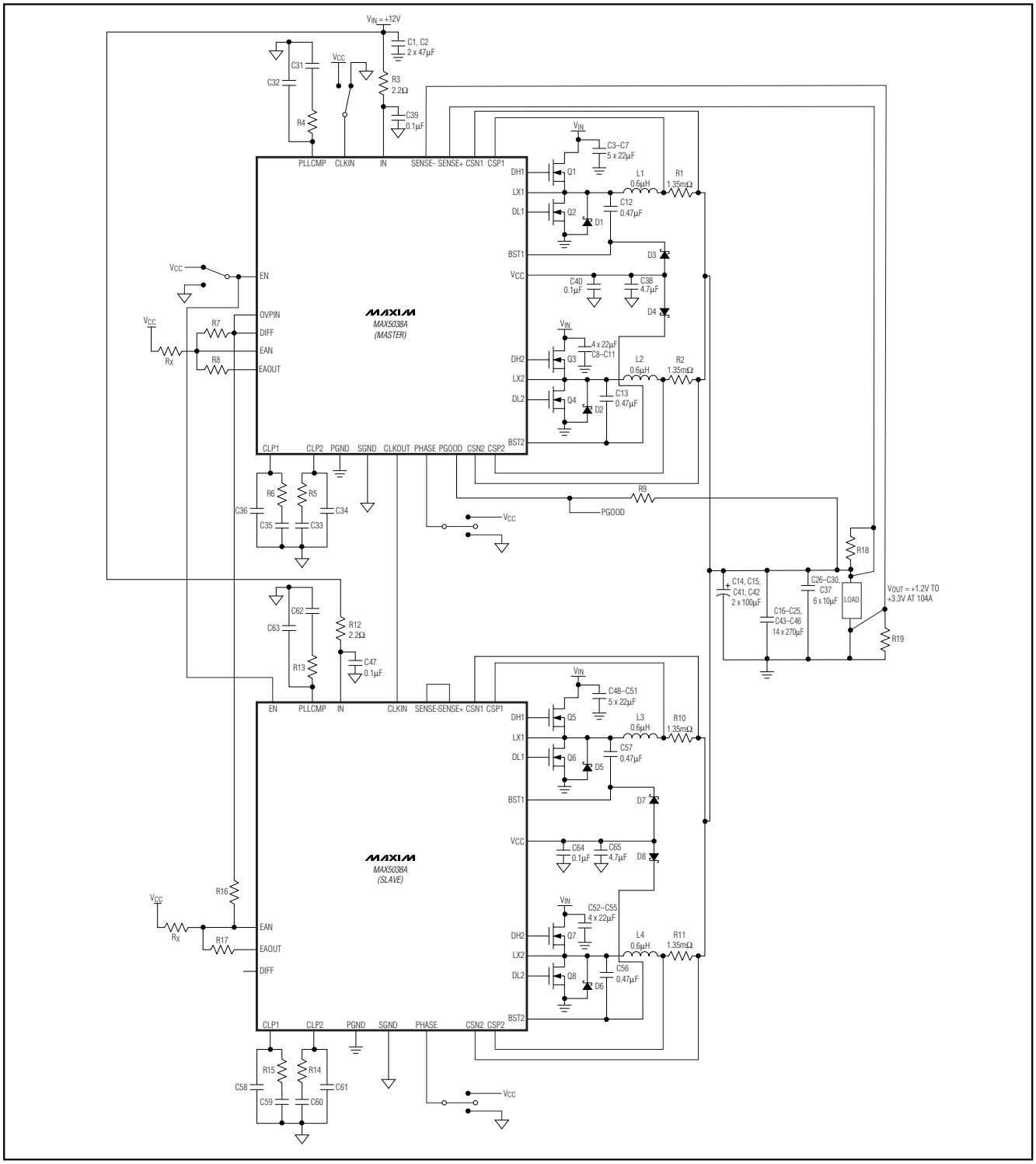



*Figure 7. Four-Phase Parallel Application Circuit ($V_{IN}$ = +12V, $V_{OUT}$ = +1.2V to +3.3V at 104A)*

## Table 1. Component List

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| C1, C2 | 2 | 47µF,16V X5R input-filter capacitors, TDK C5750X5R1C476M |
| C3–C11 | 9 | 22µF, 16V input-filter capacitors, TDK C4532X5R1C226M |
| C12, C13 | 2 | 0.47µF, 16V capacitors, TDK C1608X5R1A474K |
| C14, C15 | 2 | 100µF, 6.3V output-filter capacitors, Murata GRM44-1X5R107K6.3 |
| C16–C24, C33 | 10 | 270µF, 2V output-filter capacitors, Panasonic EEFUE0D271R |
| C25 | 1 | 4700pF, 16V X7R capacitor, Vishay-Siliconix VJ0603Y471JXJ |
| C26, C28, C30 | 3 | 470pF, 16V capacitors, Murata GRM1885C1H471JAB01 |
| C27, C29 | 2 | 0.01µF, 50V X7R capacitors, Murata GRM188R71H103KA01 |
| C31 | 1 | 4.7µF, 16V X5R capacitor, Murata GRM40-034X5R475k6.3 |
| C32, C34, C39 | 3 | 0.1µF, 16V X7R capacitors, Murata GRM188R71C104KA01 |
| D1, D2 | 2 | Schottky diodes, ON Semiconductor MBRS340T3 |
| D3, D4 | 2 | Schottky diodes, ON Semiconductor MBR0520LT1 |
| L1, L2 | 2 | 0.6µH, 27A inductors, Panasonic ETQP1H0R6BFX |
| Q1, Q3 | 2 | Upper power MOSFETs, Vishay-Siliconix Si7860DP |
| Q2, Q4 | 2 | Lower power MOSFETs, Vishay-Siliconix Si7886DP |
| R1 | 1 | 2.2Ω ±1% resistor |
| R2, R3 | 4 | Current-sense resistors, use two 2.7mΩ resistors in parallel, Panasonic ERJM1WSF2M7U |
| R4 | 1 | 7.5kΩ ±1% resistor |
| R5, R6 | 2 | 1kΩ ±1% resistors |
| R7 | 1 | 4.99kΩ ±1% resistor |
| R8, R9 | 2 | 37.4kΩ ±1% resistors |

## Table 2. Component Suppliers

| SUPPLIER | PHONE | FAX | WEBSITE |
|---|---|---|---|
| Murata | 770-436-1300 | 770-436-3030 | www.murata.com |
| ON Semiconductor | 602-244-6600 | 602-244-3345 | www.on-semi.com |
| Panasonic | 714-373-7939 | 714-373-7183 | www.panasonic.com |
| TDK | 847-803-6100 | 847-390-4405 | www.tcs.tdk.com |
| Vishay-Siliconix | 1-800-551-6933 | 619-474-8920 | www.vishay.com |

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

Selecting higher switching frequencies reduces the inductance requirement, but at the cost of lower efficiency. The charge/discharge cycle of the gate and drain capacitances in the switching MOSFETs create switching losses. The situation worsens at higher input voltages, since switching losses are proportional to the square of input voltage. Use 500kHz per phase for $V_{IN}$ = +5V and 250kHz or less per phase for $V_{IN} \geq$ +12V.

Although lower switching frequencies per phase increase the peak-to-peak inductor ripple current ($\Delta I_L$), the ripple cancellation in the multiphase topology reduces the RMS ripple current of the input and output capacitors.

Use the following equation to determine the minimum inductance value:

$$L_{MIN} = \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times \Delta I_L} \quad (13)$$

Choose $\Delta I_L$ equal to about 40% of the output current per phase. Since $\Delta I_L$ affects the output-ripple voltage, the inductance value may need minor adjustment after choosing the output capacitors for full-rated efficiency.

Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. Particular applications may require custom-made inductors. Use high-frequency core material for custom inductors. High $\Delta I_L$ causes large peak-to-peak flux excursion increasing the core losses at higher frequencies. The high-frequency operation coupled with high $\Delta I_L$, reduces the required minimum inductance and even makes the use of planar inductors possible. The advantages of using planar magnetics include low-profile design, excellent current-sharing between phases due to the tight control of parasitics, and low cost.

For example, calculate the minimum inductance at $V_{IN(MAX)}$ = +13.2V, $V_{OUT}$ = +1.8V, $\Delta I_L$ = 10A, and $f_{SW}$ = 250kHz:

$$L_{MIN} = \frac{(13.2 - 1.8) \times 1.8}{13.2 \times 250k \times 10} = 0.6\mu H \quad (14)$$

The average-current-mode control feature of the MAX5038A/MAX5041A limits the maximum peak inductor current and prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current.

Use the following equation to determine the worst-case inductor current for each phase:

$$I_{L\_PEAK} = \frac{0.051}{R_{SENSE}} + \frac{\Delta I_L}{2} \quad (15)$$

where $R_{SENSE}$ is the sense resistor in each phase.

### Switching MOSFETs

When choosing a MOSFET for voltage regulators, consider the total gate charge, $R_{DS(ON)}$, power dissipation, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications.

The average current from the MAX5038A/MAX5041A gate-drive output is proportional to the total capacitance it drives from DH1, DH2, DL1, and DL2. The power dissipated in the MAX5038A/MAX5041A is proportional to the input voltage and the average drive current. See the *$V_{IN}$ and $V_{CC}$* section to determine the maximum total gate charge allowed from all the driver outputs combined.

The gate charge and drain capacitance ($CV^2$) loss, the cross-conduction loss in the upper MOSFET due to finite rise/fall time, and the $I^2R$ loss due to RMS current in the MOSFET $R_{DS(ON)}$ account for the total losses in the MOSFET. Estimate the power loss ($PD_{MOS\_}$) in the high-side and low-side MOSFETs using following equations:

$$PD_{MOS-HI} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{4}\right) + 1.4R_{DS(ON)} \times I^2_{RMS-HI} \quad (16)$$

where $Q_G$, $R_{DS(ON)}$, $t_R$, and $t_F$ are the upper-switching MOSFET's total gate charge, on-resistance at +25°C, rise time, and fall time, respectively:

$$I_{RMS-HI} = \sqrt{\left(I^2_{DC} + I^2_{PK} + I_{DC} \times I_{PK}\right) \times \frac{D}{3}} \quad (17)$$

where D = $V_{OUT}/V_{IN}$, $I_{DC}$ = ($I_{OUT}$ - $\Delta I_L$)/2, and $I_{PK}$ = ($I_{OUT}$ + $\Delta I_L$)/2.

$$PD_{MOS-LO} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{2 \times C_{OSS} \times V_{IN}^2 \times f_{SW}}{3}\right) + 1.4R_{DS(ON)} \times I^2_{RMS-LO} \quad (18)$$

$$I_{RMS-LO} = \sqrt{\left(I^2_{DC} + I^2_{PK} + I_{DC} \times I_{PK}\right) \times \frac{(1-D)}{3}} \quad (19)$$

where $C_{OSS}$ is the MOSFET drain-to-source capacitance.

For example, from the typical specifications in the *Applications Information* section with $V_{OUT}$ = +1.8V, the high-side and low-side MOSFET RMS currents are 9.9A and 24.1A, respectively. Ensure that the thermal impedance of the MOSFET package keeps the junction temperature at least 25°C below the absolute maximum rating. Use the following equation to calculate maximum junction temperature:

$$T_J = PD_{MOS} \times \theta_{J-A} + T_A \quad (20)$$

## Table 3. Peak-to-Peak Output Ripple Current Calculations

| NO. OF PHASES (N) | DUTY CYCLE (D) (%) | EQUATION FOR $\Delta I_{P-P}$ |
|---|---|---|
| 2 | < 50 | $\Delta I = \frac{V_O(1-2D)}{L \times f_{SW}}$ |
| 2 | > 50 | $\Delta I = \frac{(V_{IN}-V_O)(2D-1)}{L \times f_{SW}}$ |
| 4 | 0 to 25 | $\Delta I = \frac{V_O(1-4D)}{L \times f_{SW}}$ |
| 4 | 25 to 50 | $\Delta I = \frac{V_O(1-2D)(4D-1)}{2 \times D \times L \times f_{SW}}$ |
| 4 | > 50 | $\Delta I = \frac{V_O(2D-1)(3-4D)}{D \times L \times f_{SW}}$ |
| 6 | < 17 | $\Delta I = \frac{V_O(1-6D)}{L \times f_{SW}}$ |

### Input Capacitors

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. Increasing the number of phases increases the effective switching frequency and lowers the peak-to-average current ratio, yielding a lower input capacitance requirement.

The input ripple comprises $\Delta V_Q$ (caused by the capacitor discharge) and $\Delta V_{ESR}$ (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contributions from the ESR and capacitor discharge are equal to 30% and 70%, respectively. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{IN} = \frac{(\Delta V_{ESR})}{\left(\frac{I_{OUT}}{N} + \frac{\Delta I_L}{2}\right)} \quad (21)$$

$$C_{IN} = \frac{\frac{I_{OUT}}{N} \times D(1-D)}{\Delta V_Q \times f_{SW}} \quad (22)$$

where $I_{OUT}$ is the total output current of the multiphase converter and N is the number of phases.

For example, at $V_{OUT}$ = +1.8V, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less yielding an ESR and capacitance value of 1mΩ and 200µF.

### Output Capacitors

The worst-case peak-to-peak and capacitor RMS ripple current, the allowable peak-to-peak output ripple voltage, and the maximum deviation of the output voltage during step loads determine the capacitance and the ESR requirements for the output capacitors.

In multiphase converter design, the ripple currents from the individual phases cancel each other and lower the ripple current. The degree of ripple cancellation depends on the operating duty cycle and the number of phases. Choose the right equation from Table 3 to calculate the peak-to-peak output ripple for a given duty cycle of two-, four-, and six-phase converters. The maximum ripple cancellation occurs when $N_{PH}$ = K / D.

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

The allowable deviation of the output voltage during the fast transient load dictates the output capacitance and ESR. The output capacitors supply the load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The resistive drop across the capacitor ESR and capacitor discharge causes a voltage drop during a step load. Use a combination of SP polymer and ceramic capacitors for better transient load and ripple/noise performance.

Keep the maximum output voltage deviation less than or equal to the adaptive voltage-positioning window ($\Delta V_{OUT}$). Assume 50% contribution each from the output capacitance discharge and the ESR drop. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}} \quad (23)$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q} \quad (24)$$

where $I_{STEP}$ is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth.

### Current Limit

The average-current-mode control technique of the MAX5038A/MAX5041A accurately limits the maximum output current per phase. The MAX5038A/MAX5041A sense the voltage across the sense resistor and limit the peak inductor current ($I_{L-PK}$) accordingly. The ON cycle terminates when the current-sense voltage reaches 45mV (min). Use the following equation to calculate maximum current-sense resistor value:

$$R_{SENSE} = \frac{0.045}{\frac{I_{OUT}}{N}} \quad (25)$$

$$PD_R = \frac{2.5 \times 10^{-3}}{R_{SENSE}} \quad (26)$$

where $PD_R$ is the power dissipation in sense resistors. Select 5% lower value of $R_{SENSE}$ to compensate for any parasitics associated with the PC board. Also, select a noninductive resistor with the appropriate wattage rating.

### Reverse Current Limit

The MAX5038A/MAX5041A limit the reverse current in the case that $V_{BUS}$ is higher than the preset output voltage setting.

Calculate the maximum reverse current based on $V_{CLR}$, the reverse current-limit threshold, and the current-sense resistor:

$$I_{REVERSE} = \frac{2 \times V_{CLR}}{R_{SENSE}} \quad (27)$$

### Compensation

The main control loop consists of an inner current loop and an outer voltage loop. The MAX5038A/MAX5041A use an average-current-mode control scheme to regulate the output voltage (Figures 3a and 3b). $I_{PHASE1}$ and $I_{PHASE2}$ are the inner average current loops. The VEA output provides the controlling voltage for these current sources. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

A resistive feedback network around the VEA provides the best possible response, since there are no capacitors to charge and discharge during large-signal excursions, $R_F$ and $R_{IN}$ determine the VEA gain. Use the following equation to calculate the value for $R_F$:

$$R_F = \frac{I_{OUT} \times R_{IN}}{N \times G_C \times \Delta V_{OUT}} \quad (28)$$

$$G_C = \frac{0.05}{R_S} \quad (29)$$

where $G_C$ is the current-loop transconductance and N is the number of phases.

When designing the current-control loop ensure that the inductor downslope (when it becomes an upslope at the CEA output) does not exceed the ramp slope. This is a necessary condition to avoid subharmonic oscillations similar to those in peak-current-mode control with insufficient slope compensation. Use the following equation to calculate the resistor $R_{CF}$:

$$R_{CF} \le \frac{2 \times f_{SW} \times L \times 10^2}{V_{OUT} \times R_{SENSE}} \quad (30)$$

For example, the maximum $R_{CF}$ is 12kΩ for $R_{SENSE}$ = 1.35mΩ.

$C_{CF}$ provides a low-frequency pole while $R_{CF}$ provides a midband zero. Place a zero ($f_Z$) to obtain a phase bump at the crossover frequency. Place a high-frequency pole ($f_P$) at least a decade away from the crossover frequency to reduce the influence of the switching noise and achieve maximum phase margin. Use the following equations to calculate $C_{CF}$ and $C_{CFF}$:

$$C_{CF} = \frac{1}{2 \times \pi \times f_Z \times R_{CF}} \quad (31)$$

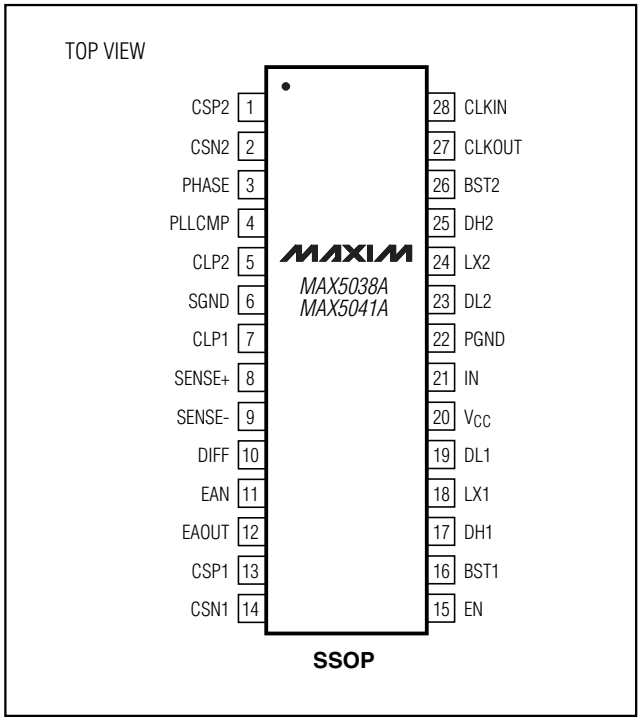
$$C_{CFF} = \frac{1}{2 \times \pi \times f_P \times R_{CF}} \quad (32)$$

### PC Board Layout

Use the following guidelines to lay out the switching voltage regulator:

1) Place the $V_{IN}$ and $V_{CC}$ bypass capacitors close to the MAX5038A/MAX5041A.
2) Minimize the area and length of the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep short the current loop formed by the lower switching MOSFET, inductor, and output capacitor.
4) Place the Schottky diodes close to the lower MOSFETs and on the same side of the PC board.
5) Keep the SGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
6) Run the current-sense lines CS+ and CS- very close to each other to minimize the loop area. Similarly, run the remote voltage sense lines SENSE+ and SENSE- close to each other. Do not cross these critical signal lines through power circuitry. Sense the current right at the pads of the current-sense resistors.
7) Avoid long traces between the $V_{CC}$ bypass capacitors, driver output of the MAX5038A/MAX5041A, MOSFET gates, and PGND. Minimize the loop formed by the $V_{CC}$ bypass capacitors, bootstrap diode, bootstrap capacitor, MAX5038A/MAX5041A, and upper MOSFET gate.
8) Place the bank of output capacitors close to the load.

## Pin Configuration




9) Distribute the power components evenly across the board for proper heat dissipation.
10) Provide enough copper area at and around the switching MOSFETs, inductor, and sense resistors to aid in thermal dissipation.
11) Use 4oz copper to keep the trace inductance and resistance to a minimum. Thin copper PC boards can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

## Chip Information

TRANSISTOR COUNT: 5431

PROCESS: BiCMOS

# Dual-Phase, Parallelable, Average-Current-Mode Controllers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.

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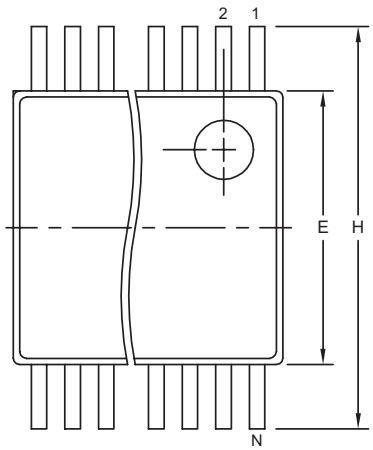
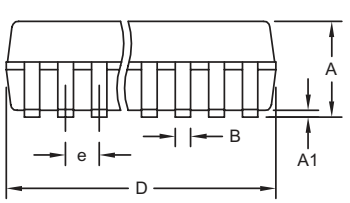
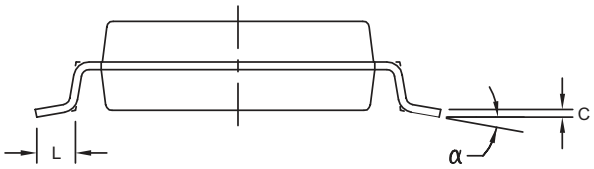



| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.068 | 0.078 | 1.73 | 1.99 |
| A1 | 0.002 | 0.008 | 0.05 | 0.21 |
| B | 0.010 | 0.015 | 0.25 | 0.38 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | SEE VARIATIONS | | | |
| E | 0.205 | 0.212 | 5.20 | 5.38 |
| e | 0.0256 BSC | | 0.65 BSC | |
| H | 0.301 | 0.311 | 7.65 | 7.90 |
| L | 0.025 | 0.037 | 0.63 | 0.95 |
| α | 0∞ | 8∞ | 0∞ | 8∞ |

| | INCHES | | MILLIMETERS | | |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N |
| D | 0.239 | 0.249 | 6.07 | 6.33 | 14L |
| D | 0.239 | 0.249 | 6.07 | 6.33 | 16L |
| D | 0.278 | 0.289 | 7.07 | 7.33 | 20L |
| D | 0.317 | 0.328 | 8.07 | 8.33 | 24L |
| D | 0.397 | 0.407 | 10.07 | 10.33 | 28L |




NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0056 | C | 1/1 |