



30V DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

Device	BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C
Q1 & Q2	001/	20mΩ @ V _{GS} = 10V	8.5A
	30V	$32m\Omega$ @ $V_{GS} = 4.5V$	5.5A

Features and Benefits

- Low Gate Threshold Voltage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

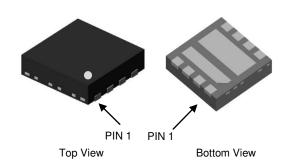
Applications

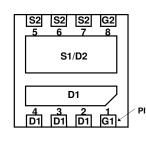
- · General Purpose Interfacing Switch
- Power Management Functions

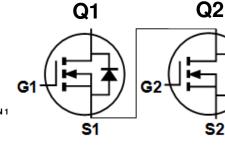
Mechanical Data

- Case: V-DFN3030-8 (Type K)
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.02 grams (Approximate)

V-DFN3030-8 (Type K)







Bottom View Internal Schematic

Equivalent Circuit

Ordering Information (Note 4)

Ī	Part Number	Case	Tape Width	Tape Pitch	Packaging
	DMT3020LDT-7	V-DFN3030-8 (Type K)	12mm	8mm	1,500/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information



AR6 = Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 18 = 2018) WW = Week Code (01 to 53)



Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Q1&Q2	Unit	
Drain-Source Voltage	V_{DSS}	30	V	
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	I _D	8.5 7.0	Α	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I _{DM}	55	Α
Maximum Body Diode Forward Current (Note 6)		Is	2.5	Α
Pulsed Body Diode Forward Current (10µs Pulse, Duty	I _{SM}	55	Α	
Avalanche Current (Note 7) L = 0.1mH	I _{AS}	11.4	Α	
Avalanche Energy (Note 7) L = 0.1mH		E _{AS}	6.5	mJ

Thermal Characteristics (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^{\circ}C$	P_{D}	0.67	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{ heta JA}$	119	°C/W
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	P_{D}	1.95	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	64	°C/W
Thermal Resistance, Junction to Case (Note 6)		R _θ JC	13.5	- C/VV
Operating and Storage Temperature Range		T _{J,} T _{STG}	-55 to +150	°C

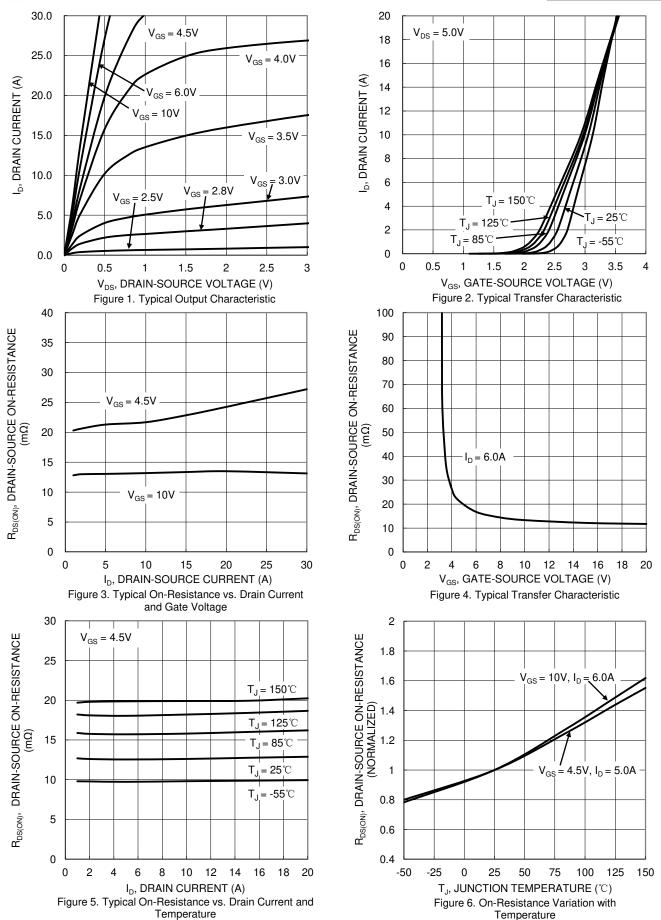
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30		_	٧	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current	I _{DSS}	_		1	μΑ	$V_{DS} = 24V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 12V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	1.0		2.5	٧	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
Static Drain-Source On-Resistance		_		20	mΩ	$V_{GS} = 10V, I_D = 6A$
Static Drain-Source On-Nesistance	R _{DS(ON)}	_	_	32	1112.2	$V_{GS} = 4.5V, I_D = 5A$
Diode Forward Voltage	V_{SD}	_	_	1.2	V	$V_{GS} = 0V, I_{S} = 2A$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	_	393	_		15) 1
Output Capacitance	Coss	_	173	_	pF	$V_{DS} = 15V$, $V_{GS} = 0V$, $f = 1.0MHz$
Reverse Transfer Capacitance	C_{rss}	_	27	_		
Gate Resistance	R_{G}	_	1.1	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$
Total Gate Charge (V _{GS} = 10V)	Q_g	_	7.0	_		
Total Gate Charge (V _{GS} = 4.5V)	Q_g	_	3.6	_	nC	V _{DD} = 15V, I _D = 9A
Gate-Source Charge	Q_{gs}	_	0.9	_	IIC	V _{DD} = 15V, I _D = 9A
Gate-Drain Charge	Q_{gd}	_	1.5	_		
Turn-On Delay Time	t _{D(ON)}	_	1.8	_		
Turn-On Rise Time	t _R	_	1.9	_	20	$V_{DD} = 15V, V_{GS} = 10V,$
Turn-Off Delay Time	t _{D(OFF)}	_	7.5	_	ns	$R_G = 6\Omega$, $I_D = 9A$
Turn-Off Fall Time	t _F	_	2.4	_		
Body Diode Reverse Recovery Time	t _{RR}	_	10	_	ns	L 0A dl/dt 100A/va
Body Diode Reverse Recovery Charge	Q _{RR}	_	2.6	_	nC	$I_F = 9A$, $dI/dt = 100A/\mu s$

- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
- 7. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
- 8. Short duration pulse test used to minimize self-heating effect.
- 9. Guaranteed by design. Not subject to product testing.









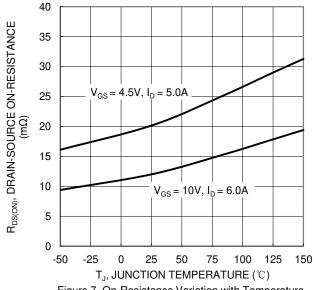


Figure 7. On-Resistance Variation with Temperature

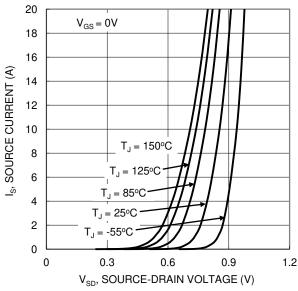


Figure 9. Diode Forward Voltage vs. Current

8

6

V_{DS} = 15V, I_D = 9A

2

0
0
2
4
6
8
10

Figure 11. Gate Charge

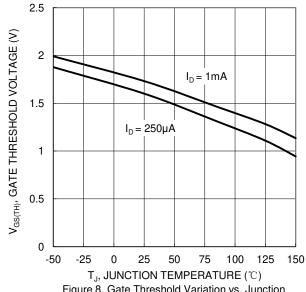
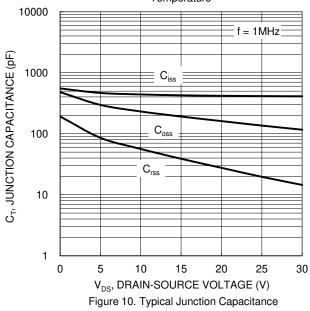


Figure 8. Gate Threshold Variation vs. Junction Temperature



100 10 ID, DRAIN CURRENT (A) = 10ms $P_W = 100 \text{ms}$ 0.1 $T_{J(Max)} = 150^{\circ}C$ $T_C = 25^{\circ}C$ Single Pulse 0.01 DUT on 1*MRP Board $V_{GS} = 10V$ 0.001 100 0.1 10 V_{DS} , DRAIN-SOURCE VOLTAGE (V)

Figure 12. SOA, Safe Operation Area

August 2018

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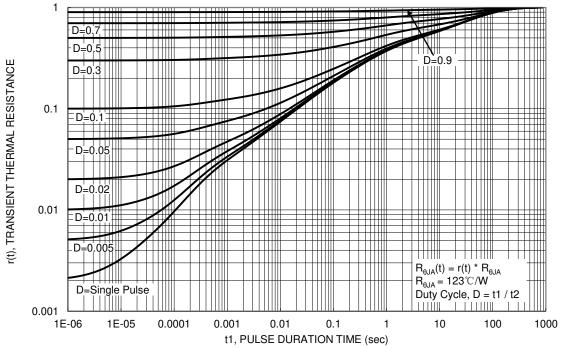


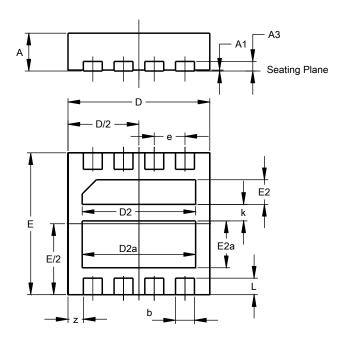
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3030-8 (Type K)

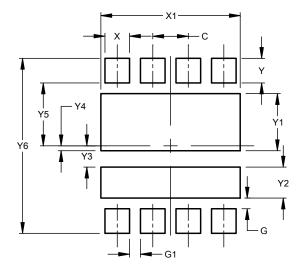


V-DFN3030-8 (Type K)								
Dim	Min	Max	Тур					
Α	0.77	0.85	0.80					
A 1	0.00	0.05	0.02					
A3	C).20BSC						
b	0.35 0.45 0.40							
D	2.95	3.050	3.00					
D2	2.30	2.50	2.40					
D2a	2.30	2.50	2.40					
Е	2.95	3.050	3.00					
E2	0.42	0.62	0.52					
E2a	0.89	1.09	0.99					
е	C).65BSC)					
k	1	-	0.35					
L	0.30	0.40	0.35					
Z	0	.325BS	С					
All	Dimensi	ons in	mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3030-8 (Type K)



Dimensions	value
Difficusions	(in mm)
С	0.650
G	0.195
G1	0.200
Х	0.450
X1	2.550
Υ	0.450
Y1	1.044
Y2	0.566
Y3	0.389
Y4	0.089
Y5	1.150
Y6	3.200

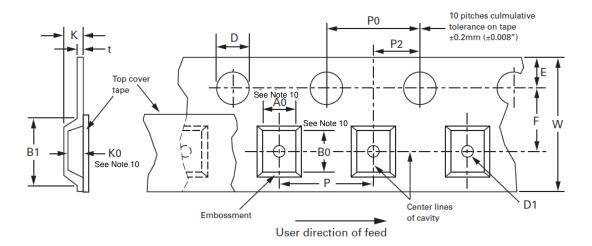


Tape and Reel Information

Please see http://www.diodes.com/_files/datasheets/ap02007.pdf for the latest version.

12mm							
Package	Suffix	Tape Orientation					
V-DFN3030-8 (Type K)	-7	Pin 1 Pin 1 Pin 1 Pin 2 Pin 2 Pin 2					

Embossed Carrier Tape Specifications



8, 12, 16, 24mm EMBOSSED TAPE DIMENSIONS IN mm								
Tape Size D E P0 t_Max A0 B0 K0 —								
12mm	1.50 +0.10 -0.0	1.75 ± 0.10	4.0 ± 0.10	0.400	See Note 10	Constant Dimensions		

Tape Size	B1 Max	D1 Min	F	K Max	P2	R Min	w	Package Type
12mm	8.2	1.5	5.5 ± 0.05	4.5	2.0 ± 0.05	30	12.0 ± 0.30	V-DFN3030-8 (Type K)

P								
Tape Size	2.0 ± 0.05	4.0 ± 0.10	8.0 ± 0.10	12.0 ± 0.10	16.0 ± 0.10			
12mm	_	_	V-DFN3030-8 (Type K)	_	_			

Note: 10. A0 B0 K0 are determined by component size.



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