



MOTOROLA

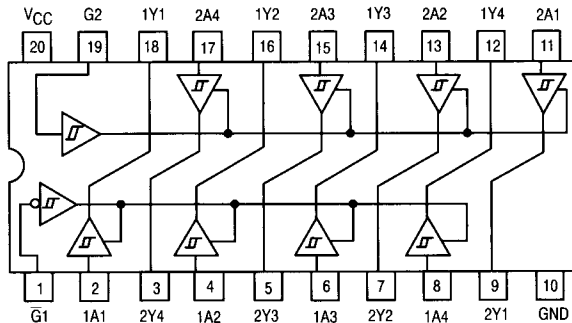
Octal Buffer/Line Driver With 3-State Outputs (Non-Inverting)

ELECTRICALLY TESTED PER:
MIL-M-38510/32402

The 54LS241 is an Octal Buffer and Line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which will provide improved PC board density.

- Hysteresis at Inputs to Improve Noise Margins
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



TRUTH TABLE

Inputs		Output
$\bar{G}1$	D	
L	L	L
L	H	H
H	X	(Z)

TRUTH TABLE

Inputs		Output
G2	D	
H	L	L
H	H	H
L	X	(Z)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance

Military 54LS241



AVAILABLE AS:

- 1) JAN: JM38510/32402BXA
- 2) SMD: N/A
- 3) 883: 54LS241/BXAJC

X = CASE OUTLINE AS FOLLOWS:
 PACKAGE: CERDIP: R
 CERFLAT: S
 LCC: 2

THE LETTER "M" APPEARS
 BEFORE THE / ON LCC.

PIN ASSIGNMENTS

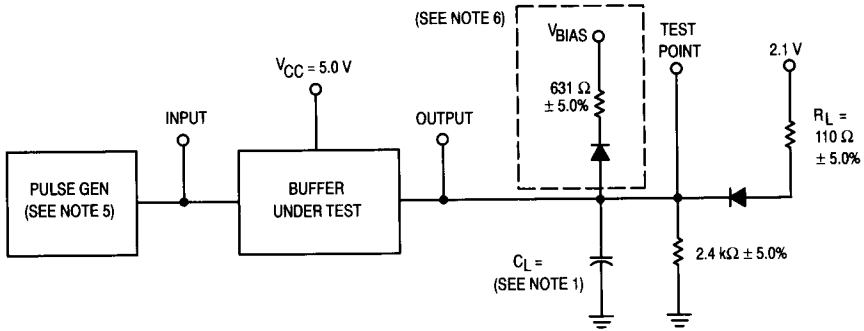
FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\bar{G}1$	1	1	1	GND
1A1	2	2	2	V _{CC}
2Y4	3	3	3	V _{CC}
1A2	4	4	4	V _{CC}
2Y3	5	5	5	V _{CC}
1A3	6	6	6	V _{CC}
2Y2	7	7	7	V _{CC}
1A4	8	8	8	V _{CC}
2Y1	9	9	9	V _{CC}
GND	10	10	10	GND
2A1	11	11	11	V _{CC}
1Y4	12	12	12	V _{CC}
2A2	13	13	13	V _{CC}
1Y3	14	14	14	V _{CC}
2A3	15	15	15	V _{CC}
1Y2	16	16	16	V _{CC}
2A4	17	17	17	V _{CC}
1Y1	18	18	18	V _{CC}
G2	19	19	19	V _{CC}
V _{CC}	20	20	20	V _{CC}

BURN-IN CONDITIONS:

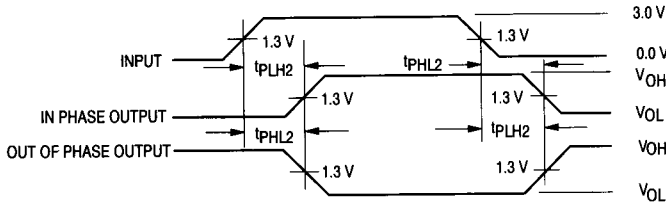
V_{CC} = 5.0 V MIN/6.0 V MAX

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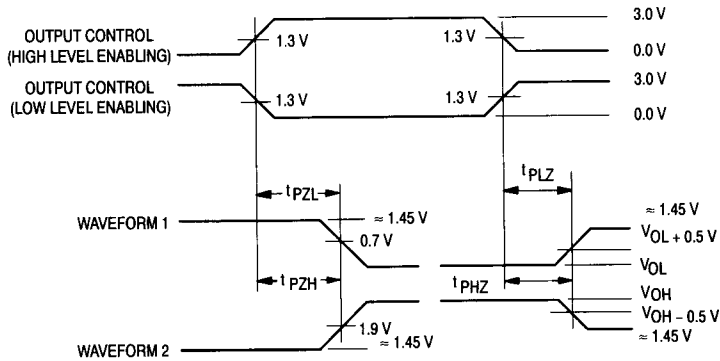
AC TEST CIRCUIT



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



REFERENCE NOTES ON PAGE 5-301

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OHH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = - 3.0 mA, V _{IN} = 2.0 V (other inputs are open), $\bar{G}1/G2 = 0.7$ V/2.0 V or open per truth table.
V _{OHL}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V, I _{OH} = - 12 mA, V _{IN} = 2.0 V (other inputs are open), $\bar{G}1/G2 = 0.5$ V/2.0 V or open per truth table.
V _{OL1}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 12 mA, V _{IN} = 0.7 V (other inputs are open), $\bar{G}1/G2 = 0.7$ V/2.0 V or open per truth table.
V _{OL2}	Logical "0" Output Voltage		0.45		0.45		0.45	V	V _{CC} = 4.5 V, I _{OL} = 18 mA, V _{IN} = 0.7 V (other inputs are open), $\bar{G}1/G2 = 0.7$ V/2.0 V or open per truth table.
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, all other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{IL}	Logical "0" Input Current	- 5.0	- 200	- 5.0	- 200	- 5.0	- 200	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs are open.
I _{OS}	Output Short Circuit Current	- 40	- 225	- 40	- 225	- 40	- 225	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (other inputs are open), V _{OUT} = GND, $\bar{G}1/G2 = GND/5.5$ V or open per truth table.
I _{IOZH}	Output Off Current High		20		20		20	μA	V _{CC} = 5.5 V, all inputs are open, V _{OUT} = 2.7 V, $\bar{G}1/G2 = 2.0$ V/0.7 V or open per truth table.
I _{IOZL}	Output Off Current Low		- 20		- 20		- 20	μA	V _{CC} = 5.5 V, all inputs are open, V _{OUT} = 0.4 V, $\bar{G}1/G2 = 2.0$ V/0.7 V or open per truth table.
I _{CCH}	Power Supply Current		27		27		27	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), $\bar{G}1 = GND$, G2 = 5.5 V.
I _{CCCL}	Power Supply Current		46		46		46	mA	V _{CC} = 5.5 V, V _{IN} = GND (all inputs), $\bar{G}1/G2 = 5.5$ V.
I _{CCZ}	Power Supply Current Off		54		54		54	mA	V _{CC} = 5.5 V, all inputs are open, $\bar{G}1/G2 = GND$.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output Output High-Low	2.0 —	18 18	2.0 —	23 23	2.0 —	23 23	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω. V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output Output Low-High	2.0 —	18 18	2.0 —	23 23	2.0 —	23 23	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω. V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PLZ1} t _{PLZ1}	Propagation Delay /Data-Output Output Low-High	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω. V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PHZ1} t _{PHZ1}	Propagation Delay /Data-Output Output High-Low	2.0 —	35 18	2.0 —	45 40	2.0 —	45 40	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω. V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PZL1} t _{PZL1}	Propagation Delay /Data-Output Output Low-High	2.0 —	30 30	2.0 —	39 34	2.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω. V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PZH1} t _{PZH1}	Propagation Delay /Data-Output Output High-Low	2.0 —	30 23	2.0 —	39 34	2.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω. V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.

NOTES:

- C_L = 50 pF ± 10%. C_L includes scope probe and jig capacitance.
- All diodes are 1N3064 or equivalent.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- In the test circuit example, the phase relationships between inputs and outputs have been chosen arbitrarily.
- All input pulses are supplied by generators having the following characteristics:
PRR ≤ 1.0 MHz, t_p = 500 ns, Z_{OUT} = 50 Ω, V_{gen} = 3.0 V, t_r ≤ 15 ns and t_f ≤ 6.0 ns between 0.7 V and 2.7 V.
- The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}, for t_{PHZ} tests, V_{BIAS} shall be - 0.6 V.