BLP8G10S-270PW

Power LDMOS transistor

Rev. 2 — 1 October 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

270 W LDMOS packaged symmetric Doherty power transistor for base station applications at frequencies from 700 MHz to 900 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a Doherty application test circuit. V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	716 to 768	28	47.5	17.3	46	–35 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.65 dB at 0.01% probability on CCDF per carrier.

1.2 Features and benefits

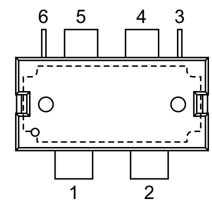
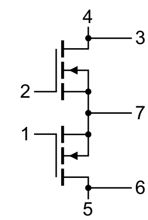
- Excellent ruggedness
- High-efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Bias through video leads
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 700 MHz to 900 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1, 2	gate		
3, 6	bias/video decoupling		
4, 5	drain		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP8G10S-270PW	HSOP6F	plastic, heatsink small outline package; 6 leads (flat)	SOT1221-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		−0.5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 28 V; I_{Dq} = 650 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 80 °C;		
		P_L = 56 W	0.50	K/W
		P_L = 89 W	0.43	K/W

6. Characteristics

Table 6. DC characteristics

Per section; T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.25 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 225 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1000 mA	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	37.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11.25 mA	-	14	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7875 mA	-	90	148	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.65 dB at 0.01 % probability on the CCDF per carrier; f_1 = 718.5 MHz; f_2 = 765.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 2000 mA (main); T_{case} = 25 °C; unless otherwise specified; in a class AB production test circuit at frequencies from 716 MHz to 768 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 56 W	19	20	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 56 W	-	−16	−12	dB
η_D	drain efficiency	$P_{L(AV)}$ = 56 W	25	29	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 56 W	-	−38	−33	dBc

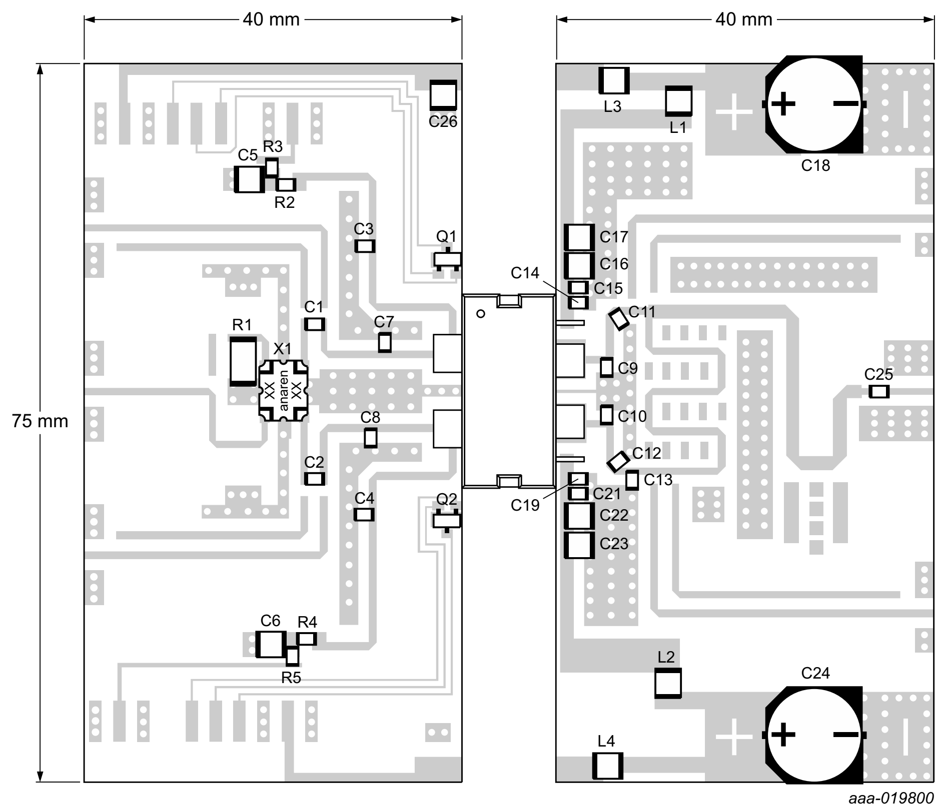
Table 8. RF characteristics

Test signal: pulsed RF; f_1 = 718.5 MHz; f_2 = 756.5 MHz; t_p = 10 ms; δ = 10 %; RF performance at V_{DS} = 28 V; I_{Dq} = 2000 mA (main); T_{case} = 25 °C; unless otherwise specified; in a class-AB narrow band production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression		315	365	-	W

7. Application information

7.1 Application circuit



Printed-Circuit Board (PCB): Rogers RO3006: ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 70 μm. See Table 11 for a list of components.

Fig 1. Component layout

Table 9. List of components

See Figure 15 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C14, C19, C25	multilayer ceramic chip capacitor	82 pF	ATC 600F
C5, C6, C16, C17, C22, C23, C26	multilayer ceramic chip capacitor	10 μF	Murata: GRM32ER71H106KA12
C7, C8, C9, C10	multilayer ceramic chip capacitor	15 pF	ATC 600F
C11, C12	multilayer ceramic chip capacitor	5.6 pF	ATC 600F
C13	multilayer ceramic chip capacitor	1.8 pF	ATC 600F
C15, C21	multilayer ceramic chip capacitor	1 μF	Murata: GRM31CR72A105KA01L
C18, C24	electrolytic capacitor	2200 μF	Multicomp: MCGPR35V228M16X32
L1, L2, L3, L4	chip ferrite bead	-	Murata; BLE32PN300SN1L
Q1, Q2	transistor	-	Fairchild: MMBT2222
R1	resistor	50 Ω	Panasonic: ERJ-L14KF50MU
R2, R4	resistor	1.1 kΩ	Vishay Dale

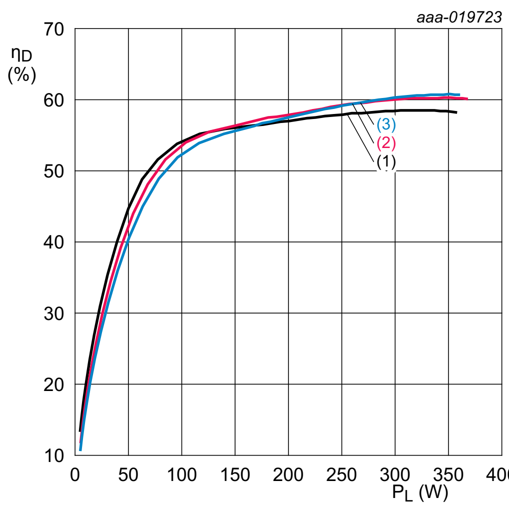
Table 9. List of components

See Figure 15 for component layout.

Component	Description	Value	Remarks
R3	resistor	1.2 kΩ	Vishay Dale
R5	resistor	3.9 kΩ	Vishay Dale
X1	hybrid coupler	3 dB, 90°	Anaren: X3C07P1-03S

7.2 Graphical data measured at frequency band from 716 MHz to 768 MHz

7.2.1 Pulsed CW



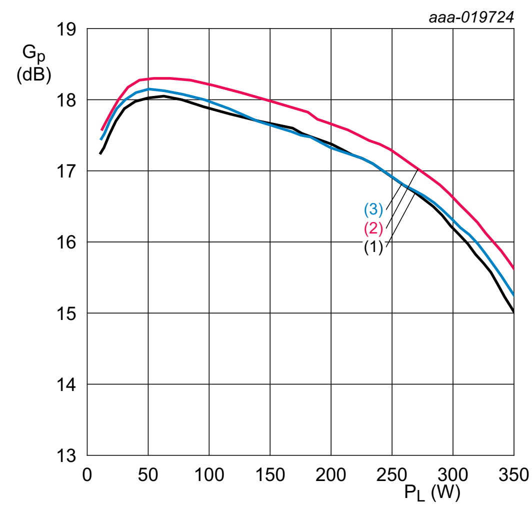
V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V; t_p = 100 μs; δ = 10 %.

(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

Fig 2. Drain efficiency as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V; t_p = 100 μs; δ = 10 %.

(1) f = 716 MHz

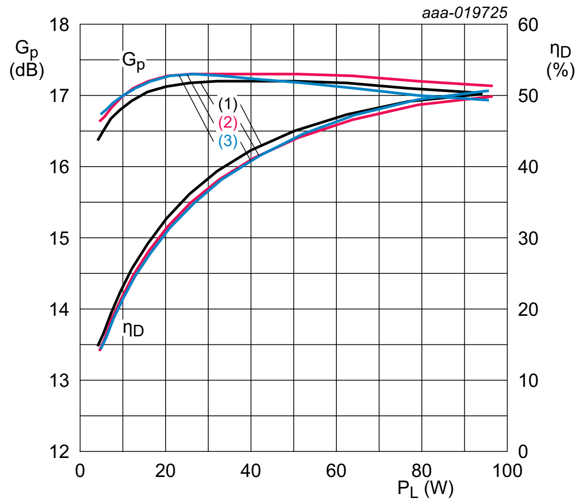
(2) f = 742 MHz

(3) f = 768 MHz

Fig 3. Power gain as a function of output power; typical values

7.2.2 1-Carrier W-CDMA

PAR = 9.7 dB per carrier at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (100 % clipping).



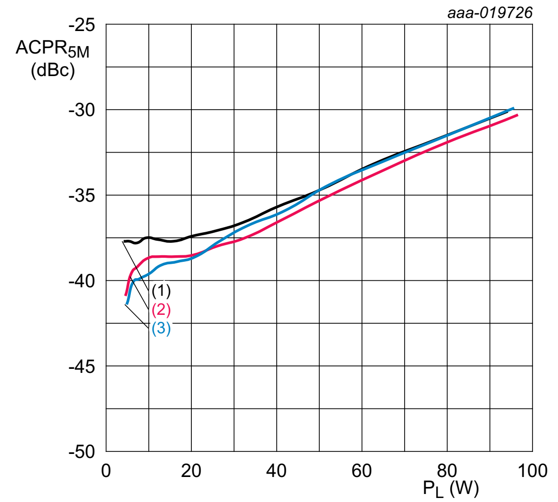
V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



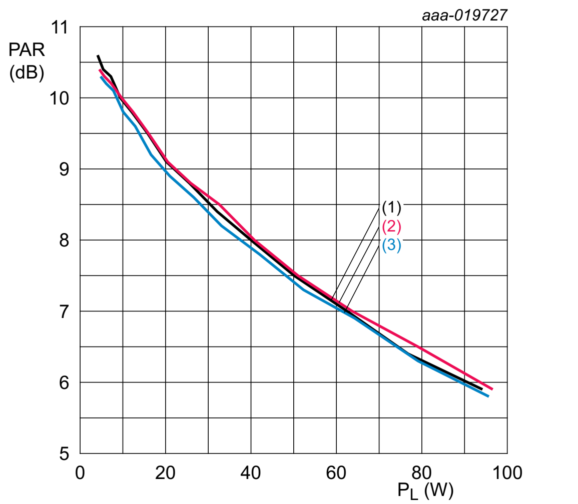
V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



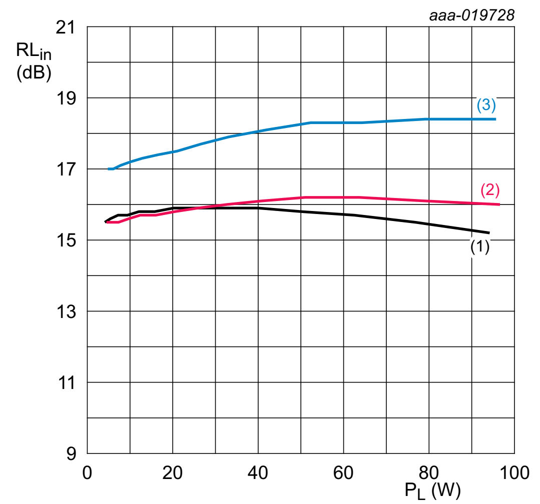
V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 716 MHz

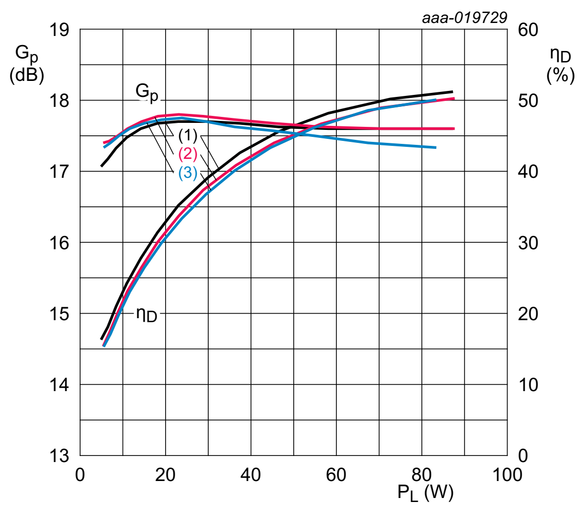
(2) f = 742 MHz

(3) f = 768 MHz

Fig 7. Input return loss as a function of output power; typical values

7.2.3 2-Carrier W-CDMA

PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (46 % clipping).



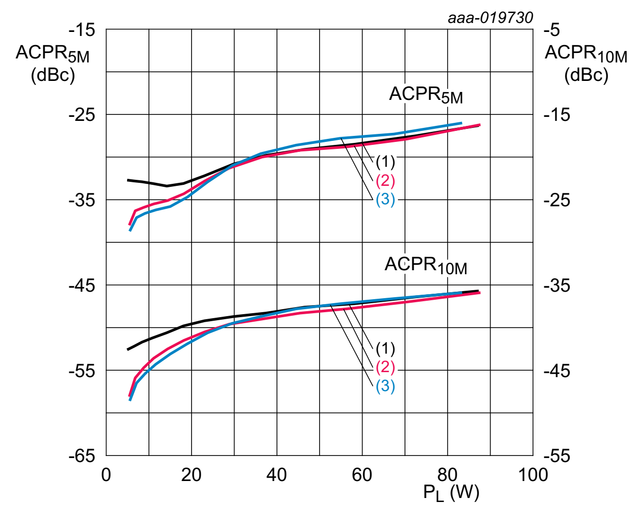
V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



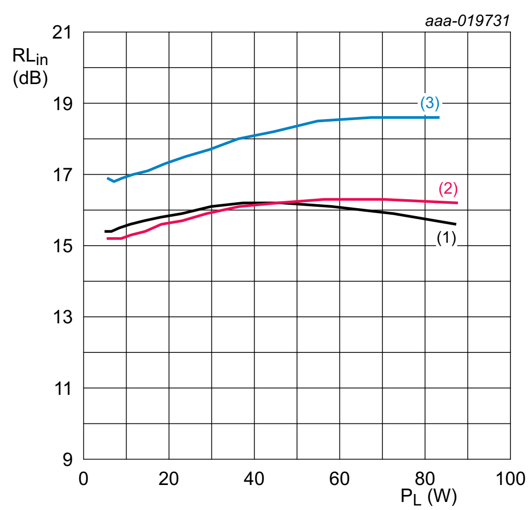
V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

Fig 9. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.50 V.

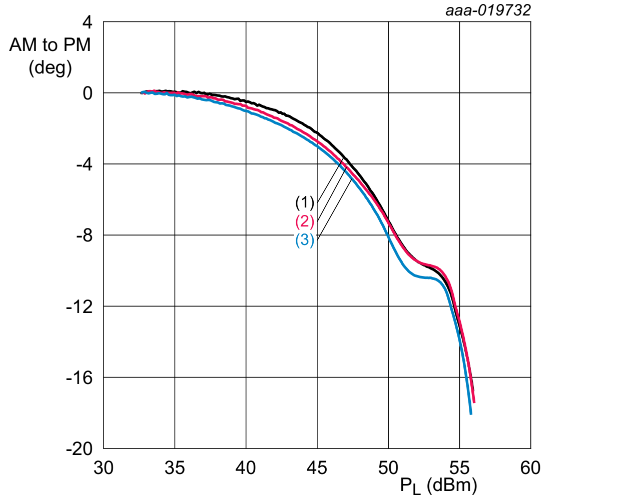
(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

Fig 10. Input return loss as a function of output power; typical values

7.2.4 CW



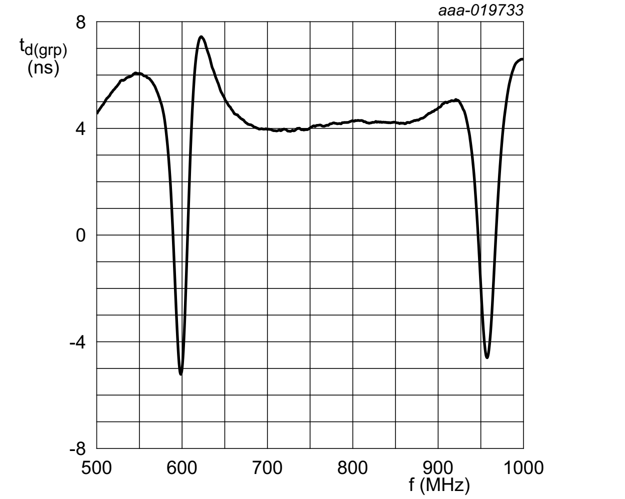
V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 716 MHz

(2) f = 742 MHz

(3) f = 768 MHz

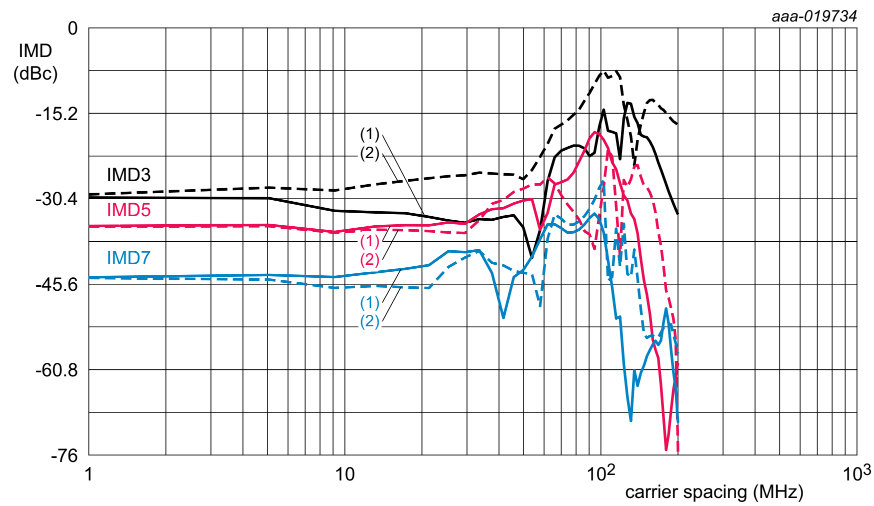
Fig 11. AM to PM as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.50 V.
P_L = 27.5 dBm.

Fig 12. Group delay time as a function of frequency; typical values

7.2.5 2-Tone VBW



V_{DS} = 28 V; I_{Dq} = 500 mA (main device); $V_{GS(amp)peak}$ = 0.50 V; f = 742 MHz.

(1) IMD low

(2) IMD high

Fig 13. VBW capability in Doherty demo

8. Test information

8.1 Ruggedness in Doherty operation

The BLP8G10S-270PW is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 2000 mA; f =719 MHz. Test signal: 1-carrier W-CDMA; P_L = 85 W (5 dB OBO); 100 % clipping

8.2 Impedance information

Table 10. Typical impedance of main or peak device

Measured load-pull data of main device; I_{Dq} = 700 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
728	3.1 – j0.8	1.3 – j2.0	261.2	60.0	17.3
748	3.1 – j1.1	1.3 – j1.9	258.6	60.6	17.3
768	3.1 – j1.4	1.3 – j1.9	252.1	60.3	17.4
869	4.4 – j2.2	1.4 – j2.6	240.6	60.1	17.3
880	4.7 – j2.3	1.3 – j2.6	237.3	59.9	17.3
894	5.1 – j2.0	1.3 – j2.6	235.9	60.5	17.3
Maximum drain efficiency load					
728	3.1 – j0.8	3.5 – j1.1	164.7	73.4	20.0
748	3.1 – j1.1	3.5 – j0.7	150.3	73.2	20.2
768	3.1 – j1.4	3.2 – j0.7	150.3	72.2	20.0
869	4.4 – j2.2	2.4 – j1.0	141.9	71.4	19.8
880	4.7 – j2.3	2.4 – j1.0	136.7	70.4	19.7
894	5.1 – j2.0	2.0 – j1.4	155.9	70.3	19.3

[1] Z_S and Z_L defined in Figure 14.

[2] At 3 dB gain compression.

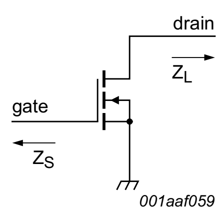
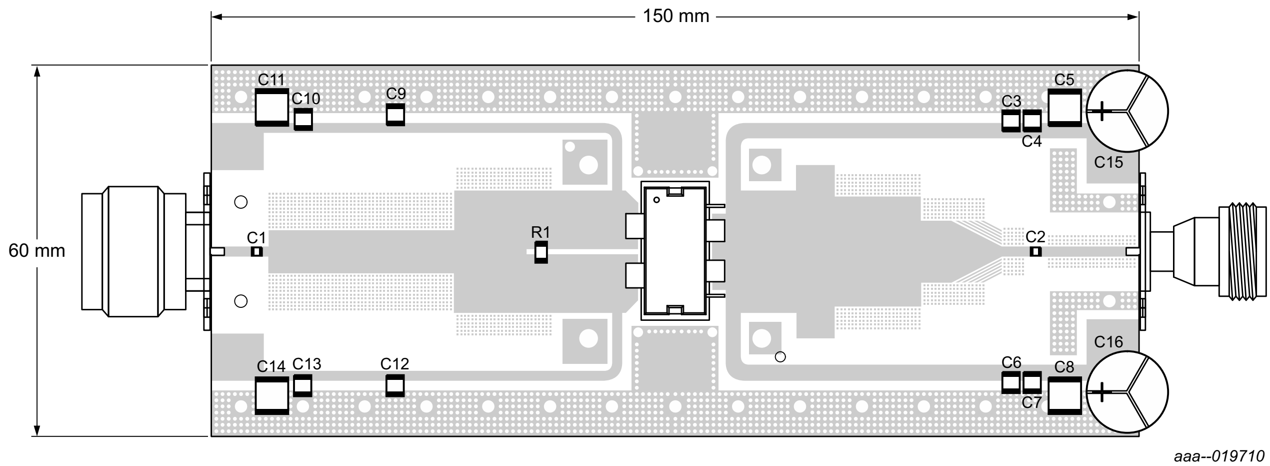


Fig 14. Definition of transistor impedance

8.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B: thickness = 0.762 mm; thickness copper plating = 35 μm. See Table 11 for a list of components.

Fig 15. Component layout

Table 11. List of components
See Figure 15 for component layout.

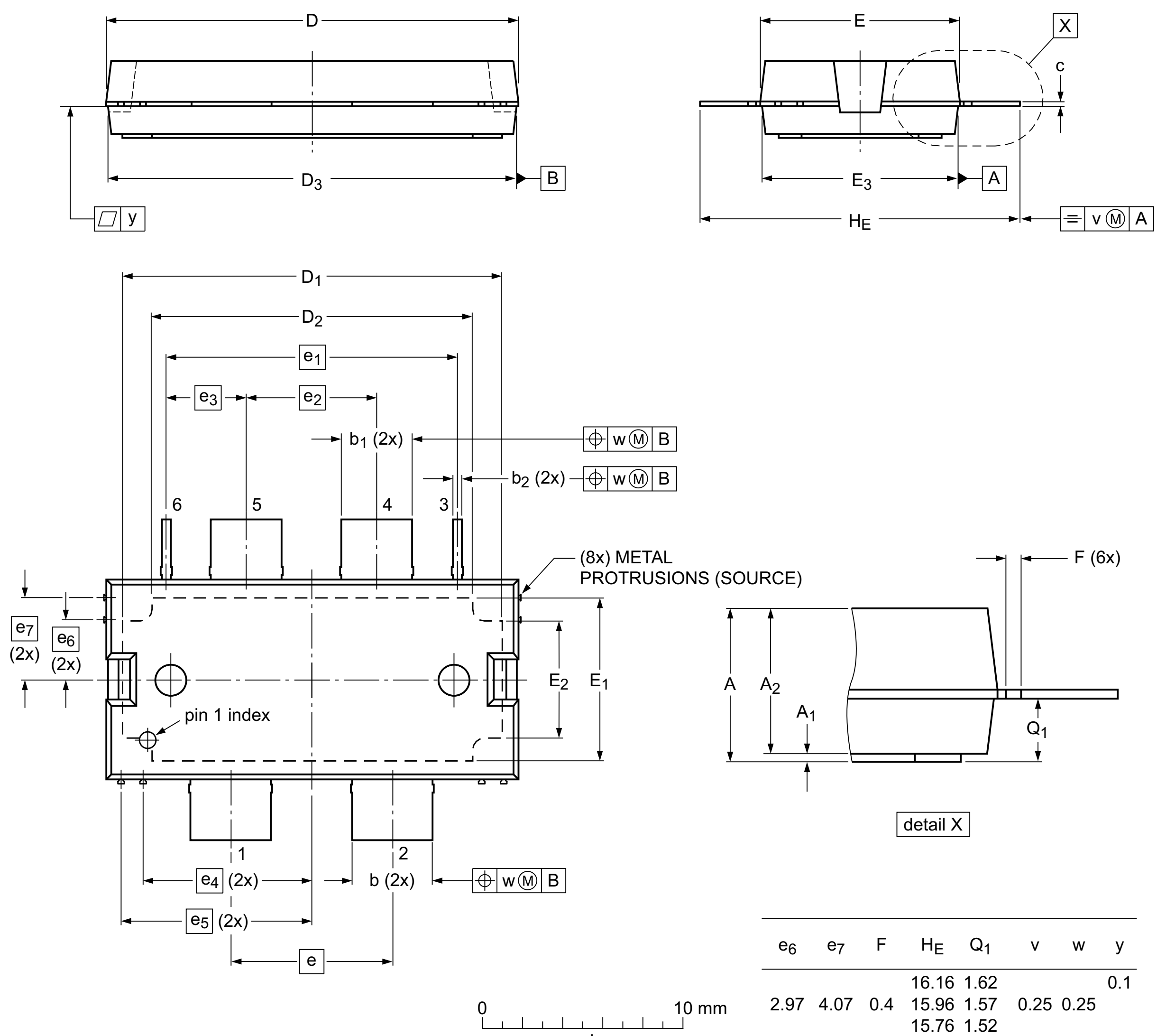
Component	Description	Value	Remarks
C1, C3, C6, C9, C12	multilayer ceramic chip capacitor	82 pF [1]	ATC 800B
C2	multilayer ceramic chip capacitor	180 pF [1]	ATC 800B
C4, C7, C10, C13	multilayer ceramic chip capacitor	1 μF [2]	Murata
C5, C8, C11, C14	multilayer ceramic chip capacitor	10 μF, 50 V [2]	Murata
C15, C16	electrolytic capacitor	2200 μF, 63 V	
R1	resistor	5 kΩ	SMD 1206

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] Murata or capacitor of same quality.

9. Package outline

HSOP6F: plastic, heatsink small outline package; 6 leads(flat) **SOT1221-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	b_1	b_2	c	$D^{(1)}$	D_1	D_2	D_3	$E^{(1)}$	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	e_5	e_6	e_7	F	H_E	Q_1	v	w	y
mm	max	3.9	0.2	3.65	4.05	3.55	0.50	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83										16.16	1.62			0.1
	nom		0.1	3.60	4.00	3.50	0.45	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	8.0	14.5	6.5	4.0	8.45	9.55	2.97	4.07	0.4	15.96	1.57	0.25	0.25	
	min		0	3.55	3.95	3.45	0.40	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73										15.76	1.52			

Note

1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimensions “b, “ b_1 and “ b_2 do not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.

sot1221-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1221-2		- - -				~~15-01-12~~ 15-06-08

Fig 16. Package outline SOT1221-2 (HSOP6F)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back-Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
SMD	Surface Mounted Device
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP8G10S-270PW v.2	20151001	Product data sheet	-	BLP8G10S-270PW v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon • Legal texts have been adapted to the new company name where appropriate			
BLP8G10S-270PW v.1	20150917	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contact information

For more information, please visit: **http://www.ampleon.com**

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