0.1 GHz to 50 GHz, GaAs, MMIC Reflective SPDT Switch

Data Sheet **HMC986A**

FEATURES

- Broadband frequency range: 0.1 GHz to 50 GHz
- Reflective 50 Ω design
- Low insertion loss: 2.3 dB at 50 GHz
- High isolation: 30 dB at 50 GHz
- High input linearity
  - 1 dB power compression (P1dB): 28 dBm typical
  - Third-order intercept (IP3): 40 dBm typical
- High power handling
  - 27 dBm through path
- 13-pad, 0.98 mm × 0.75 mm × 0.1 mm, CHIP

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, and electronic counter measures (ECMs)
- Broadband telecommunications systems

FUNCTIONAL BLOCK DIAGRAM

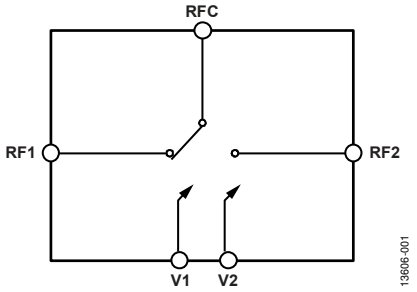

Figure 1.

GENERAL DESCRIPTION

The HMC986A is a reflective, single-pole, double throw (SPDT) switch, manufactured using a gallium arsenide (GaAs) process. This switch typically provides low insertion loss of 2.3 dB and high isolation of 30 dB in broadband frequency range from 0.1 GHz to 50 GHz.

This switch operates with two negative logic control voltages from −5 V to −3 V. All electrical performance data is acquired with the RFx pads of the HMC986A connected to 50 Ω transmission lines via one 3.0 mil × 0.5 mil ribbon bond of minimal length.

Rev. B
Document Feedback

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REVISION HISTORY

7/2019—Rev. A to Rev. B

Deleted Figure 1; Renumbered Sequentially 1
Added Figure 1; Renumbered Sequentially 1
Changes to Features Section and General Description Section 1
Changes to Specifications Section and Table 1 3
Added Figure 2, Thermal Resistance Section, and Table 3; Renumbered Sequentially 4
Changes to Table 2 4
Added Figure 3, Figure 4, and Figure 5 5
Changes to Table 4 5
Added Figure 6 to Figure 9 6
Added Figure 10 to Figure 15 .....

SPECIFICATIONS

V_{CTL} = −5 V to −3 V or 0V, T_{DIE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BROADBAND FREQUENCY RANGE	f		0.1		50	GHz
INSERTION LOSS		0.1 GHz to 18 GHz		1.7	2.3	dB
		18 GHz to 40 GHz		1.9	2.5	dB
		40 GHz to 50 GHz		2.3	2.8	dB
ISOLATION						
Between RFC and RF1 to RF2		0.1 GHz to 18 GHz	30	36		dB
		18 GHz to 40 GHz	25	32		dB
		40 GHz to 50 GHz	22	30		dB
RETURN LOSS						
RFC and RF1/RF2		0.1 GHz to 18 GHz		15		dB
		18 GHz to 40 GHz		15		dB
		40 GHz to 50 GHz		13		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		2		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		11		ns
INPUT LINEARITY[1]		2 GHz to 50 GHz				
1 dB Compression	P1dB	V_{CTL} = −5 V/0 V	22	28		dBm
		V_{CTL} = −3 V/0 V		25		dBm
0.1 dB Compression	P0.1dB	V_{CTL} = −5 V/0 V		25		dBm
		V_{CTL} = −3 V/0 V		22		dBm
Third-Order Intercept	IP3	0 dBm per tone, 1 MHz spacing				
		V_{CTL} = −5 V/0 V		40		dBm
		V_{CTL} = −3 V/0 V		40		dBm
DIGITAL CONTROL INPUTS		V_1 and V_2 pins				
Voltage	V_{CTL}					
Low	V_{INL}		−0.2	0	+0.2	V
High	V_{INH}		−5		−3	V
Current	I_{CTL}					
Low	I_{INL}	V_{CTL} = 0 V		1		µA
High	I_{INH}	V_{CTL} = −5 V to −3 V		10		µA

[1] For input linearity performance over frequency, see Figure 11 to Figure 13.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Digital Control Input Voltage	−5.5 V to +0.5 V
RF Input Power[1] (f = 2 GHz to 50 GHz, T_{DIE} = 85°C)	
V_{CTL} = −5 V/0 V	
Through Path	27 dBm
Hot Switching	24 dBm
V_{CTL} = −3 V/0 V	
Through Path	24 dBm
Hot Switching	21 dBm
Temperature	
Junction Temperature, T_J	150°C
Die Bottom Temperature Range, T_{DIE}	−55°C to +85°C
Storage Temperature Range	−65°C to +150°C
ESD Sensitivity	
Human Body Model (HBM)	150 V (Class 0)

[1] For power derating at frequencies less than 2 GHz, see Figure 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

POWER DERATING CURVE

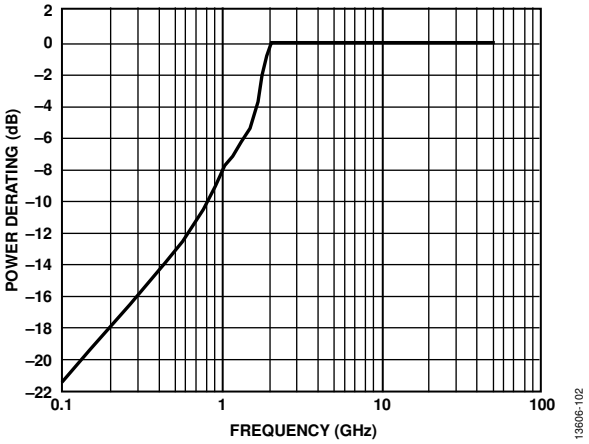

Figure 2. Power Derating at Frequencies <2 GHz

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 3.

Package Option	θ_{JC}	Unit
C-13-1	260	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

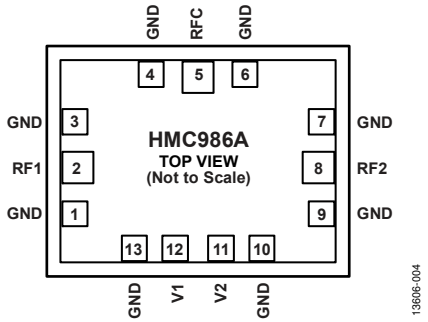

Figure 3. Pin Configuration

Table 4. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 6, 7, 9	GND	Analog Ground. These pads are connected to die backside ground and can be used to achieve a ground to signal to ground interface for optimum RF performance. The performance of the HMC986A is measured with a Ground-Signal-Ground interface on RF1, RFC, and RF2.
2	RF1	RF Throw Pad 1. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
5	RFC	RF Common Pad. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
8	RF2	RF Throw Pad 2. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
10, 13	GND	Ground. These pads are connected to die backside ground and are optional for use as V_1, V_2 control signal ground return.
11	V_2	Control Input 2. See Table 5. See Figure 5 for the interface schematic.
12	V_1	Control Input 1. See Table 5. See Figure 5 for the interface schematic.
Die Bottom	GND	Ground. The Die bottom must be attached directly to the ground plane eutectically or with conductive epoxy.

INTERFACE SCHEMATICS

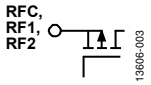

Figure 4. RFC to RF1/RF2 Interface Schematic

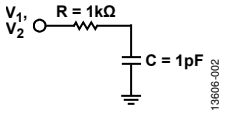

Figure 5. V_1 and V_2 Control Input Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

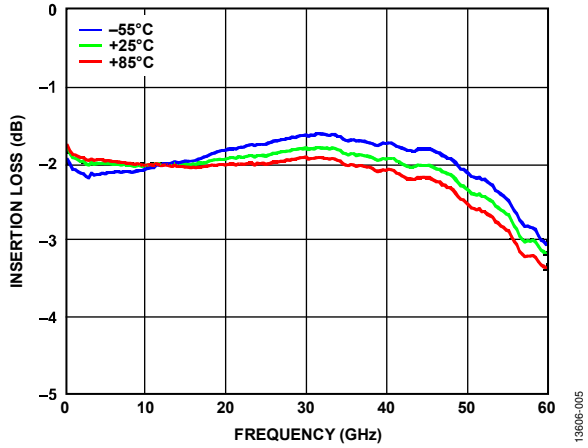

Figure 6. Insertion Loss Between RFC and RF1 vs. Frequency over Temperature

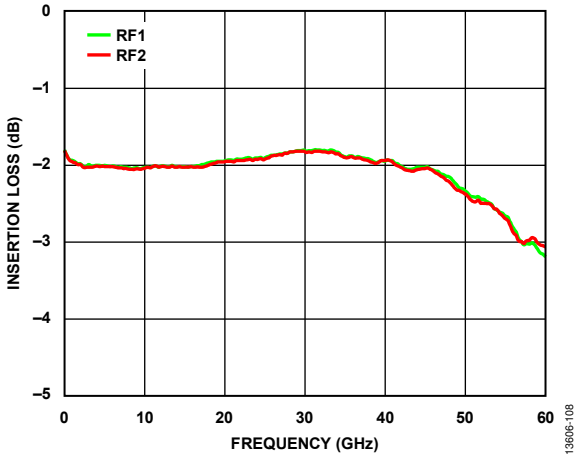

Figure 8. Insertion Loss Between RFC and RF1/RF2 vs. Frequency

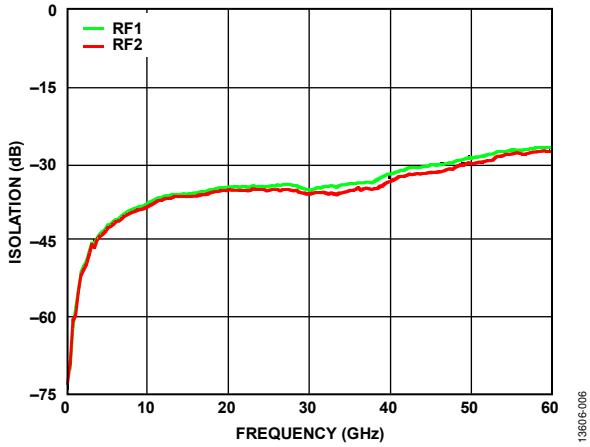

Figure 7. Isolation Between RFC and RF1/ RF2 vs. Frequency

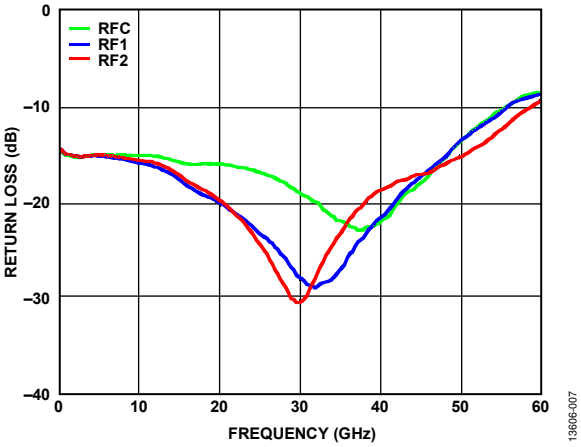

Figure 9. Return Loss for RFC, RF1 ON and RF2 ON vs. Frequency

INPUT POWER COMPRESSION (P1dB) AND THIRD-ORDER INTERCEPT (IP3)

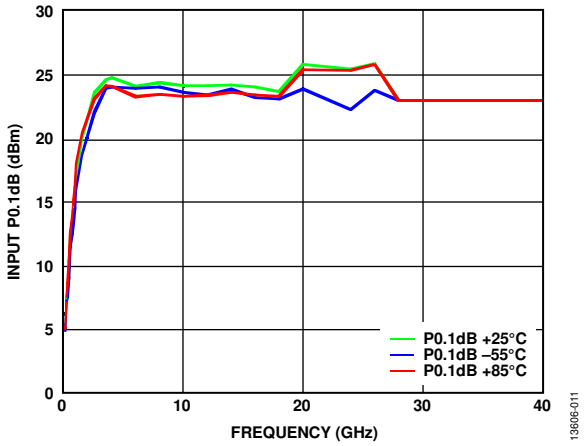

Figure 10. Input P0.1dB vs. Frequency over Temperature, V_{CTL} = –5 V

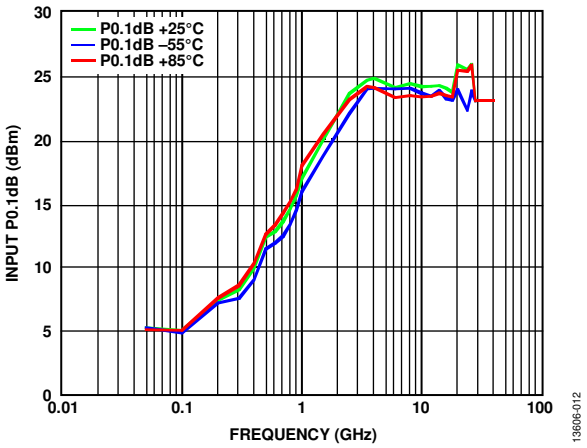

Figure 11. Input P0.1dB vs Low Frequency over Temperature, V_{CTL} = –5 V

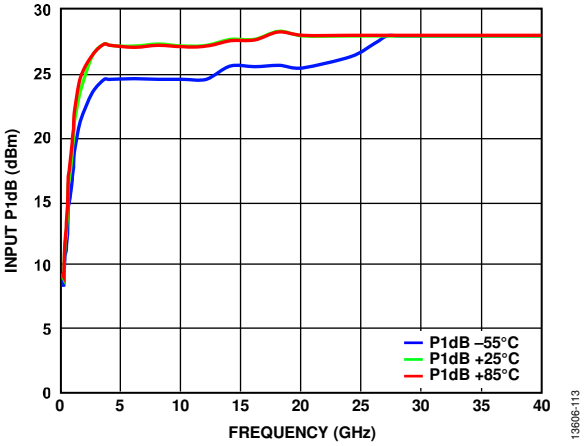

Figure 12. Input P1dB vs. Frequency over Temperature, V_{CTL} = –5 V

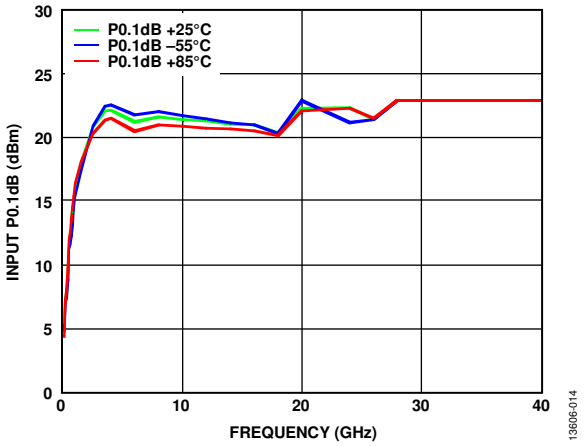

Figure 13. Input P0.1dB vs Frequency over Temperature, V_{CTL} = –3 V

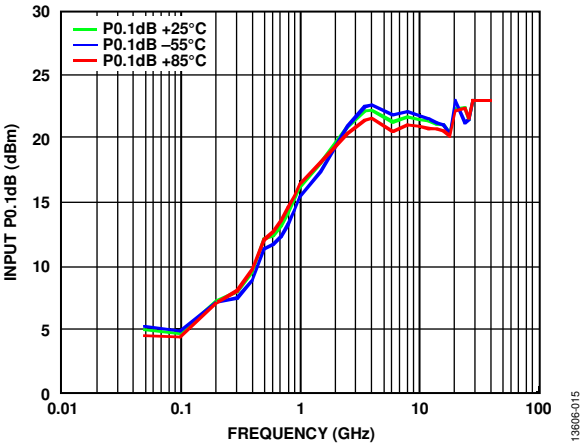

Figure 14. Input P0.1dB vs. Low Frequency over Temperature, V_{CTL} = –3 V

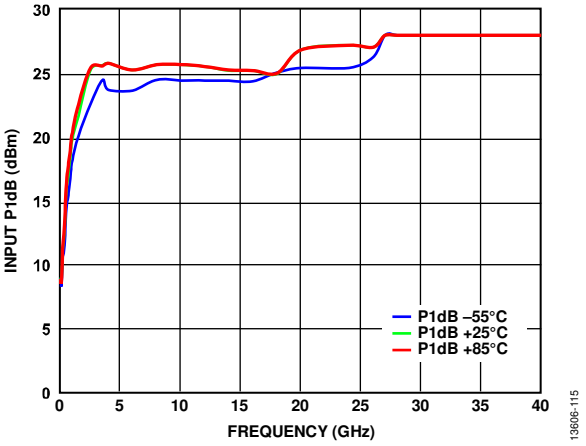

Figure 15 Input P1dB vs. Low Frequency over Temperature, V_{CTL} = –3 V

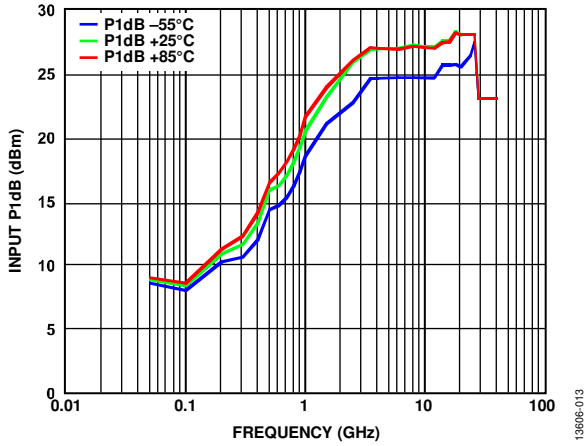

Figure 16. Input P1dB vs. Low Frequency over Temperature, V_{CTL} = –5 V

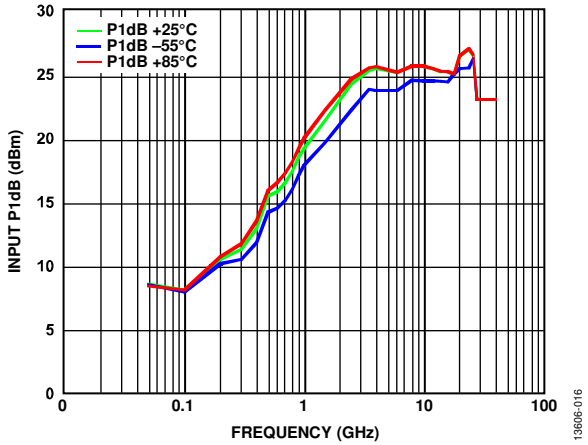

Figure 19. Input P1dB vs. Low Frequency over Temperature, V_{CTL} = –3 V

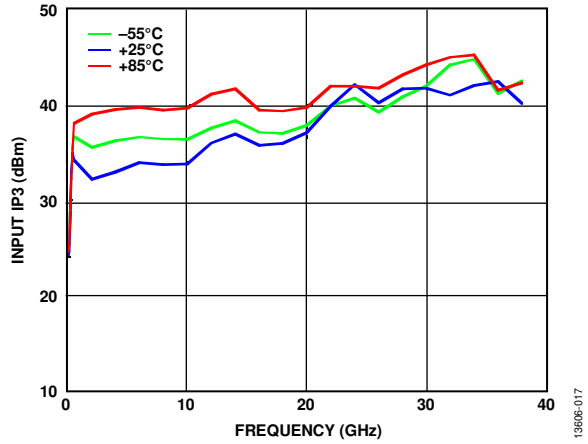

Figure 17. Input IP3 vs Frequency over Temperature, V_{CTL} = –5 V

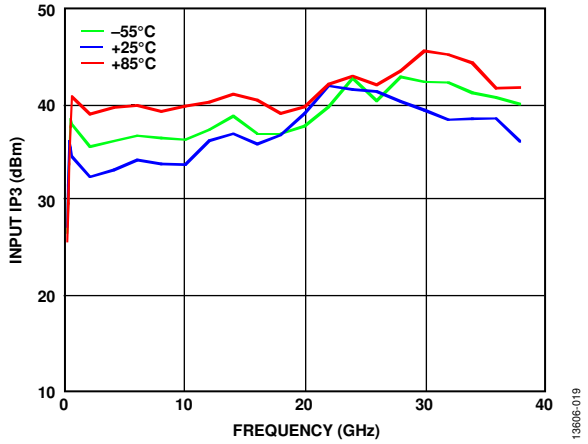

Figure 20. Input IP3 vs. Frequency over Temperature, V_{CTL} = –3 V

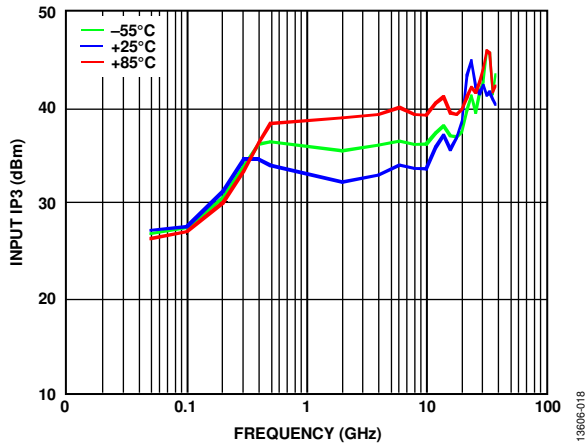

Figure 18. Input IP3 vs. Low Frequency over Temperature, V_{CTL} = –5 V

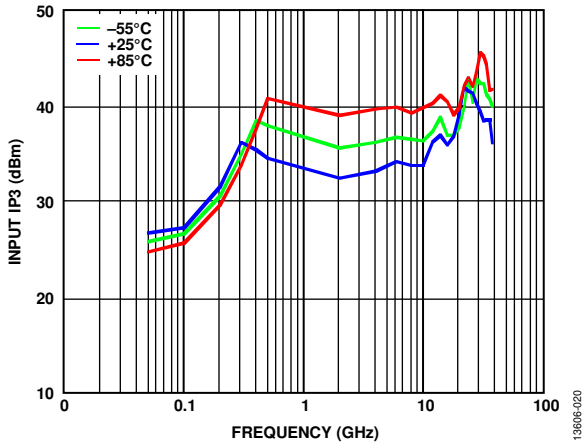

Figure 21 Input IP3 vs. Low Frequency over Temperature, V_{CTL} = –3 V

THEORY OF OPERATION

The HMC986A requires two logic control inputs at the V_1 and V_2 pads to control the state of the RF paths.

Depending on the logic level applied to the V_1 and V_2 pads, one RF path is in the insertion loss state while the other path is in an isolation state (see Table 5). The insertion loss path conducts the RF signal between the RF throw pad and RF common pad. The unselected RF port of the HMC986A is reflective. The isolation path provides high isolation between the unselected port and the insertion loss path.

The ideal power-up sequence is as follows:

1. Ground to the die bottom.
2. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{CTL} supply can inadvertently become forward-biased and damage the internal electrostatic discharge (ESD) protection structures.
3. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC pad while the RF throw pads are the outputs or the RF input signal can be applied to the RF throw pads while the RFC pad is the output. All of the RF pads are dc-coupled to 0 V, and no dc blocking is required at the RF pads when the RF line potential is equal to 0 V.

The power-down sequence is the reverse of the power-up sequence.

Table 5. Control Voltage Truth Table

Digital Control Input			
V_1	**V_2**	**RF1 to RFC**	**RF2 to RFC**
High	Low	Insertion loss (on)	Isolation (off)
Low	High	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

MOUNTING AND BONDING TECHNIQUES

The HMC986A is back metallized and must be attached directly to the ground plane with gold tin (AuSn) eutectic preforms or with electrically conductive epoxy.

The die thickness is 0.102 mm (4 mil). The 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the HMC986A (see Figure 22).

The HMC986A must be raised 0.150 mm (6 mil) when using 0.254 mm (10 mil) thick alumina thin film substrates so that the surface of the HMC986A is coplanar with the surface of the substrate, which can be achieved by attaching the 0.102 mm (4 mil) thick die to a 0.15 mm (6 mil) thick molybdenum heat spreader (moly tab). The moly tab is then attached to the ground plane (see Figure 23).

Microstrip substrates are placed as close to the HMC986A as possible to minimize bond length. Typical die to substrate spacing is 0.076 mm (3 mil).

RF bonds made with 3 mil × 5 mil ribbon are recommended. DC bonds made with 1 mil diameter wire are recommended. All bonds must be as short as possible.

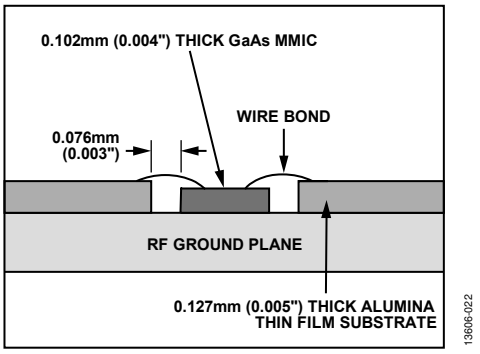

Figure 22. Bonding RF Pads to 5 mil Substrate

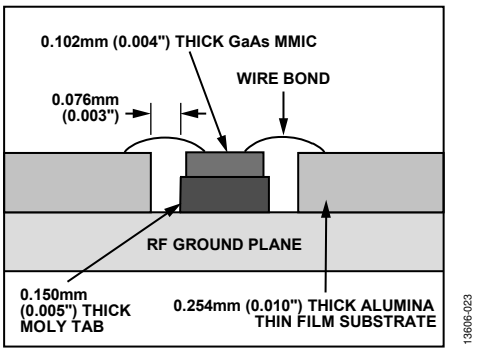

Figure 23. Bonding RF Pads to 10 mil Substrate

ASSEMBLY DIAGRAM

An assembly diagram of the HMC986A is shown in Figure 24.

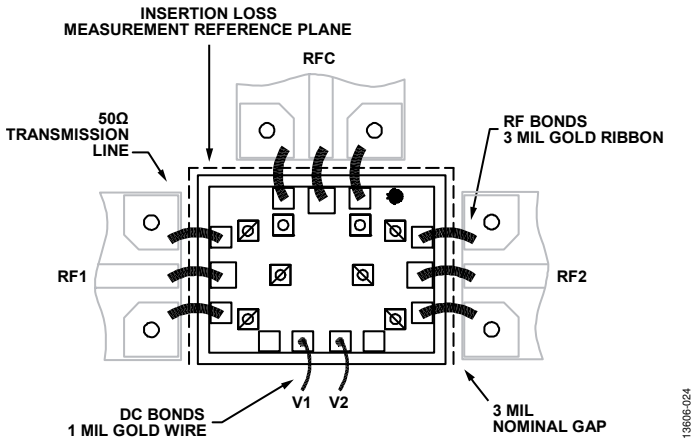

Figure 24. Die Assembly Diagram

OUTLINE DIMENSIONS

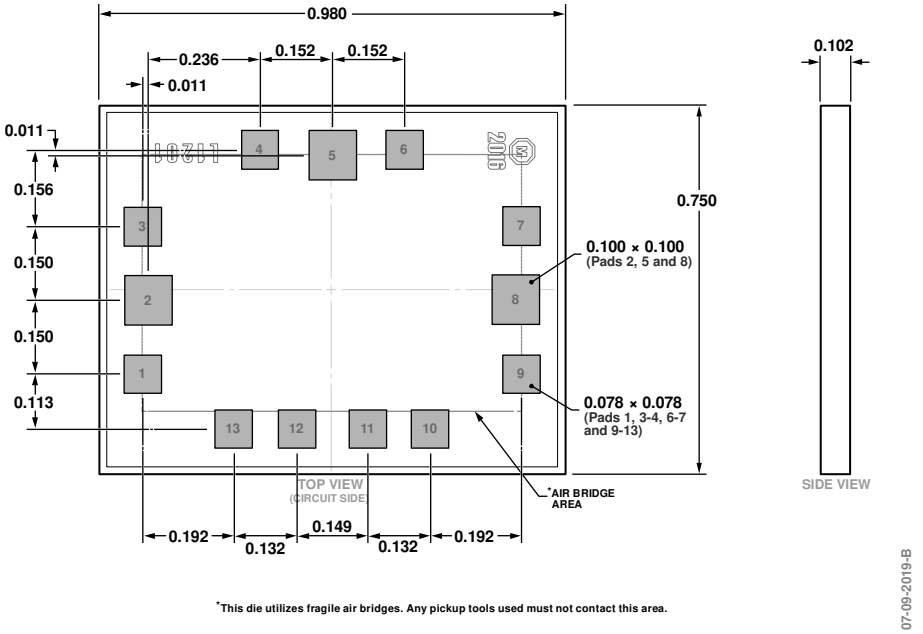

Figure 25. 13-Pad Bare Die [CHIP]
(C-13-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
HMC986A	−55°C to +85°C	13-Pad Bare Die [CHIP]	C-13-1
HMC986A-SX	−55°C to +85°C	13-Pad Bare Die [CHIP]	C-13-1

[1] The HMC986A is a RoHS-compliant part.
[2] The HMC986A-SX is a sample order model.

D13606-0-7/19(B)