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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

μPD703031A, 703031AY, 703033A, 703033AY, 70F3033A, 70F3033AY

V850/SB1™
32-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD703031A, 703031AY, 703033A, 703033AY, 70F3033A, and 70F3033AY (V850/SB1) are 32-bit single-chip microcontrollers of the V850 Series™ for AV equipment. 32-bit CPU, ROM, RAM, timer/counters, serial interfaces, A/D converter, DMA controller, and so on are integrated on a single chip.

The μPD70F3033A and 70F3033AY have flash memory in place of the internal mask ROM of the μPD703033A and 703033AY. Because flash memory allows the program to be written and erased electrically with the device mounted on the board, these products are ideal for the evaluation stages of system development, small-scale production, and rapid development of new products.

The μPD703032A, 703032AY, 70F3032A, 70F3032AY, products with a different ROM/RAM size are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850/SB1, V850/SB2™ Hardware User's Manual: U13850E
V850 Series Architecture User's Manual: U10243E

FEATURES

- Number of instructions: 74
- Minimum instruction execution time: 50 ns (@ internal 20 MHz operation)
- General-purpose registers: 32 bits × 32 registers
- Instruction set: Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space: 16 MB linear address space
- Internal memory ROM: 128 KB (μPD703031A, 703031AY: mask ROM)
  256 KB (μPD703033A, 703033AY: mask ROM)
  256 KB (μPD70F3033A, 70F3033AY: flash memory)
  RAM: 12 KB (μPD703031A, 703031AY)
  16 KB (μPD703033A, 703033AY, 70F3033A, 70F3033AY)
- Interrupt/exception: μPD703031A, 703033A, 70F3033A (external: 8, internal: 31 sources, exception: 1 source)
  μPD703031AY, 703033AY, 70F3033AY (external: 8, internal: 32 sources, exception: 1 source)
- I/O lines Total: 83
- Timer/counters: 16-bit timer (2 channels: TM0, TM1)
  8-bit timer (6 channels: TM2 to TM7)
- Watch timer: 1 channel
- Watchdog timer: 1 channel

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Printed in Japan

The mark ★ shows major revised points.

- Serial interface
  - Asynchronous serial interface (UART0, UART1)
  - Clocked serial interface (CSI0 to CSI3)
  - 3-wire variable length serial interface (CSI4)
  - I^2C bus interface (I^2C0, I^2C1) (μPD703031AY, 703033AY, 70F3033AY only)
- 10-bit resolution A/D converter: 12 channels
- DMA controller: 6 channels
- Real-time output port: 8 bits × 1 channel or 4 bits × 2 channels
- ROM correction: 4 places can be corrected
- Power-saving function: HALT/IDLE/STOP modes
- Packages: 100-pin plastic LQFP (fine pitch) (14 × 14)
  100-pin plastic QFP (14 × 20)
- μPD70F3033A, 70F3033AY
  - Can be replaced with μPD703033A and 703033AY (internal mask ROM) in mass production

APPLICATIONS

- AV equipment (audio, car audio, VCR, TV, etc.)

ORDERING INFORMATION

	Part Number	Package	Internal ROM
	μPD703031AGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (128 KB)
	μPD703031AYGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (128 KB)
	μPD703031AGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (128 KB)
	μPD703031AYGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (128 KB)
	μPD703033AGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (256 KB)
	μPD703033AYGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (256 KB)
	μPD703033AGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (256 KB)
	μPD703033AYGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (256 KB)
★	μPD70F3033AGC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Flash memory (256 KB)
★	μPD70F3033AYGC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Flash memory (256 KB)
★	μPD70F3033AGF-3BA	100-pin plastic QFP (14 × 20)	Flash memory (256 KB)
★	μPD70F3033AYGF-3BA	100-pin plastic QFP (14 × 20)	Flash memory (256 KB)

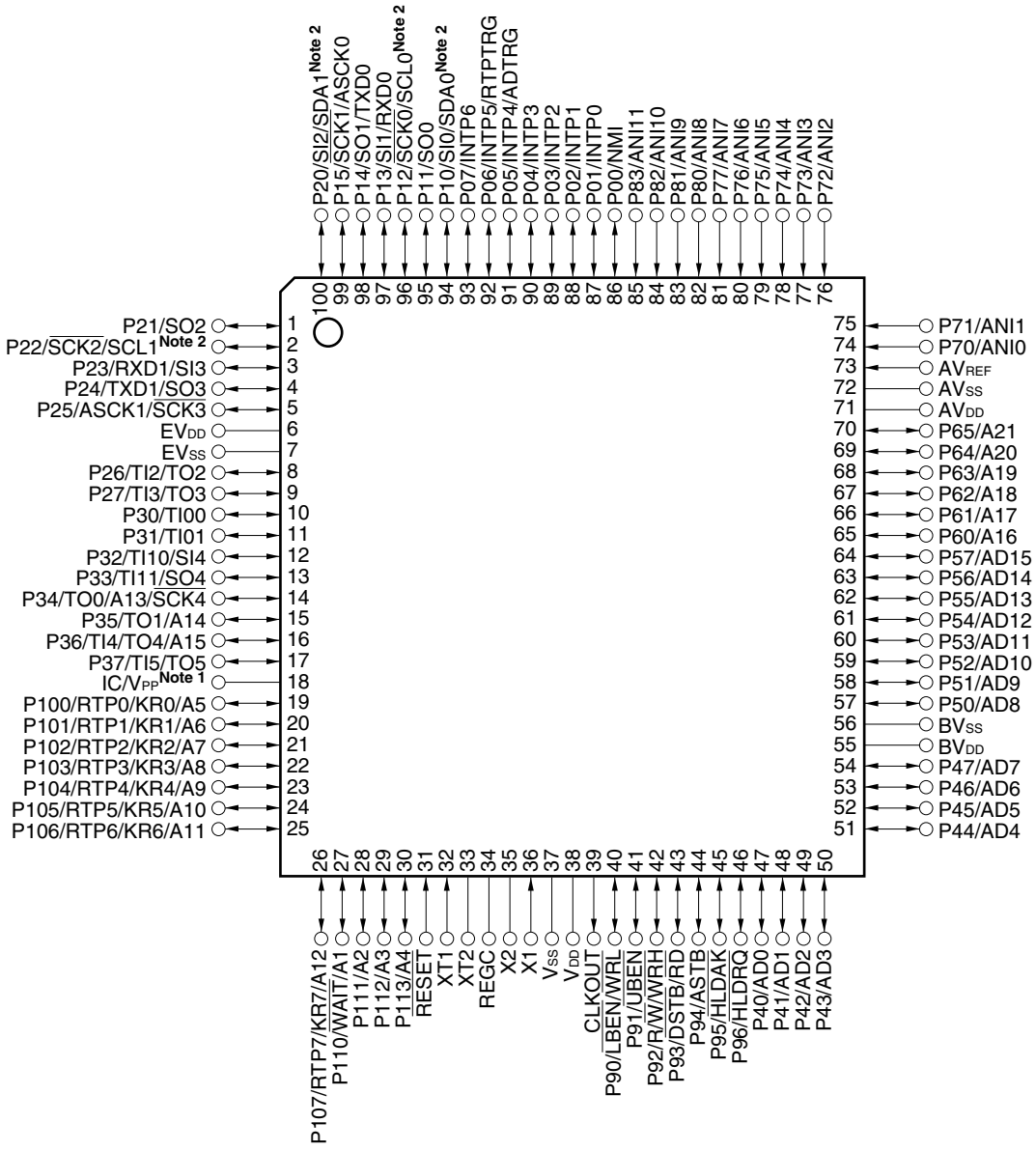
Remarks 1. ××× indicates ROM code suffix.

2. ROMless versions are not provided.

PIN CONFIGURATION (Top View)

100-pin plastic LQFP (fine pitch) (14 × 14)

- μPD703031AGC-×××-8EU
- μPD703031AYGC-×××-8EU
- μPD703033AGC-×××-8EU
- μPD703033AYGC-×××-8EU
- μPD70F3033AGC-8EU
- μPD70F3033AYGC-8EU

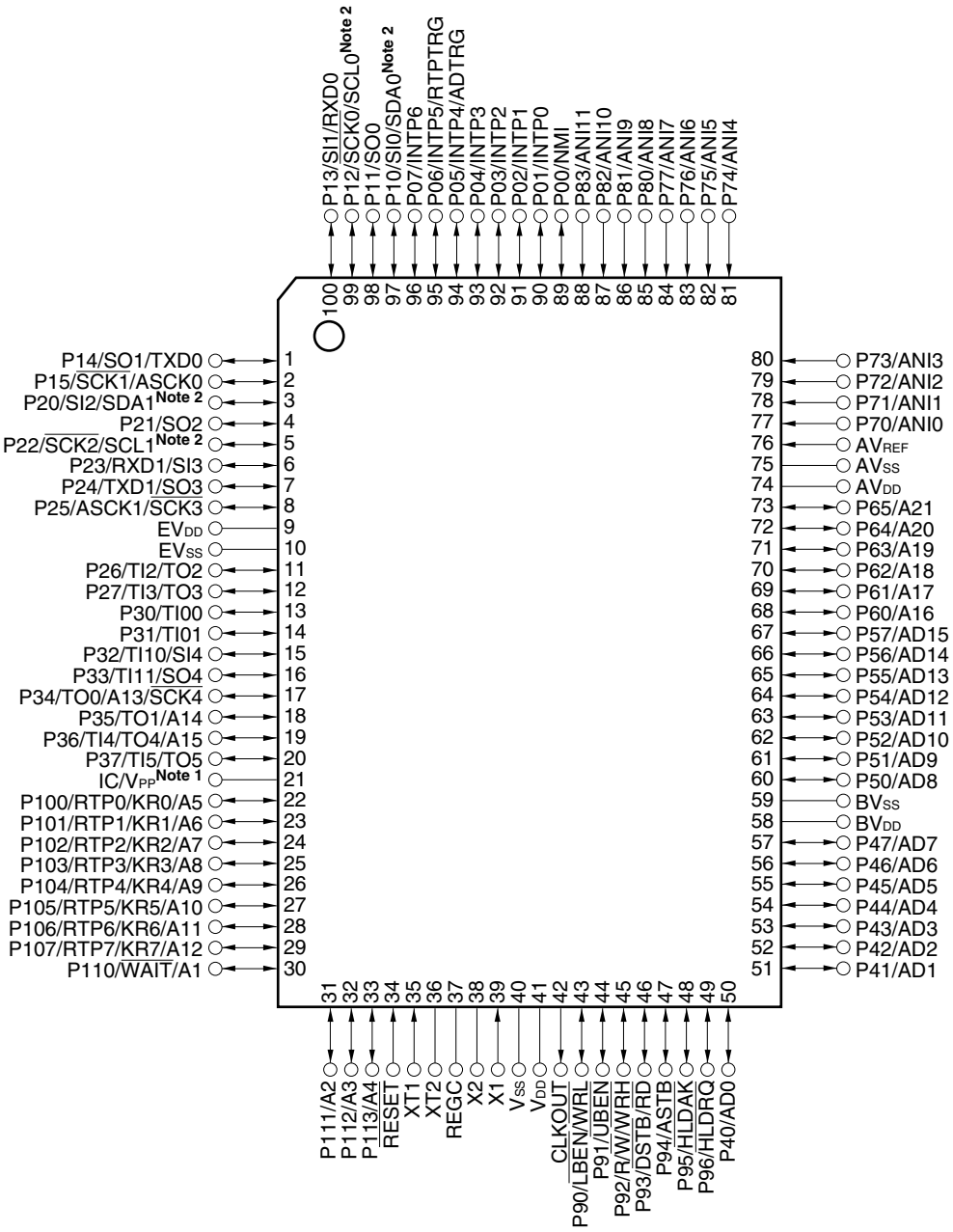


Notes 1. IC: Connect directly to VSS (μPD703031A, 703031AY, 703033A, 703033AY).
VPP: Connect to VSS in normal operation mode (μPD70F3033A, 70F3033AY).

2. SCL0, SCL1, SDA0, and SDA1 are available only in the μPD703031AY, 703033AY, and 70F3033AY.

100-pin plastic QFP (14 × 20)

- μPD703031AGF-×××-3BA
- μPD703031AYGF-×××-3BA
- μPD703033AGF-×××-3BA
- μPD703033AYGF-×××-3BA
- μPD70F3033AGF-3BA
- μPD70F3033AYGF-3BA



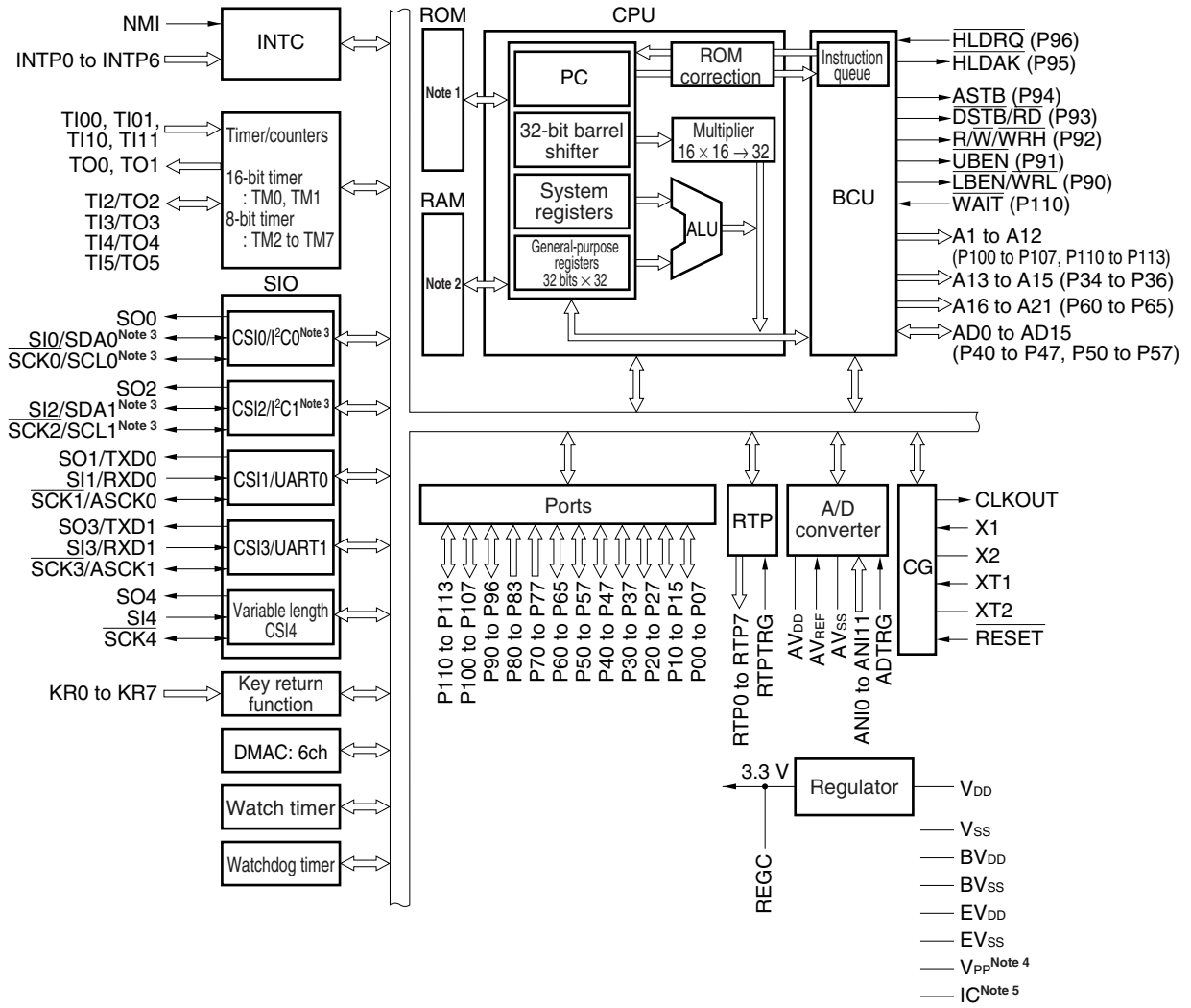
Notes 1. IC: Connect directly to VSS (μPD703031A, 703031AY, 703033A, 703033AY).
VPP: Connect to VSS in normal operation mode (μPD70F3033A, 70F3033AY).

2. SCL0, SCL1, SDA0, and SDA1 are available only in the μPD703031AY, 703033AY, and 70F3033AY.

PIN IDENTIFICATION

A1 to A21:	Address Bus	P80 to P83:	Port 8
AD0 to AD15:	Address/Data Bus	P90 to P96:	Port 9
ADTRG:	A/D Trigger Input	P100 to P107:	Port 10
ANI0 to ANI11:	Analog Input	P110 to P113:	Port 11
ASCK0, ASCK1:	Asynchronous Serial Clock	$\overline{RD}$:	Read
ASTB:	Address Strobe	REGC:	Regulator Control
AV_{DD}:	Analog Power Supply	$\overline{RESET}$:	Reset
AV_{REF}:	Analog Reference Voltage	RTP0 to RTP7:	Real-time Output Port
AV_{SS}:	Analog Ground	RTPTRG:	RTP Trigger Input
BV_{DD}:	Power Supply for Bus Interface	R/$\overline{W}$:	Read/Write Status
BV_{SS}:	Ground for Bus Interface	RXD0, RXD1:	Receive Data
CLKOUT:	Clock Output	$\overline{SCK0}$ to $\overline{SCK4}$:	Serial Clock
$\overline{DSTB}$:	Data Strobe	SCL0, SCL1:	Serial Clock
EV_{DD}:	Power Supply for Port	SDA0, SDA1:	Serial Data
EV_{SS}:	Ground for Port	SI0 to SI4:	Serial Input
$\overline{HLDAK}$:	Hold Acknowledge	SO0 to SO4:	Serial Output
$\overline{HLDRQ}$:	Hold Request	TI00, TI01, TI10, :	Timer Input
IC:	Internally Connected	TI11, TI2 to TI5	
INTP0 to INTP6:	Interrupt Request from Peripherals	TO0 to TO5:	Timer Output
KR0 to KR7:	Key Return	TXD0, TXD1:	Transmit Data
$\overline{LBEN}$:	Lower Byte Enable	$\overline{UBEN}$:	Upper Byte Enable
NMI:	Non-Maskable Interrupt Request	V_{DD}:	Power Supply
P00 to P07:	Port 0	V_{PP}:	Programming Power Supply
P10 to P15:	Port 1	V_{SS}:	Ground
P20 to P27:	Port 2	$\overline{WAIT}$:	Wait
P30 to P37:	Port 3	$\overline{WRH}$:	Write Strobe High Level Data
P40 to P47:	Port 4	$\overline{WRL}$:	Write Strobe Low Level Data
P50 to P57:	Port 5	X1, X2:	Crystal for Main Clock
P60 to P65:	Port 6	XT1, XT2:	Crystal for Sub-clock
P70 to P77:	Port 7		

INTERNAL BLOCK DIAGRAM



Notes 1. μPD703031A, 703031AY: 128 KB (mask ROM)
μPD703033A, 703033AY: 256 KB (mask ROM)
μPD70F3033A, 70F3033AY: 256 KB (flash memory)

2. μPD703031A, 703031AY: 12 KB
μPD703033A, 703033AY, 70F3033A, 70F3033AY: 16 KB

3. I^2C bus interface and SDAn and SCLn pins (n = 0, 1) are available only in the μPD703031AY, 703033AY, and 70F3033AY.

4. μPD70F3033A, 70F3033AY

5. μPD703031A, 703031AY, 703033A, 703033AY

CONTENTS

1. DIFFERENCES AMONG PRODUCTS

Part Number	On-Chip I^2C	ROM		RAM Size	Flash Memory Programming Pin	Package
		Type	Size			
μPD703031A	No	Mask ROM	128 KB	12 KB	No	100-pin QFP (14 × 20) 100-pin LQFP (14 × 14)
μPD703031AY	Yes					
μPD703033A	No	Mask ROM	256 KB	16 KB	No	100-pin QFP (14 × 20) 100-pin LQFP (14 × 14)
μPD703033AY	Yes					
μPD70F3033A	No	Flash memory			Yes (V_{PP})	
μPD70F3033AY	Yes					
μPD703032A	No	Mask ROM	512 KB	24 KB	No	100-pin QFP (14 × 20)
μPD703032AY	Yes					
μPD70F3032A	No	Flash memory			Yes (V_{PP})	
μPD70F3032AY	Yes					

Cautions 1. There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. When replacing the flash memory versions with mask ROM versions, write the same code in the empty area of the internal ROM.

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	Yes	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P05				INTP4/ADTRG
P06				INTP5/RTPTRG
P07				INTP6
P10	I/O	Yes	Port 1 6-bit I/O port Input/output can be specified in 1-bit units.	SI0/SDA0 Note
P11				SO0
P12				$\overline{\text{SCK0}}$/SCL0 Note
P13				SI1/RXD0
P14				SO1/TXD0
P15				$\overline{\text{SCK1}}$/ASCK0
P20	I/O	Yes	Port 2 8-bit I/O port Input/output can be specified in 1-bit units.	SI2/SDA1 Note
P21				SO2
P22				$\overline{\text{SCK2}}$/SCL1 Note
P23				SI3/RXD1
P24				SO3/TXD1
P25				$\overline{\text{SCK3}}$/ASCK1
P26				TI2/TO2
P27				TI3/TO3
P30	I/O	Yes	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	TI00
P31				TI01
P32				TI10/SI4
P33				TI11/SO4
P34				TO0/A13/$\overline{\text{SCK4}}$
P35				TO1/A14
P36				TI4/TO4/A15
P37				TI5/TO5
P40 to P47	I/O	No	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	AD0 to AD7
P50 to P57	I/O	No	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	AD8 to AD15

Note μPD703031AY, 703033AY, 70F3033AY only.

Remark PULL: On-chip pull-up resistor

(2/2)

Pin Name	I/O	PULL	Function	Alternate Function
P60 to P65	I/O	No	Port 6 6-bit I/O port Input/output can be specified in 1-bit units.	A16 to A21
P70 to P77	Input	No	Port 7 8-bit input port	ANI0 to ANI7
P80 to P83	Input	No	Port 8 4-bit input port	ANI8 to ANI11
P90	I/O	No	Port 9 7-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}/\overline{\text{WRL}}$
P91				$\overline{\text{UBEN}}$
P92				R/$\overline{\text{W}}$/$\overline{\text{WRH}}$
P93				$\overline{\text{DSTB}}/\overline{\text{RD}}$
P94				ASTB
P95				$\overline{\text{HLDAK}}$
P96				$\overline{\text{HLDRQ}}$
P100	I/O	Yes	Port 10 8-bit I/O port Input/output can be specified in 1-bit units.	RTP0/A5/KR0
P101				RTP1/A6/KR1
P102				RTP2/A7/KR2
P103				RTP3/A8/KR3
P104				RTP4/A9/KR4
P105				RTP5/A10/KR5
P106				RTP6/A11/KR6
P107				RTP7/A12/KR7
P110	I/O	Yes	Port 11 4-bit I/O port Input/output can be specified in 1-bit units.	A1/$\overline{\text{WAIT}}$
P111				A2
P112				A3
P113				A4

Remark PULL: On-chip pull-up resistor

2.2 Non-Port Pins

(1/4)

Pin Name	I/O	PULL	Function	Alternate Function
A1	Output	Yes	Lower address bus used for external memory expansion	P110/$\overline{\text{WAIT}}$
A2				P111
A3				P112
A4				P113
A5				P100/RTP0/KR0
A6				P101/RTP1/KR1
A7				P102/RTP2/KR2
A8				P103/RTP3/KR3
A9				P104/RTP4/KR4
A10				P105/RTP5/KR5
A11				P106/RTP6/KR6
A12				P107/RTP7/KR7
A13				P34/TO0/$\overline{\text{SCK4}}$
A14				P35/TO1
A15				P36/TO4/TI4
A16 to A21	Output	No	Higher address bus used for external memory expansion	P60 to P65
AD0 to AD7	I/O	No	16-bit multiplexed address/data bus used for external memory expansion	P40 to P47
AD8 to AD15				P50 to P57
ADTRG	Input	Yes	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI11				P80 to P83
ASCK0	Input	Yes	Baud rate clock input for UART0	P15/$\overline{\text{SCK1}}$
ASCK1			Baud rate clock input for UART1	P25/$\overline{\text{SCK3}}$
ASTB	Output	No	External address strobe output	P94
AV_{DD}	–	–	Positive power supply for A/D converter and alternate port	–
AV_{REF}	Input	–	Reference voltage input for A/D converter	–
AV_{SS}	–	–	Ground potential for A/D converter and alternate port	–
BV_{DD}	–	–	Positive power supply for bus interface and alternate port	–
BV_{SS}	–	–	Ground potential for bus interface and alternate port	–
CLKOUT	Output	–	Internal system clock output	–
$\overline{\text{DSTB}}$	Output	No	External data strobe output	P93/$\overline{\text{RD}}$
EV_{DD}	–	–	Positive power supply for I/O ports and alternate-function pins (except bus interface alternate port)	–
EV_{SS}	–	–	Ground potential for I/O ports and alternate-function pins (except bus interface alternate port)	–
$\overline{\text{HLDAK}}$	Output	No	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	No	Bus hold request input	P96
IC	–	–	Internally connected (μPD703031A, 703031AY, 703033A, 703033AY only)	–

Remark PULL: On-chip pull-up resistor

(2/4)

Pin Name	I/O	PULL	Function	Alternate Function
INTP0	Input	Yes	External interrupt request input (analog noise elimination)	P01
INTP1				P02
INTP2				P03
INTP3				P04
INTP4	Input	Yes	External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5				P06/RTPTRG
INTP6	Input	Yes	External interrupt request input (digital noise elimination supporting remote controller)	P07
KR0	Input	Yes	Key return input	P100/RTP0/A5
KR1				P101/RTP1/A6
KR2				P102/RTP2/A7
KR3				P103/RTP3/A8
KR4				P104/RTP4/A9
KR5				P105/RTP5/A10
KR6				P106/RTP6/A11
KR7				P107/RTP7/A12
$\overline{\text{LBEN}}$	Output	No	External data bus's lower byte enable output	P90/$\overline{\text{WRL}}$
NMI	Input	Yes	Non-maskable interrupt request input	P00
$\overline{\text{RD}}$	Output	No	Read strobe output	P93/$\overline{\text{DSTB}}$
REGC	–	–	Regulator output stabilization capacitance connection	–
$\overline{\text{RESET}}$	Input	–	System reset input	–
RTP0	Output	Yes	Real-time output port	P100/KR0/A5
RTP1				P101/KR1/A6
RTP2				P102/KR2/A7
RTP3				P103/KR3/A8
RTP4				P104/KR4/A9
RTP5				P105/KR5/A10
RTP6				P106/KR6/A11
RTP7				P107/KR7/A12
RTPTRG	Input	Yes	Real-time output port external trigger input	P06/INTP5
R/$\overline{\text{W}}$	Output	No	External read/write status output	P92/$\overline{\text{WRH}}$
RXD0	Input	Yes	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P23/SI3

Remark PULL: On-chip pull-up resistor

(3/4)

Pin Name	I/O	PULL	Function	Alternate Function
$\overline{SCK0}$	I/O	Yes	Serial clock I/O (3-wire type) for CSI0 to CSI3	P12/SCL0[Note]
$\overline{SCK1}$				P15/ASCK0
$\overline{SCK2}$				P22/SCL1[Note]
$\overline{SCK3}$				P25/ASCK1
$\overline{SCK4}$	I/O	Yes	Serial clock I/O (3-wire type) for variable length CSI4	P34/TO0/A13
SCL0	I/O	Yes	Serial clock I/O for I^2C0 and I^2C1 (μPD703031AY, 703033AY, 70F3033AY only)	P12/$\overline{SCK0}$
SCL1				P22/$\overline{SCK2}$
SDA0	I/O	Yes	Serial transmit/receive data I/O for I^2C0 and I^2C1 (μPD703031AY, 703033AY, 70F3033AY only)	P10/SI0
SDA1				P20/SI2
SI0	Input	Yes	Serial receive data input (3-wire type) for CSI0 to CSI3	P10/SDA0[Note]
SI1				P13/RXD0
SI2				P20/SDA1[Note]
SI3				P23/RXD1
SI4	Input	Yes	Serial receive data input (3-wire type) for variable length CSI4	P32/TI10
SO0	Output	Yes	Serial transmit data output (3-wire type) for CSI0 to CSI3	P11
SO1				P14/TXD0
SO2				P21
SO3				P24/TXD1
SO4	Output	Yes	Serial transmit data output (3-wire type) for variable length CSI4	P33/TI11
TI00	Input	Yes	External count clock input for TM0/external capture trigger input for TM0	P30
TI01			External capture trigger input for TM0	P31
TI10			External count clock input for TM1/external capture trigger input for TM1	P32/SI4
TI11			External capture trigger input for TM1	P33/SO4
TI2	Input	Yes	External count clock input for TM2 to TM5	P26/TO2
TI3				P27/TO3
TI4				P36/TO4/A15
TI5				P37/TO5
TO0	Output	Yes	Pulse signal output for TM0 and TM1	P34/A13/$\overline{SCK4}$
TO1				P35/A14
TO2	Output	Yes	Pulse signal output for TM2 to TM5	P26/TI2
TO3				P27/TI3
TO4				P36/TI4/A15
TO5				P37/TI5
TXD0	Output	Yes	Serial transmit data output for UART0 and UART1	P14/SO1
TXD1				P24/SO3
$\overline{UBEN}$	Output	No	Higher byte enable output for external data bus	P91
V_{DD}	–	–	Positive power supply pin	–

Note μPD703031AY, 703033AY, and 70F3033AY only

Remark PULL: On-chip pull-up resistor

(4/4)

Pin Name	I/O	PULL	Function	Alternate Function
V_{PP}	–	–	High voltage apply pin for program write/verify (μPD70F3033A, 70F3033AY only)	–
V_{SS}	–	–	Ground potential	–
$\overline{WAIT}$	Input	Yes	Control signal input for inserting wait in bus cycle	P110/A1
$\overline{WRH}$	Output	No	Higher byte write strobe signal output for external data bus	P92/R/$\overline{W}$
$\overline{WRL}$	Output	No	Lower byte write strobe signal output for external data bus	P90/$\overline{LBEN}$
X1	Input	No	Resonator connection for main clock	–
X2	–			–
XT1	Input	No	Resonator connection for subsystem clock	–
XT2	–			–

Remark PULL: On-chip pull-up resistor

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are show in Table 2-1. For the I/O schematic circuit diagram of each type, refer to Figure 2-1.

Table 2-1. Types of Pin I/O Circuits (1/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection of Unused Pins
P00	NMI	8-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P01	INTP0			
P02	INTP1			
P03	INTP2			
P04	INTP3			
P05	INTP4/ADTRG			
P06	INTP5/RTPTRG			
P07	INTP6			
P10	SI0/SDA0	10-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P11	SO0	26		
P12	$\overline{SCK0}$/SCL0	10-A		
P13	SI1/RXD0	8-A		
P14	SO1/TXD0	26		
P15	$\overline{SCK1}$/ASCK0	10-A		
P20	SI2/SDA1	10-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P21	SO2	26		
P22	$\overline{SCK2}$/SCL1	10-A		
★ P23	SI3/RXD1	8-A		
P24	SO3/TXD1	26		
P25	$\overline{SCK3}$/ASCK1	10-A		
P26	TI2/TO2	8-A		
P27	TI3/TO3			
P30	TI00	8-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P31	TI01			
P32	TI10/SI4			
P33	TI11/SO4			
P34	TO0/A13/$\overline{SCK4}$			
P35	TO1/A14	5-A		
P36	TI4/TO4/A15	8-A		
P37	TI5/TO5			
P40 to P47	AD0 to AD7	5	BV_{DD}	Input state: Independently connect to BV_{DD} or BV_{SS} via a resistor. Output state: Leave open.
P50 to P57	AD8 to AD15	5	BV_{DD}	
P60 to P65	A16 to A21	5	BV_{DD}	

Table 2-1. Types of Pin I/O Circuits (2/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection of Unused Pins
P70 to P77	ANI0 to ANI7	9	AV_{DD}	Independently connect to AV_{DD} or AV_{SS} via a resistor.
P80 to P83	ANI8 to ANI11	9	AV_{DD}	
P90	$\overline{LBEN}/\overline{WRL}$	5	BV_{DD}	Input state: Independently connect to BV_{DD} or BV_{SS} via a resistor. Output state: Leave open.
P91	$\overline{UBEN}$			
P92	$R/\overline{W}/\overline{WRH}$			
P93	$\overline{DSTB}/\overline{RD}$			
P94	ASTB			
★ P95	$\overline{HLDAK}$			
★ P96	$\overline{HLDRQ}$			
P100	RTP0/A5/KR0	10-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P101	RTP1/A6/KR1			
P102	RTP2/A7/KR2			
P103	RTP3/A8/KR3			
P104	RTP4/A9/KR4			
P105	RTP5/A10/KR5			
P106	RTP6/A11/KR6			
P107	RTP7/A12/KR7			
P110	A1/$\overline{WAIT}$	5-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P111	A2			
P112	A3			
P113	A4			
CLKOUT	–	4	BV_{DD}	Leave open.
$\overline{RESET}$	–	2	EV_{DD}	–
XT1	–	16	–	Connect to V_{SS} via a resistor.
XT2	–	16	–	Leave open.
AV_{REF}	–	–	–	Connect to AV_{SS} via a resistor.
IC[Note 1]	–	–	–	Connect directly to V_{SS}.
V_{PP}[Note 2]	–	–	–	Connect to V_{SS}.

Notes 1. μPD703031A, 703031AY, 703033A, 703033AY

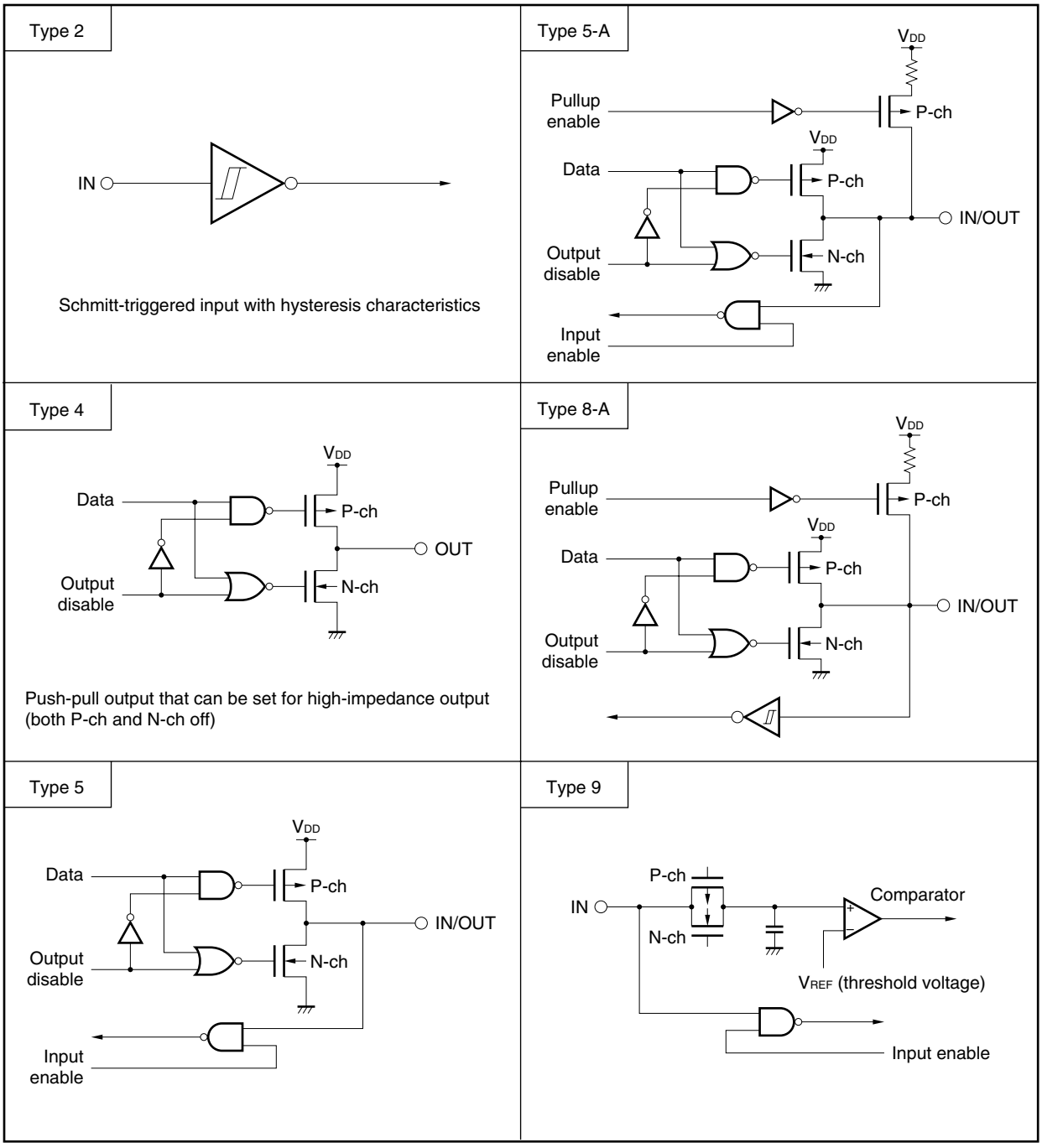
2. μPD70F3033A, 70F3033AY

Caution Three power supply systems are available to supply power to the I/O buffers of the V850/SB1's pins: EV_{DD}, BV_{DD}, and AV_{DD}. The voltage ranges that can be used for these I/O buffer power supplies are shown below.

EV_{DD}, BV_{DD}: 3.0 V to 5.5 V
AV_{DD}: 4.5 V to 5.5 V

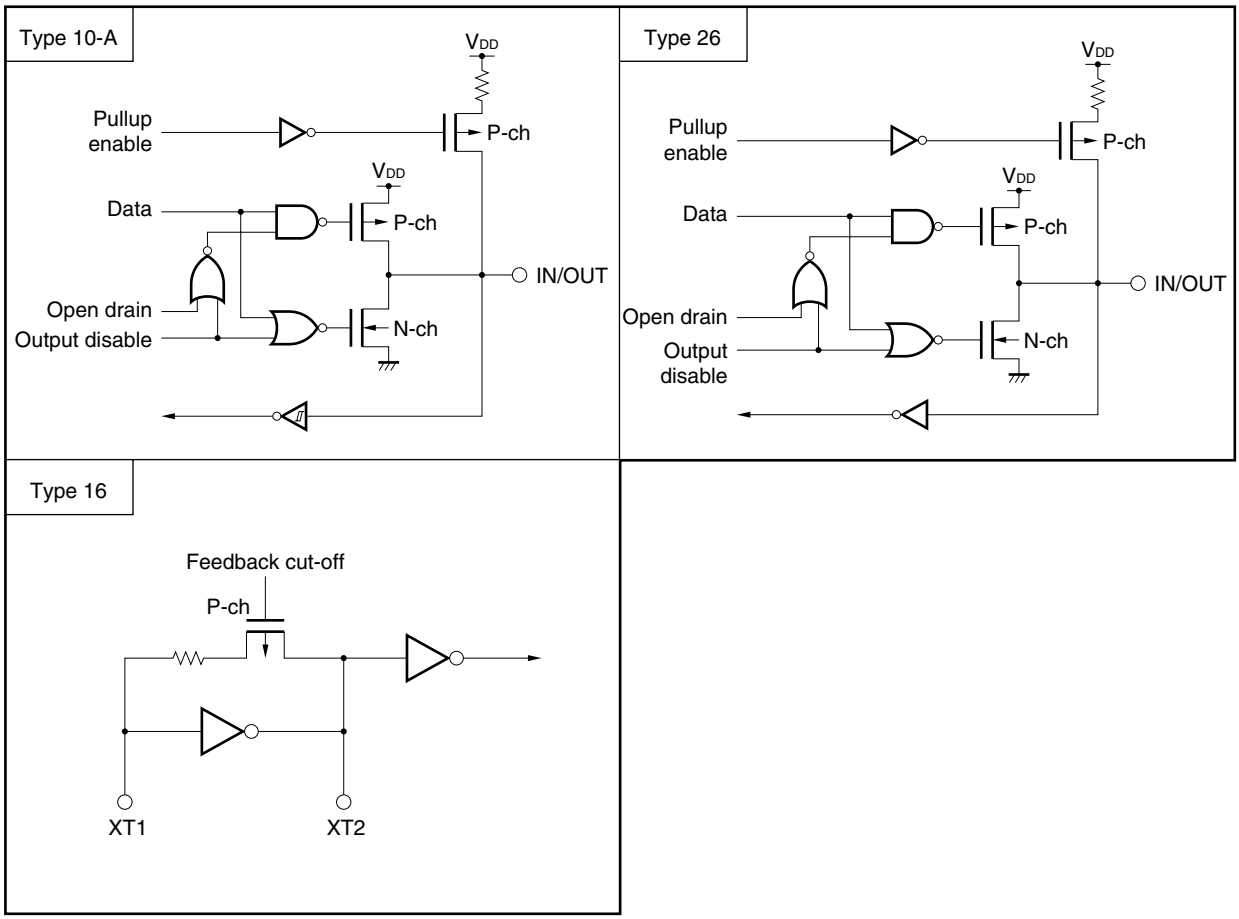
The electrical specifications differ depending on whether the power supply voltage range is 3.0 V to under 4.0 V, or 4.0 V to 5.5 V.

Figure 2-1. Pin I/O Circuits (1/2)



Caution V_{DD} in the circuit diagrams can be read as EV_{DD}, BV_{DD}, or AV_{DD}, as appropriate.

Figure 2-1. Pin I/O Circuits (2/2)



Caution V_{DD} in the circuit diagrams can be read as EV_{DD}, BV_{DD}, or AV_{DD}, as appropriate.

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	–0.5 to +7.0	V
★	V_{PP}	V_{PP} pin (μPD70F3033A, 70F3033AY only)	–0.5 to +8.5	V
	AV_{DD}	AV_{DD} pin	–0.5 to +7.0	V
	BV_{DD}	BV_{DD} pin	–0.5 to +7.0	V
	EV_{DD}	EV_{DD} pin	–0.5 to +7.0	V
	AV_{SS}	AV_{SS} pin	–0.5 to +0.5	V
	BV_{SS}	BV_{SS} pin	–0.5 to +0.5	V
	EV_{SS}	EV_{SS} pin	–0.5 to +0.5	V
★ Input voltage	V_{I1}	**Note 1** (BV_{DD} pin)	–0.5 to BV_{DD} + 0.5[Note 4]	V
	V_{I2}	**Note 2**, $\overline{\text{RESET}}$ (EV_{DD} pin)	–0.5 to EV_{DD} + 0.5[Note 4]	V
Analog input voltage	V_{IAN}	**Note 3** (AV_{DD} pin)	–0.5 to AV_{DD} + 0.5[Note 4]	V
Analog reference input voltage	AV_{REF}	AV_{REF} pin	–0.5 to AV_{DD} + 0.5[Note 4]	V
Output current, low	I_{OL}	Per pin	4.0	mA
		Total for P00 to P07, P10 to P15, P20 to P25	25	mA
		Total for P26, P27, P30 to P37, P100 to P107, P110 to P113	25	mA
		Total for P40 to P47, P90 to P96, CLKOUT	25	mA
		Total for P50 to P57, P60 to P65	25	mA
Output current, high	I_{OH}	Per pin	–4.0	mA
		Total for P00 to P07, P10 to P15, P20 to P25	–25	mA
		Total for P26, P27, P30 to P37, P100 to P107, P110 to P113	–25	mA
		Total for P40 to P47, P90 to P96, CLKOUT	–25	mA
		Total for P50 to P57, P60 to P65	–25	mA
Output voltage	V_{O1}	**Note 1**, CLKOUT (BV_{DD} pin)	–0.5 to BV_{DD} + 0.5[Note 4]	V
★	V_{O2}	**Note 2** (EV_{DD} pin)	–0.5 to EV_{DD} + 0.5[Note 4]	V
Operating ambient temperature	T_A	Normal operation mode	–40 to +85	°C
★		Flash memory programming mode (μPD70F3033A, 70F3033AY only)	**Note 5**	°C
Storage temperature	T_{stg}	μPD703031A, 703031AY, 703033A, 703033AY	–65 to +150	°C
		μPD70F3033A, 70F3033AY	–40 to +125	°C

Notes 1. Ports 4, 5, 6, 9, and their alternate-function pins

2. Ports 0, 1, 2, 3, 10, 11, and their alternate-function pins

3. Ports 7, 8, and their alternate-function pins

4. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

★ **5.** K rank product: T_A = 10 to 85°C

E rank product: T_A = –20 to +85°C

The rank is indicated by the letter appearing as the 5th digit from the left in the lot number.

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance (T_A = 25°C, V_{DD} = AV_{DD} = BV_{DD} = EV_{DD} = V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions

★ (1) Operating frequency

Operating Frequency (f_{XX})		V_{DD}	AV_{DD}		BV_{DD}	EV_{DD}	Remark
			Note 1	**Note 2**			
2 to 20 MHz		4.0 to 5.5 V	4.5 to 5.5 V	4.0 to 5.5 V	4.0 to 5.5 V	4.0 to 5.5 V	**Note 3**
2 to 17 MHz		4.0 to 5.5 V	4.5 to 5.5 V	4.0 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	
32.768 kHz	Other than IDLE mode	4.0 to 5.5 V	4.5 to 5.5 V	4.0 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	–
	IDLE mode	3.5 to 5.5 V	–	4.0 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	**Note 4**

Notes 1. When A/D converter is used

2. When A/D converter is not used

3. During STOP mode (when only watch timer is operating), V_{DD} = 3.5 to 5.5 V. Shifting to STOP mode or restoring from STOP mode must be performed at V_{DD} = 4.0 V min.

4. Shifting to IDLE mode or restoring from IDLE mode must be performed at V_{DD} = 4.0 V min.

(2) CPU operating frequency

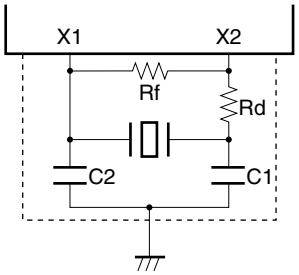
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU operating frequency	f_{CPU}	Main clock operation	0.25		20	MHz
		Subclock operation		32.768		kHz

Recommended Oscillator

(1) Main clock oscillator (T_A = –40 to +85°C)

(a) Connection of ceramic resonator or crystal resonator

★



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XX}		2		20	MHz
Oscillation stabilization time	–	Upon reset release		$2^{19}/f_{XX}$		s
	–	Upon STOP mode release		**Note**		s

Note The TYP. value differs depending on the setting of the oscillation stabilization time select register (OSTS).

Cautions 1. The main clock oscillator operates on the output voltage of the on-chip regulator (3.3 V). External clock input is prohibited.

2. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

3. Ensure that the duty of oscillation waveform is between 5.5 and 4.5.

4. Sufficiently evaluate the matching between the μPD703031A, 703031AY, 703033A, 703033AY, 70F3033A, 70F3033AY and the resonator.

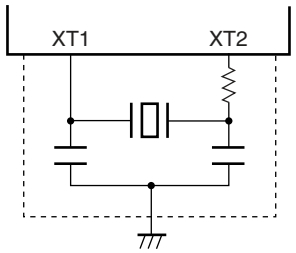
★ (i) Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant				Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	Rf (kΩ)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSTLS8M00G56-B0	8.00	On-chip	On-chip	–	0	4.0	5.5
	CSTCC8M00G56-R0		On-chip	On-chip	–	0	4.0	5.5
	CSTLA12M5T55-B0	12.5	On-chip	On-chip	–	0	4.0	5.5
	CSTCV12M5T54J-R0		On-chip	On-chip	–	0	4.0	5.5
	CSALS16M0X55-B0	16.00	10	10	–	0	4.0	5.5
	CSTCV16M0X51J-R0		On-chip	On-chip	–	0	4.0	5.5
	CSTLS20M0X51-B0	20.00	On-chip	On-chip	–	0	4.0	5.5
	CSTCW20M0X51-R0		On-chip	On-chip	22k	0	4.0	5.5

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

(2) Subclock oscillator (T_A = –40 to +85°C)

(a) Connection of crystal resonator



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XT}		32	32.768	35	kHz
Oscillation stabilization time	–			10		s

Cautions 1. The subclock oscillator operates on the output voltage of the on-chip regulator (3.3 V). External clock input is prohibited.

2. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

3. Sufficiently evaluate the matching between the μPD703031A, 703031AY, 703033A, 703033AY, 70F3033A, 70F3033AY and the resonator.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, AV_{DD} = 4.5 to 5.5 V (when A/D converter is used), AV_{DD} = 4.0 to 5.5 V (when A/D converter is not used), V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V) (1/2)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★	Input voltage, high	V_{IH1}	**Note 1**	4.0 V ≤ BV_{DD} ≤ 5.5 V	0.7BV_{DD}		BV_{DD}	V
				3.0 V ≤ BV_{DD} < 4.0 V	0.8BV_{DD}		BV_{DD}	V
		V_{IH2}	**Note 2**	4.0 V ≤ EV_{DD} ≤ 5.5 V	0.7EV_{DD}		EV_{DD}	V
				3.0 V ≤ EV_{DD} < 4.0 V	0.8EV_{DD}		EV_{DD}	V
		V_{IH3}	**Note 3**, $\overline{\text{RESET}}$	4.0 V ≤ EV_{DD} ≤ 5.5 V	0.7EV_{DD}		EV_{DD}	V
				3.0 V ≤ EV_{DD} < 4.0 V	0.8EV_{DD}		EV_{DD}	V
		V_{IH4}	**Note 4**		0.7AV_{DD}		AV_{DD}	V
★	Input voltage, low	V_{IL1}	**Note 1**		BV_{SS}		0.3BV_{DD}	V
		V_{IL2}	**Note 2**		EV_{SS}		0.3EV_{DD}	V
		V_{IL3}	**Note 3**, $\overline{\text{RESET}}$		EV_{SS}		0.3EV_{DD}	V
		V_{IL4}	**Note 4**		AV_{SS}		0.3AV_{DD}	V
	Output voltage, high	V_{OH1}	**Note 1**, CLKOUT	3.0 V ≤ BV_{DD} ≤ 5.5 V, I_{OH} = –100 μA	BV_{DD}–0.5			V
				4.0 V ≤ BV_{DD} ≤ 5.5 V, I_{OH} = –3 mA	BV_{DD}–1.0			V
		V_{OH2}	**Notes 2, 3**	3.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = –100 μA	EV_{DD}–0.5			V
				4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = –3 mA	EV_{DD}–1.0			V
	Output voltage, low	V_{OL}	I_{OL} = 3 mA, 3.0 V ≤ BV_{DD}, EV_{DD} ≤ 5.5 V				0.5	V
			I_{OL} = 3 mA, 4.0 V ≤ BV_{DD}, EV_{DD} ≤ 5.5 V				0.4	V
★	V_{PP} power supply voltage	V_{PP1}	Normal operation		0		0.6	V
	Input leakage current, high	I_{LIH}	V_I = V_{DD} = BV_{DD} = EV_{DD} = AV_{DD}				5	μA
	Input leakage current, low	I_{LIL}	V_I = 0 V				–5	μA
★	Output leakage current, high	I_{LOH}	V_O = V_{DD} = BV_{DD} = EV_{DD} = AV_{DD}				5	μA
★	Output leakage current, low	I_{LOL}	V_O = 0 V				–5	μA

Notes 1. Ports 4, 5, 6, 9, and their alternate-function pins

2. P11, P14, P21, P24, P34, P35, P110 to P113, and their alternate-function pins

3. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, P100 to P107, and their alternate-function pins

4. Ports 7, 8, and their alternate-function pins

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, AV_{DD} = 4.5 to 5.5 V (when A/D converter is used), AV_{DD} = 4.0 to 5.5 V (when A/D converter is not used), V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V) (2/2)

Parameter		Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	μPD703031A, μPD703031AY, μPD703033A, μPD703033AY	I_{DD1}	In normal operation mode[Note 1]			25	40	mA
		I_{DD2}	In HALT mode[Note 1]			10	20	mA
		I_{DD3}	In IDLE mode[Note 2]	Watch timer operating		1	4	mA
		I_{DD4}	In STOP mode	Watch timer, subclock oscillator operating		13	70	μA
				Subclock oscillator stopped, XT1 = V_{SS}		8	70	μA
		I_{DD5}	In normal operation mode (subclock operation)[Note 3]			50	150	μA
		I_{DD6}	In IDLE mode (subclock operation)[Note 3]			13	70	μA
	μPD70F3033A, μPD70F3033AY	I_{DD1}	In normal operation mode[Note 1]			33	60	mA
		I_{DD2}	In HALT mode[Note 1]			10	20	mA
		I_{DD3}	In IDLE mode[Note 2]	Watch timer operating		1	4	mA
		I_{DD4}	In STOP mode	Watch timer, subclock oscillator operating		13	100	μA
				Subclock oscillator stopped, XT1 = V_{SS}		8	100	μA
		I_{DD5}	In normal operation mode (subclock operation)[Note 3]			200	600	μA
		I_{DD6}	In IDLE mode (subclock operation)[Note 3]			90	180	μA
Pull-up resistance		R_L	V_{IN} = 0 V		10	30	100	kΩ

Notes 1. f_{CPU} = f_{XX} = 20 MHz, all peripheral functions operating

2. f_{XX} = 20 MHz

3. f_{CPU} = f_{XT} = 32.768 kHz, main clock oscillator stopped

Remark TYP. values are reference values for when T_A = 25°C, V_{DD} = BV_{DD} = EV_{DD} = AV_{DD} = 5.0 V. The current consumed by the output buffer is not included.

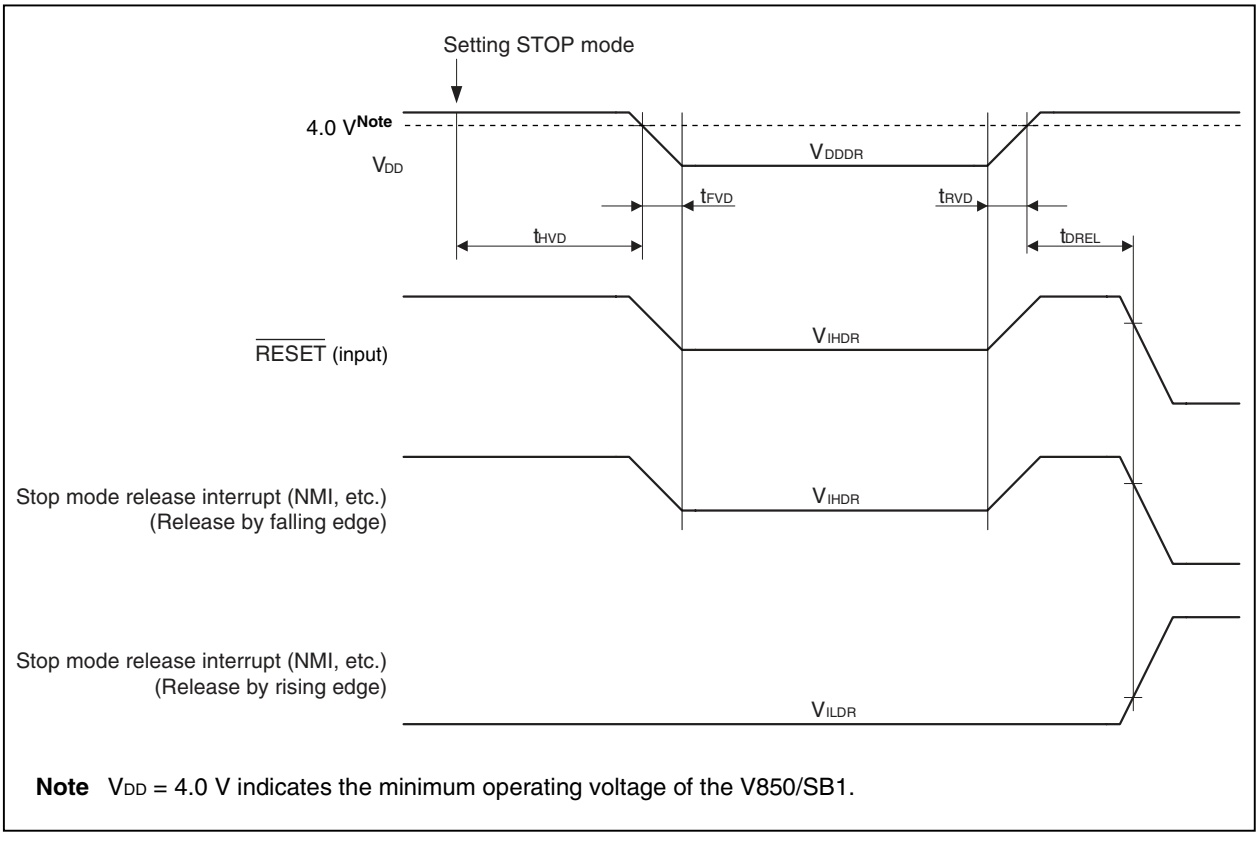
Data Retention Characteristics (T_A = –40 to +85°C, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★ Data retention voltage	V_{DDDR}	STOP mode (all functions not operating)		2.7[Note]		5.5	V
Data retention current	I_{DDDR}	V_{DD} = V_{DDDR}, XT1 = V_{SS} (Subclock stopped)	μPD703031A, μPD703031AY, μPD703033A, μPD703033AY		8	70	μA
			μPD70F3033A, μPD70F3033AY		8	100	μA
Power supply voltage rise time	t_{RVD}			200			μs
Power supply voltage fall time	t_{FVD}			200			μs
Power supply voltage hold time (from STOP mode setting)	t_{HVD}			0			ms
STOP mode release signal input time	t_{DREL}			0			ms
Data retention high-level input voltage	V_{IHDR}	All input ports		0.9V_{DDDR}		V_{DDDR}	V
Data retention low-level input voltage	V_{ILDR}	All input ports		0		0.1V_{DDDR}	V

Note During STOP mode (when only watch timer is operating), V_{DD} = 3.5 to 5.5 V. Shifting to STOP mode or restoring from STOP mode must be performed at V_{DD} = 4.0 V min.

Remark TYP. values are reference values for when T_A = 25°C.

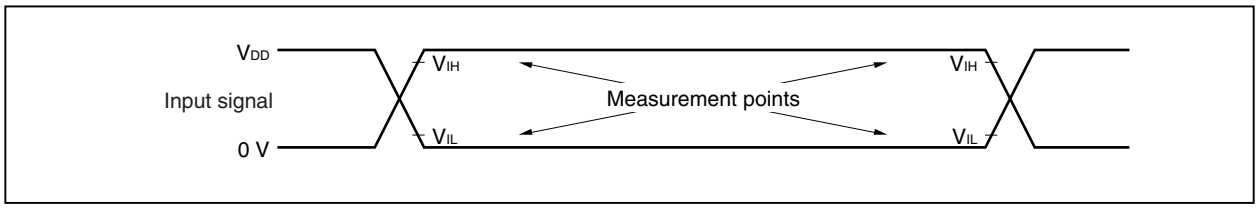
★



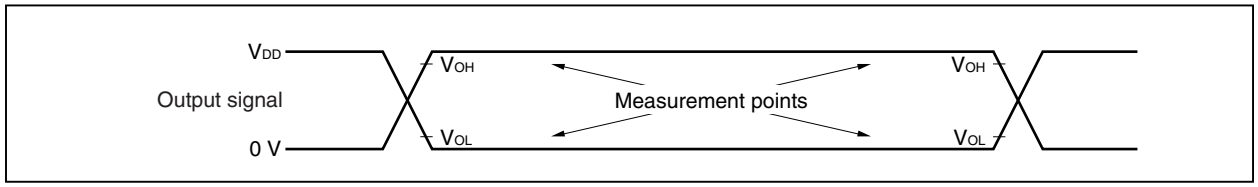
★ **Note** V_{DD} = 4.0 V indicates the minimum operating voltage of the V850/SB1.

AC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V,
AV_{DD} = 4.5 to 5.5 V (when A/D converter is used),
AV_{DD} = 4.0 to 5.5 V (when A/D converter is not used), V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

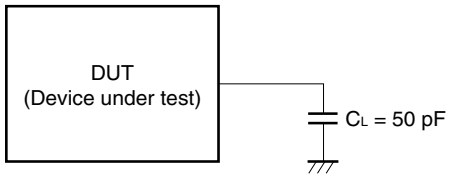
AC Test Input Measurement Point (V_{DD}: EV_{DD}, BV_{DD}, AV_{DD})



AC Test Output Measurement Points (V_{DD}: EV_{DD}, BV_{DD})



Load Conditions



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

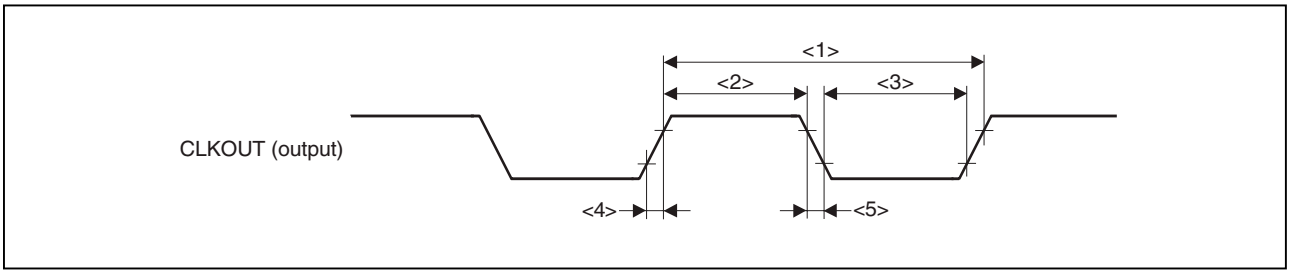
(1) Clock timing

(a) T_A = –40 to +85°C, V_{DD} = BV_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKOUT output cycle	<1>	t_{CYK}		50 ns	31.2 μs	
CLKOUT high-level width	<2>	t_{WKH}		$0.4t_{CYK}$ – 12		ns
CLKOUT low-level width	<3>	t_{WKL}		$0.4t_{CYK}$ – 12		ns
CLKOUT rise time	<4>	t_{KR}			12	ns
CLKOUT fall time	<5>	t_{KF}			12	ns

(b) T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = 3.0 to 4.0 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V

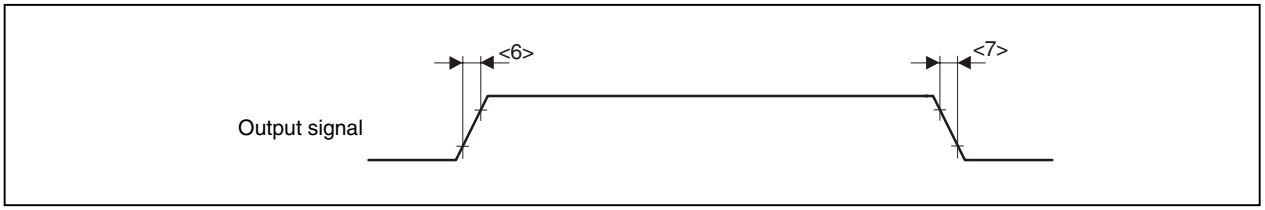
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKOUT output cycle	<1>	t_{CYK}		58.8 ns	31.2 μs	
CLKOUT high-level width	<2>	t_{WKH}		$0.4t_{CYK}$ – 15		ns
CLKOUT low-level width	<3>	t_{WKL}		$0.4t_{CYK}$ – 15		ns
CLKOUT rise time	<4>	t_{KR}			15	ns
CLKOUT fall time	<5>	t_{KF}			15	ns



(2) Output waveform (other than port 4, port 5, port 6, port 9, and CLKOUT)

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = BV_{SS} = EV_{SS} = 0 V)

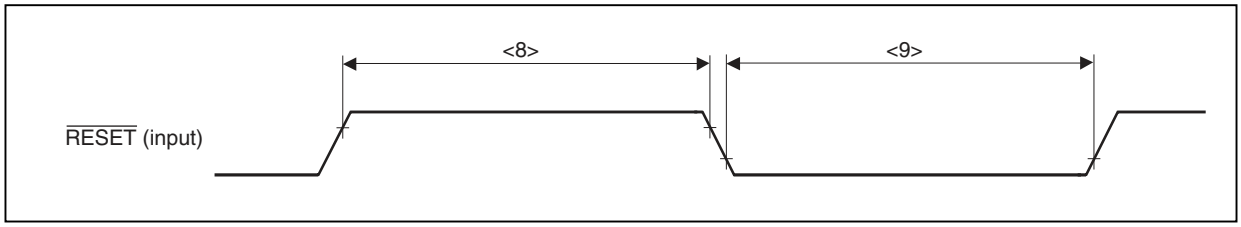
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	<6>	t_{OR}			20	ns
Output fall time	<7>	t_{OF}			20	ns



(3) Reset timing

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ pin high-level width	<8>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ pin low-level width	<9>	t_{WRSL}		500		ns



(4) Bus timing

(a) Clock asynchronous (T_A = –40 to +85°C, V_{DD} = BV_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	<10>	t_{SAST}		0.5T – 16		ns
Address hold time (from ASTB↓)	<11>	t_{HSTA}		0.5T – 15		ns
Address float delay time from $\overline{DSTB}$↓	<12>	t_{FDA}			0	ns
Data input setup time from address	<13>	t_{SAID}			(2 + n)T – 40	ns
Data input setup time from $\overline{DSTB}$↓	<14>	t_{SDID}			(1 + n)T – 40	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	<15>	t_{DSTD}		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	<16>	t_{HDID}		0		ns
Address output time from $\overline{DSTB}$↑	<17>	t_{DDA}		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	<18>	t_{DDST1}		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	<19>	t_{DDST2}		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	<20>	t_{WDL}		(1 + n)T – 22		ns
ASTB high-level width	<21>	t_{WSTH}		T – 15		ns
Data output time from $\overline{DSTB}$↓	<22>	t_{DDOD}			10	ns
Data output setup time (to $\overline{DSTB}$↑)	<23>	t_{SODD}		(1 + n)T – 25		ns
Data output hold time (from $\overline{DSTB}$↑)	<24>	t_{HDOD}		T – 20		ns
$\overline{WAIT}$ setup time (to address)	<25>	t_{SAWT1}	n ≥ 1		1.5T – 40	ns
	<26>	t_{SAWT2}	n ≥ 1		(1.5 + n)T – 40	ns
$\overline{WAIT}$ hold time (from address)	<27>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<28>	t_{HAWT2}	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<29>	t_{SSTWT1}	n ≥ 1		T – 32	ns
	<30>	t_{SSTWT2}	n ≥ 1		(1 + n)T – 32	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<31>	t_{HSTWT1}	n ≥ 1	nT		ns
	<32>	t_{HSTWT2}	n ≥ 1	(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	<33>	t_{WHQH}		T + 10		ns
$\overline{HLDAK}$ low-level width	<34>	t_{WHAL}		T – 15		ns
Bus output delay time from $\overline{HLDAK}$↑	<35>	t_{DHAC}		–6		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	<36>	t_{DHQHA1}			(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	<37>	t_{DHQHA2}		0.5T	1.5T + 25	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

★ **3.** i: Number of idle states inserted after a read cycle (0 or 1).

4. The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

(b) Clock asynchronous (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = 3.0 to 4.0 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	<10>	t_{SAST}		0.5T – 20		ns
Address hold time (from ASTB↓)	<11>	t_{HSTA}		0.5T – 20		ns
Address float delay time from $\overline{DSTB}$↓	<12>	t_{FDA}			0	ns
Data input setup time from address	<13>	t_{SAID}			(2 + n)T – 50	ns
Data input setup time from $\overline{DSTB}$↓	<14>	t_{SDID}			(1 + n)T – 50	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	<15>	t_{DSTD}		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	<16>	t_{HDID}		0		ns
Address output time from $\overline{DSTB}$↑	<17>	t_{DDA}		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	<18>	t_{DDST1}		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	<19>	t_{DDST2}		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	<20>	t_{WDL}		(1 + n)T – 35		ns
ASTB high-level width	<21>	t_{WSTH}		T – 15		ns
Data output time from $\overline{DSTB}$↓	<22>	t_{DDOD}			10	ns
Data output setup time (to $\overline{DSTB}$↑)	<23>	t_{SODD}		(1 + n)T – 35		ns
Data output hold time (from $\overline{DSTB}$↑)	<24>	t_{HDOD}		T – 25		ns
$\overline{WAIT}$ setup time (to address)	<25>	t_{SAWT1}	n ≥ 1		1.5T – 55	ns
	<26>	t_{SAWT2}	n ≥ 1		(1.5 + n)T – 55	ns
$\overline{WAIT}$ hold time (from address)	<27>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<28>	t_{HAWT2}	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<29>	t_{SSTWT1}	n ≥ 1		T – 45	ns
	<30>	t_{SSTWT2}	n ≥ 1		(1 + n)T – 45	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<31>	t_{HSTWT1}	n ≥ 1	nT		ns
	<32>	t_{HSTWT2}	n ≥ 1	(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	<33>	t_{WHQH}		T + 10		ns
$\overline{HLDAK}$ low-level width	<34>	t_{WHAL}		T – 25		ns
Bus output delay time from $\overline{HLDAK}$↑	<35>	t_{DHAC}		–6		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	<36>	t_{DHQHA1}			(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	<37>	t_{DHQHA2}		0.5T	1.5T + 25	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

★ **3.** i: Number of idle states inserted after a read cycle (0 or 1).

4. The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

(c) Clock synchronous (T_A = –40 to +85°C, V_{DD} = BV_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<38>	t_{DKA}		0	19	ns
Delay time from CLKOUT↑ to address float	<39>	t_{FKA}		–12	10	ns
Delay time from CLKOUT↓ to ASTB	<40>	t_{DKST}		0	19	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	<41>	t_{DKD}		0	19	ns
Data input setup time (to CLKOUT↑)	<42>	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	<43>	t_{HKID}		5		ns
Data output delay time from CLKOUT↑	<44>	t_{DKOD}			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<45>	t_{SWTK}		20		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<46>	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<47>	t_{SHQK}		20		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<48>	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to address float (during bus hold)	<49>	t_{DKF}			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	<50>	t_{DKHA}			19	ns

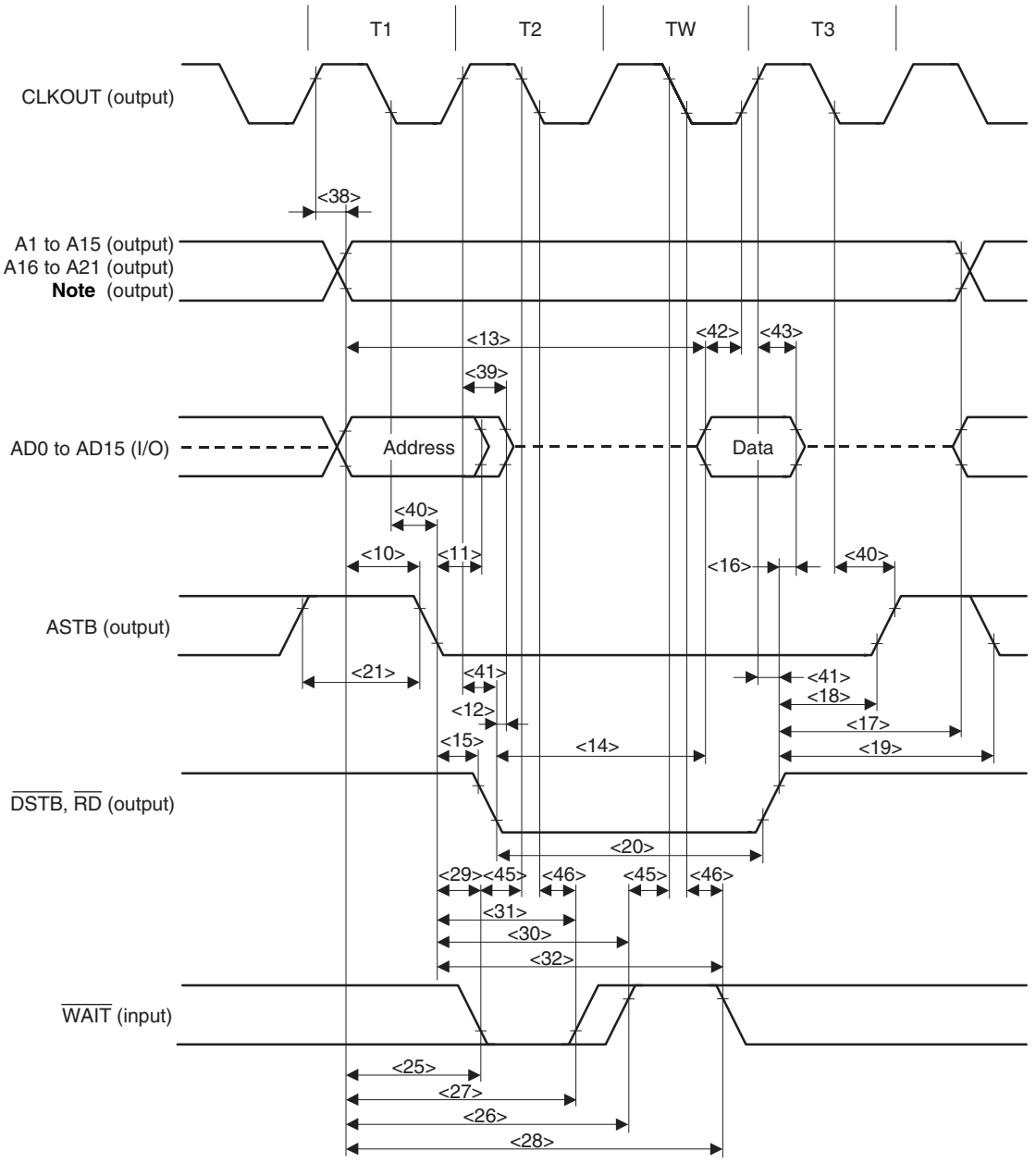
Remark The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

(d) Clock synchronous (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = 3.0 to 4.0 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<38>	t_{DKA}		0	22	ns
Delay time from CLKOUT↑ to address float	<39>	t_{FKA}		–16	10	ns
Delay time from CLKOUT↓ to ASTB	<40>	t_{DKST}		0	19	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	<41>	t_{DKD}		0	22	ns
Data input setup time (to CLKOUT↑)	<42>	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	<43>	t_{HKID}		5		ns
Data output delay time from CLKOUT↑	<44>	t_{DKOD}			22	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<45>	t_{SWTK}		24		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<46>	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<47>	t_{SHQK}		24		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<48>	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to address float (during bus hold)	<49>	t_{DKF}			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	<50>	t_{DKHA}			19	ns

Remark The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

(e) Read cycle (CLKOUT synchronous/asynchronous, 1 wait)

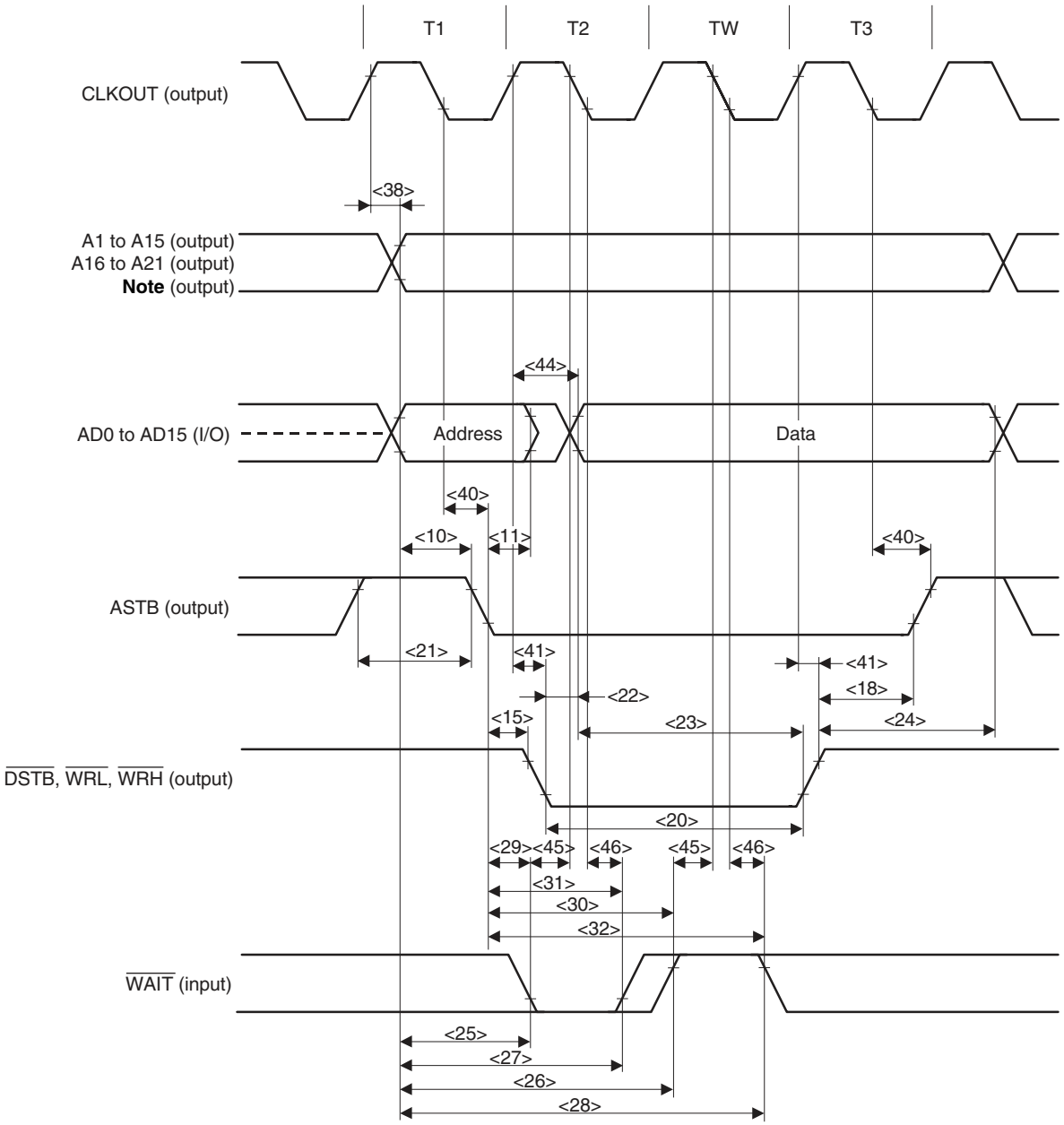


Note R/W, UBEN, LBEN

Remarks 1. The broken lines indicate high impedance.

★ **2.** WRL and WRH are high level.

(f) Write cycle (CLKOUT synchronous/asynchronous, 1 wait)

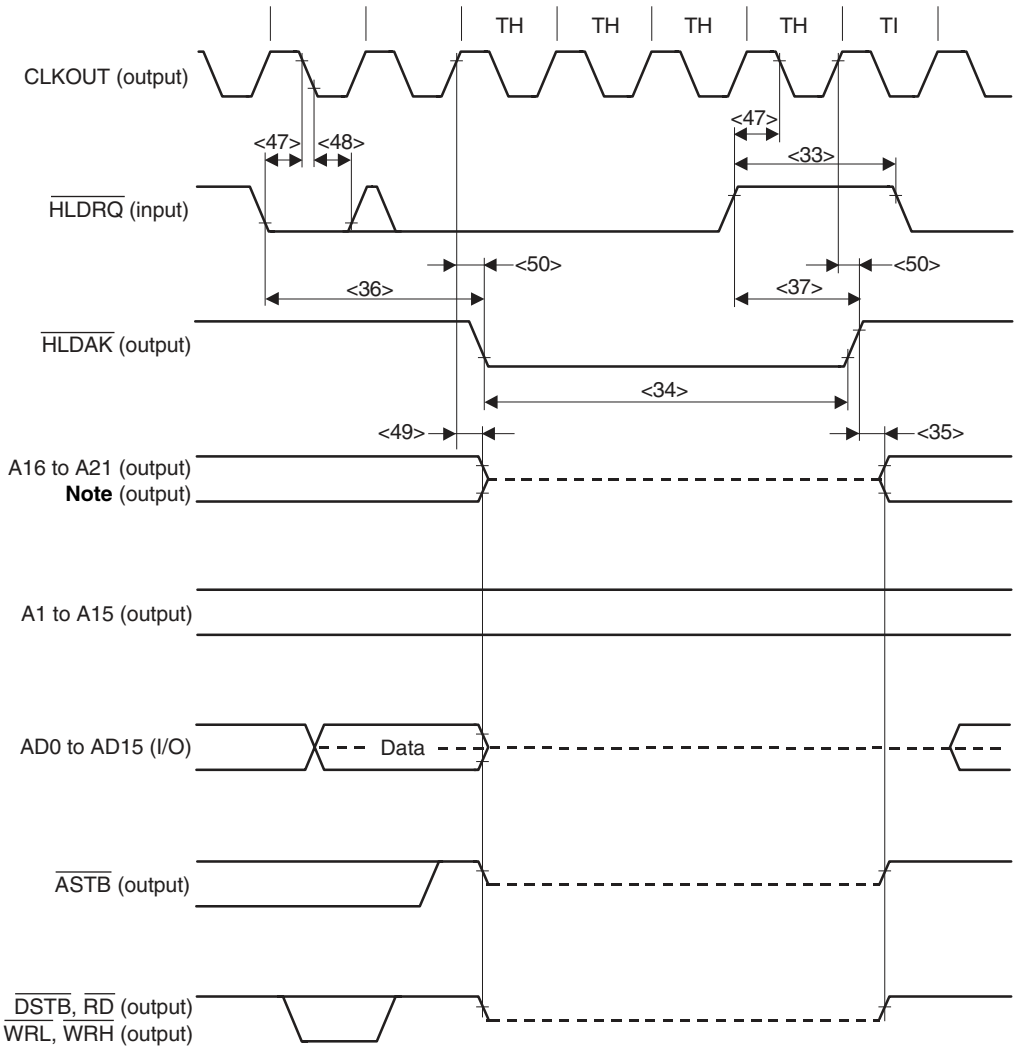


Note R/$\overline{W}$, $\overline{UBEN}$, $\overline{LBEN}$

Remarks 1. The broken lines indicate high impedance.

★ **2.** $\overline{RD}$ is high level.

(g) Bus hold timing



Note R/$\overline{W}$, $\overline{UBEN}$, $\overline{LBEN}$

Remark The broken lines indicate high impedance.

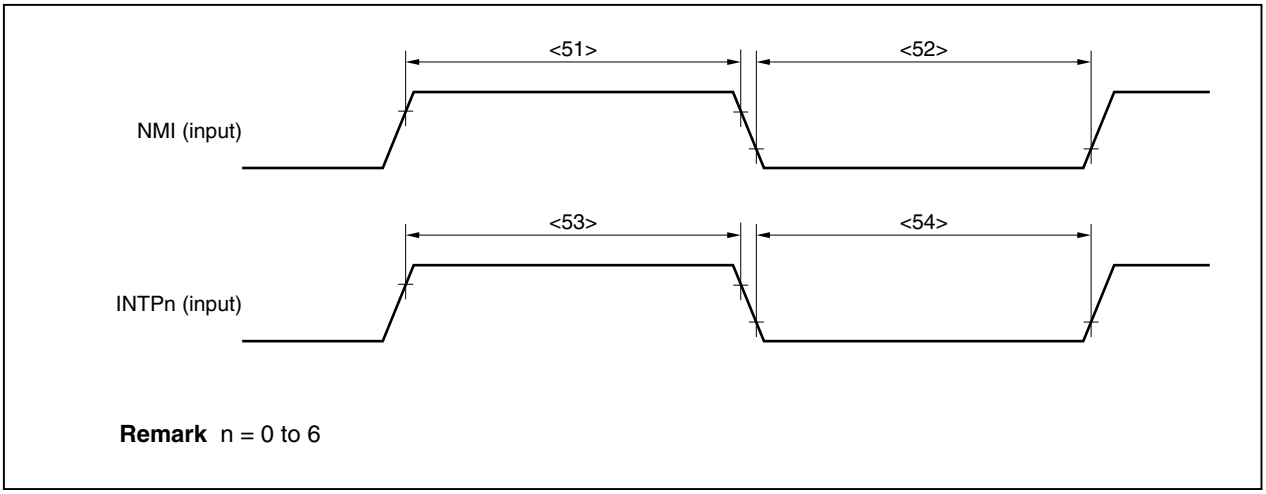
(5) Interrupt timing

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<51>	t_{WNIH}		500		ns
NMI low-level width	<52>	t_{WNIL}		500		ns
INTPn high-level width	<53>	t_{WITH}	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns
INTPn low-level width	<54>	t_{WITL}	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns

Remarks 1. T = 1/f_{XX}

2. Tsmp = Noise elimination sampling clock cycle



Remark n = 0 to 6

(6) RPU timing

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TIn0, TIn1 high-level width	<55>	t_{TIHn}	n = 0, 1	$2T_{sam}$ + 20[Note]		ns
TIn0, TIn1 low-level width	<56>	t_{TILn}	n = 0, 1	$2T_{sam}$ + 20[Note]		ns
TIm high-level width	<57>	t_{TIHm}	m = 2 to 5	3T + 20		ns
TIm low-level width	<58>	t_{TILm}	m = 2 to 5	3T + 20		ns

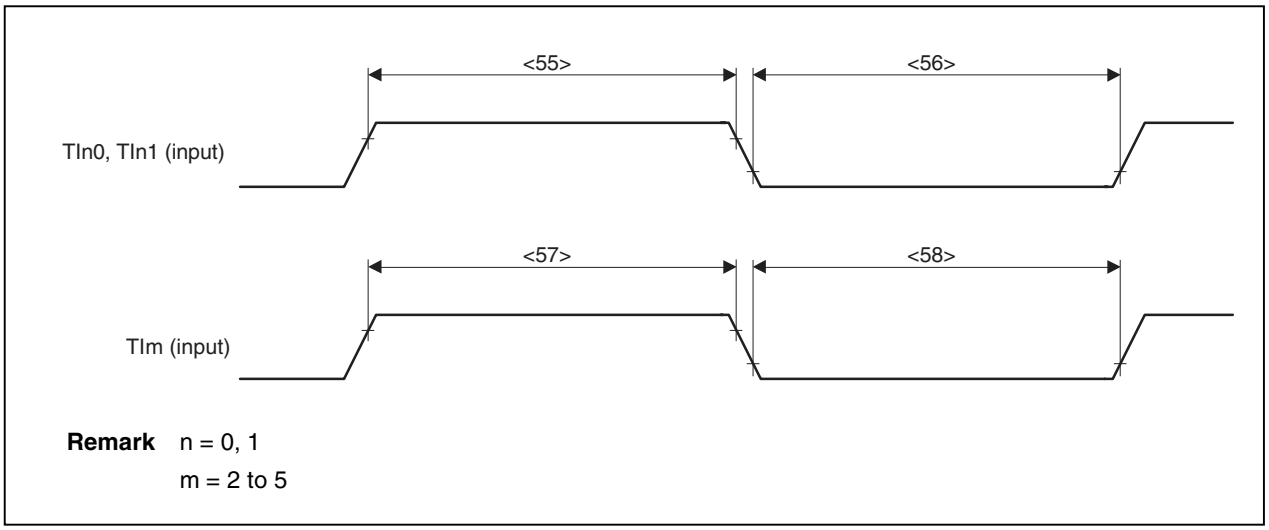
Note T_{sam} can select the following count clocks by setting the PRMn2 to PRMn0 bits of prescaler mode registers n0, n1 (PRMn0, PRMn1).

When n = 0 (TM0), T_{sam} = 2T, 4T, 16T, 64T, 256T, or 1/INTWTNI cycle

When n = 1 (TM1), T_{sam} = 2T, 4T, 16T, 32T, 128T, or 256T

However, when the TIn0 valid edge is selected as the count clock, T_{sam} = 4T.

Remark T = 1/fxx



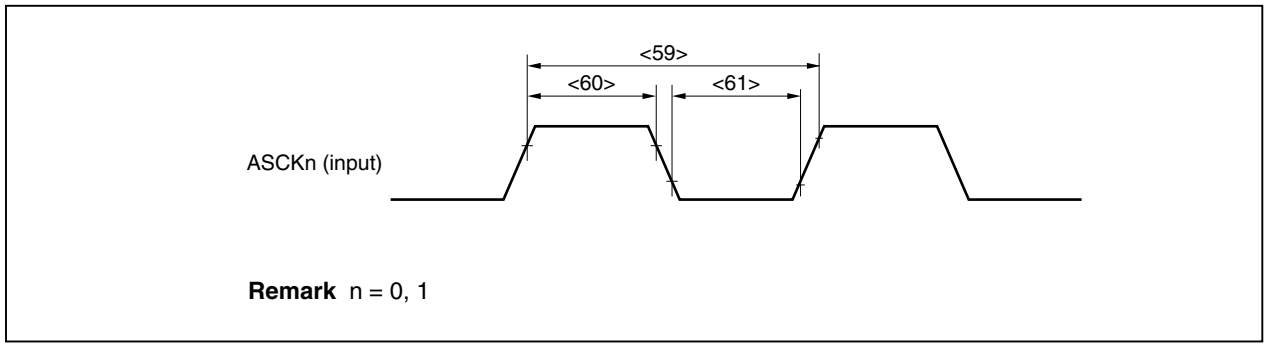
Remark n = 0, 1
m = 2 to 5

(7) Asynchronous serial interface (UART0, UART1) timing

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
ASCKn cycle time	<59>	t_{KCY13}		200		ns
ASCKn high-level width	<60>	t_{KH13}		80		ns
ASCKn low-level width	<61>	t_{KL13}		80		ns

Remark n = 0, 1



Remark n = 0, 1

(8) 3-wire serial interface (CSI0 to CSI3) timing

(a) Master mode

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<62>	t_{KCY1}		400		ns
$\overline{SCKn}$ high-level width	<63>	t_{KH1}		140		ns
$\overline{SCKn}$ low-level width	<64>	t_{KL1}		140		ns
SIn setup time (to $\overline{SCKn}\uparrow$)	<65>	t_{SIK1}		50		ns
SIn hold time (from $\overline{SCKn}\uparrow$)	<66>	t_{KSI1}		50		ns
Delay time from $\overline{SCKn}\downarrow$ to SOn output	<67>	t_{KSO1}			60	ns

Remark n = 0 to 3

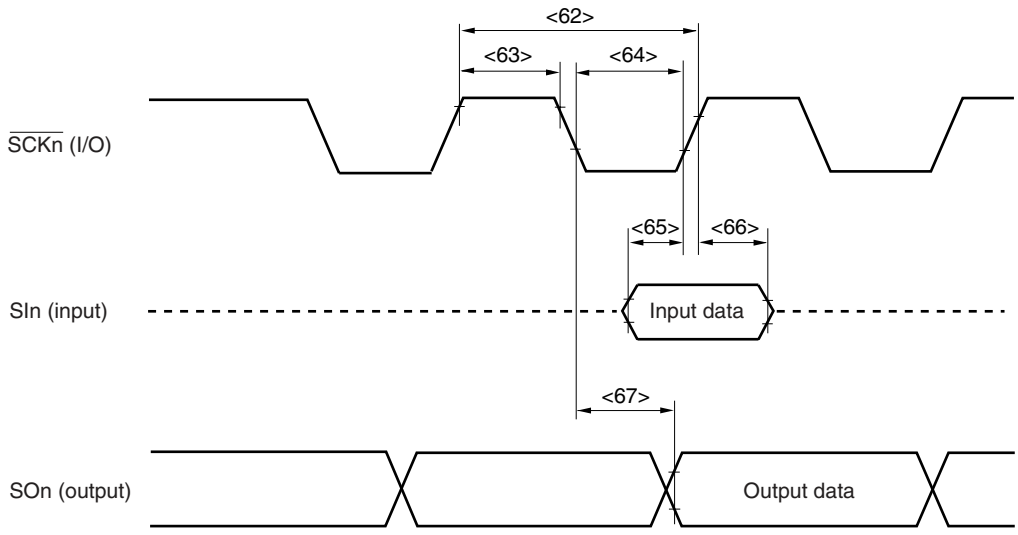
(b) Slave mode

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = V_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<62>	t_{KCY2}		400		ns
$\overline{SCKn}$ high-level width	<63>	t_{KH2}		140		ns
$\overline{SCKn}$ low-level width	<64>	t_{KL2}		140		ns
SIn setup time (to $\overline{SCKn}\uparrow$)	<65>	t_{SIK2}		50		ns
SIn hold time (from $\overline{SCKn}\uparrow$)	<66>	t_{KSI2}		50		ns
Delay time from $\overline{SCKn}\downarrow$ to SOn output	<67>	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		60	ns
			3.0 V ≤ EV_{DD} < 4.0 V		100	ns

Remark n = 0 to 3

★



Remarks 1. The broken lines indicate high impedance.

2. n = 0 to 3

(9) 3-wire variable length serial interface (CSI4) timing

(a) Master mode

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

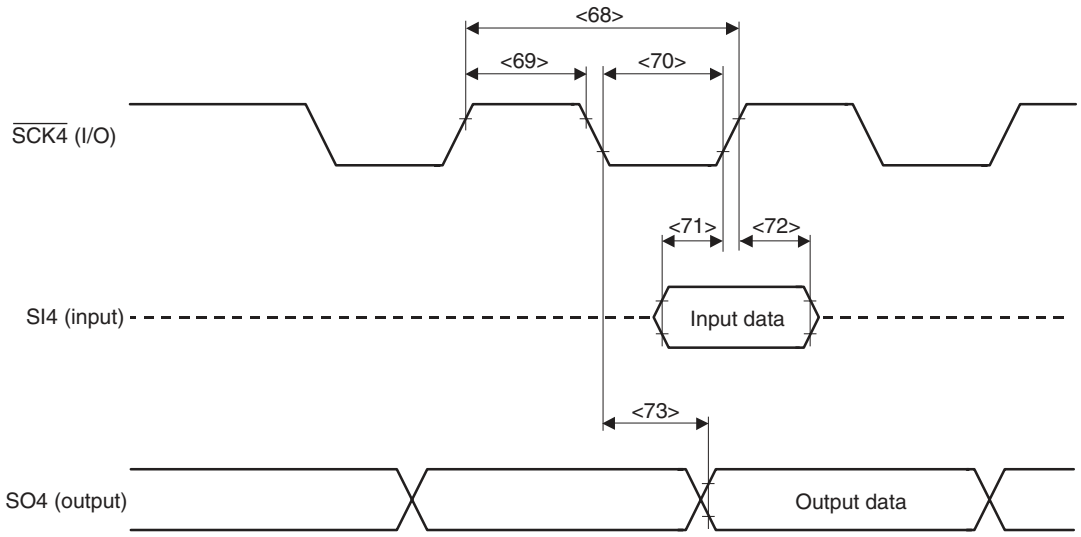
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK4}$ cycle	<68>	t_{KCY1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	200		ns
			3.0 V ≤ EV_{DD} < 4.0 V	400		ns
$\overline{SCK4}$ high-level width	<69>	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
$\overline{SCK4}$ low-level width	<70>	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
SI4 setup time (to $\overline{SCK4}$↑)	<71>	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	25		ns
			3.0 V ≤ EV_{DD} < 4.0 V	50		ns
SI4 hold time (from $\overline{SCK4}$↑)	<72>	t_{KSI1}		20		ns
Delay time from $\overline{SCK4}$↓ to SO4 output	<73>	t_{KSO1}			55	ns

(b) Slave mode

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK4}$ cycle	<68>	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	200		ns
			3.0 V ≤ EV_{DD} < 4.0 V	400		ns
$\overline{SCK4}$ high-level width	<69>	t_{KH2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
$\overline{SCK4}$ low-level width	<70>	t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
SI4 setup time (to $\overline{SCK4}$↑)	<71>	t_{SIK2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	25		ns
			3.0 V ≤ EV_{DD} < 4.0 V	50		ns
SI4 hold time (from $\overline{SCK4}$↑)	<72>	t_{KSI2}		20		ns
Delay time from $\overline{SCK4}$↓ to SO4 output	<73>	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		55	ns
			3.0 V ≤ EV_{DD} < 4.0 V		100	ns

★



Remark The broken lines indicate high impedance.

(10) I^2C bus mode (μPD703031AY, 703033AY, 70F3033AY only)

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency		–	f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		<74>	t_{BUF}	4.7	–	1.3	–	μs
Hold time[Note 1]		<75>	$t_{HD:STA}$	4.0	–	0.6	–	μs
SCLn clock low-level width		<76>	t_{LOW}	4.7	–	1.3	–	μs
SCLn clock high-level width		<77>	t_{HIGH}	4.0	–	0.6	–	μs
Setup time for start/restart conditions		<78>	$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	<79>	$t_{HD:DAT}$	5.0	–	–	–	μs
	I^2C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		<80>	$t_{SU:DAT}$	250	–	100[Note 4]	–	ns
SDAn and SCLn signal rise time		<81>	t_R	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDAn and SCLn signal fall time		<82>	t_F	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		<83>	$t_{SU:STO}$	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		<84>	t_{SP}	–	–	0	50	ns
Capacitance load of each bus line		–	Cb	–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDAn signal (at $V_{IHmin.}$ of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

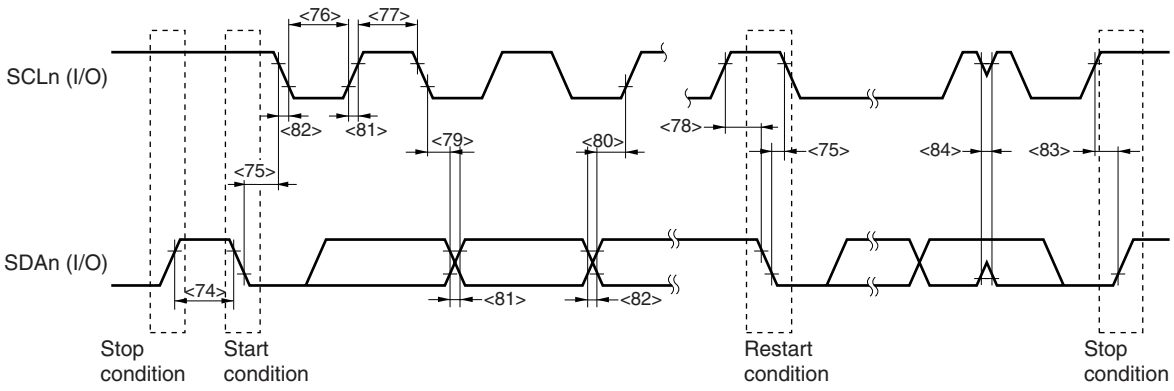
3. If the system does not extend the SCLn signal low-level width (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

4. The high-speed mode I^2C bus can be used in the normal-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

- If the system does not extend the SCLn signal's low-level width:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCLn signal's low-level width:
  Transmit the following data bit to the SDAn line prior to the SCLn line release ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode I^2C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark n = 0, 1


SCLn (I/O)
SDAn (I/O)
<74>
<75>
<76>
<77>
<78>
<79>
<80>
<81>
<82>
<83>
<84>
Stop condition
Start condition
Restart condition
Stop condition

Remark n = 0, 1

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10	10	10	bit
Overall error[Note 1]	–	ADM2 = 00H			±0.6	%FSR
		ADM2 = 01H			±1.0	%FSR
Conversion time	t_{CONV}		5		10	μs
Zero-scale error[Note 1]	–				±0.4	%FSR
Full-scale error[Note 1]	–	ADM2 = 00H			±0.4	%FSR
		ADM2 = 01H			±0.6	%FSR
Integral linearity error[Note 2]	–	ADM2 = 00H			±4.0	LSB
		ADM2 = 01H			±6.0	LSB
Differential linearity error[Note 2]	–	ADM2 = 00H			±4.0	LSB
		ADM2 = 01H			±6.0	LSB
Analog reference voltage	AV_{REF}	AV_{REF} = AV_{DD}	4.5		5.5	V
Analog power supply voltage	AV_{DD}		4.5		5.5	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} input current	AI_{REF}			1	2	mA
AV_{DD} power supply current	AI_{DD}	ADM2 = 00H		3	6	mA
		ADM2 = 01H		4	8	mA

Notes 1. Excluding quantization error (±0.05 %FSR)

2. Excluding quantization error (±0.5 LSB)

Remarks 1. LSB: Least Significant Bit
FSR: Full Scale Range

2. ADM2: A/D converter mode register 2

Regulator (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output stabilization time	t_{REG}	Stabilization capacitance C = 1 μF (Connected to REGC pin)	1			ms

Cautions 1. Be sure to start inputting supply voltage V_{DD} when $\overline{RESET}$ = V_{SS} = EV_{SS} = BV_{SS} = 0 V (the above state), and make $\overline{RESET}$ high level after the t_{REG} period has elapsed.

2. If supply voltage BV_{DD} or EV_{DD} is input before the t_{REG} period has elapsed following the input of supply voltage V_{DD}, note that data may be driven from the pins until the t_{REG} period has elapsed because the I/O buffers' power supply was turned on while the circuit was in an undefined state.

★ 3.1 Flash Memory Programming Mode (μPD70F3033A, 70F3033AY only)

Write/erase characteristics (T_A = 10 to 85°C … K rank product,
T_A = –20 to +85°C … E rank product,
V_{DD} = AV_{DD} = BV_{DD} = EV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} power supply voltage	V_{PP2}	During flash memory programming	7.5	7.8	8.1	V
V_{DD} power supply current	I_{DD}	When V_{PP} = V_{PP2}, f_{XX} = 20 MHz			63	mA
V_{PP} power supply current	I_{PP}	V_{PP} = V_{PP2}			100	mA
Step erase time	t_{ER}	**Note 1**		0.2		s
Overall erase time per area	t_{ERA}	When the step erase time = 0.2 s, **Note 2**			20	s/area
Write-back time	t_{WB}	**Note 3**		1		ms
Number of write-backs per write-back command	C_{WB}	When the write-back time = 1 ms, **Note 4**			300	Count/write-back command
Number of erase/write-backs	C_{ERWB}				16	Count
Step writing time	t_{WR}	**Note 5**		20		μs
Overall writing time per word	t_{WRW}	When the step writing time = 20 μs (1 word = 4 bytes), **Note 6**	20		200	μs/word
Number of rewrites per area	C_{ERWR}	1 erase + 1 write after erase = 1 rewrite, **Note 7**	**Note 8**			Count/area

Notes 1. The recommended setting value of the step erase time is 0.2 s.

2. The prewrite time prior to erasure and the erase verify time (write-back time) are not included.

3. The recommended setting value of the write-back time is 1 ms.

4. Write-back is executed once by the issuance of the write-back command. Therefore, the retry count must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step writing time is 20 μs.

6. 20 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.

7. When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)
Shipped product ⟶ P → E → P → E → P: 3 rewrites
Shipped product → E → P → E → P → E → P: 3 rewrites

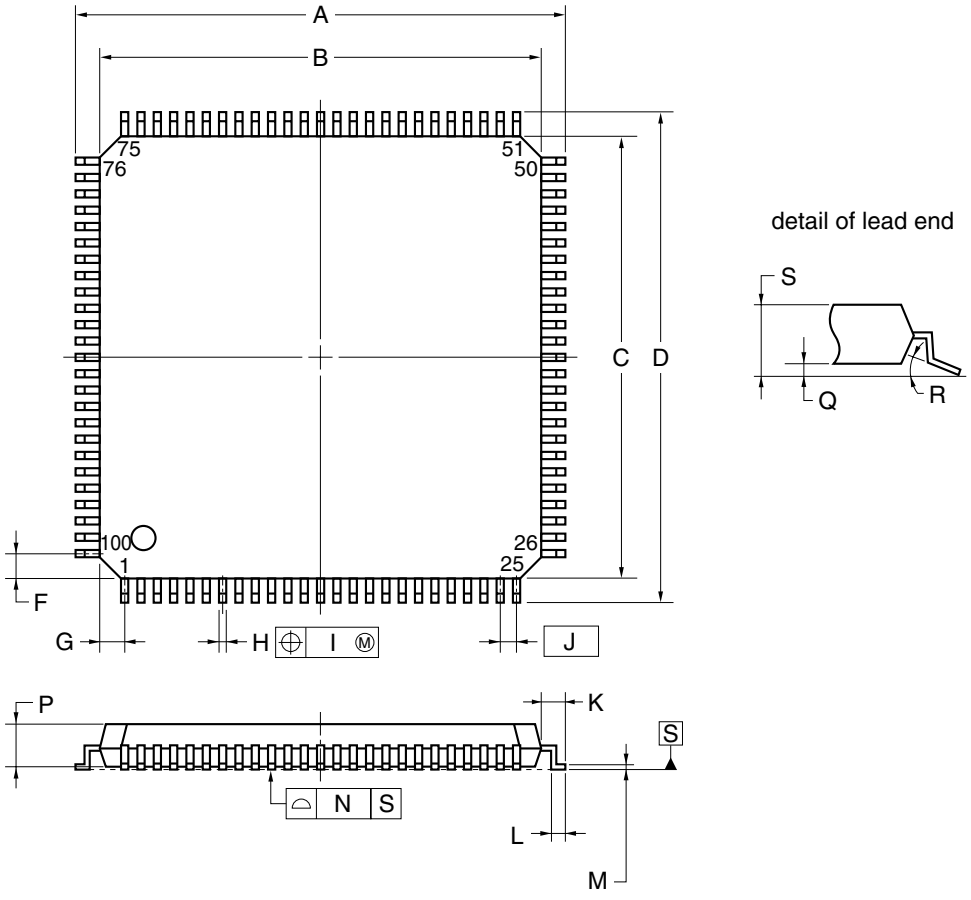
8. K rank product: 20 writes/area
E rank product: 100 writes/area

Remarks 1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings unless otherwise specified.

2. Area 0 = 000000H to 01FFFFH
Area 1 = 020000H to 03FFFFH

4. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



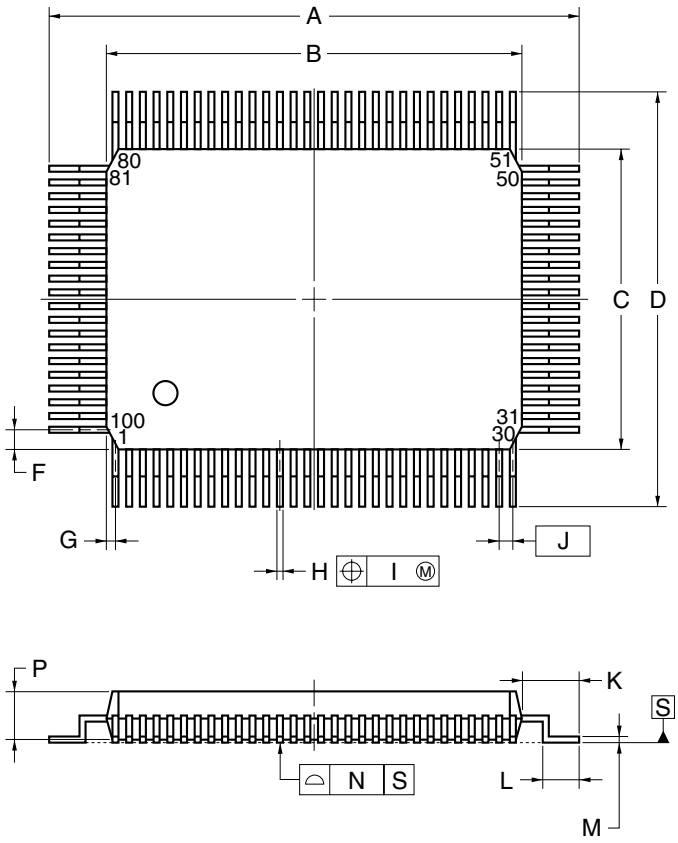
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

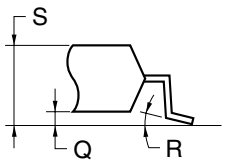
ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

100-PIN PLASTIC QFP (14x20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

5. RECOMMENDED SOLDERING CONDITIONS

The μPD703031A, 703031AY, 703033A, 703033AY, 70F3033A, and 70F3033AY should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 5-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD703031AGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703031AYGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703033AGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703033AYGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD70F3033AGC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD70F3033AYGC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Table 5-1. Surface Mounting Type Soldering Conditions (2/2)

(3) μPD703031AGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD703031AYGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD703033AGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD703033AYGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD70F3033AGF-3BA: 100-pin plastic QFP (14 × 20)
μPD70F3033AYGF-3BA: 100-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR35-207-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	VP15-207-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once Preheating temperature: 120°C max. (package surface temperature) Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	WS60-207-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

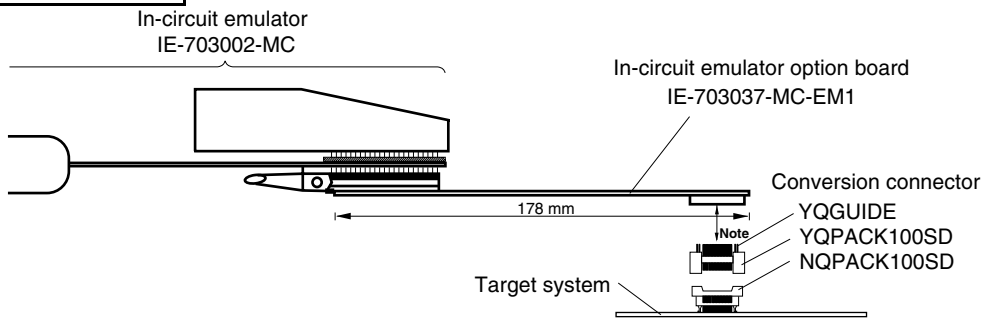
Caution Do not use different soldering methods together (except for partial heating).

★ APPENDIX NOTES ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.

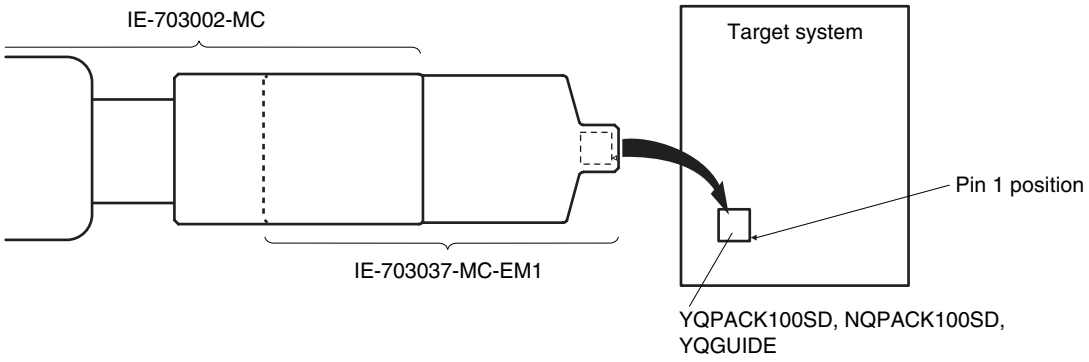
Appendix-1. 100-pin Plastic LQFP (Fine Pitch) (14 × 14)

Side view

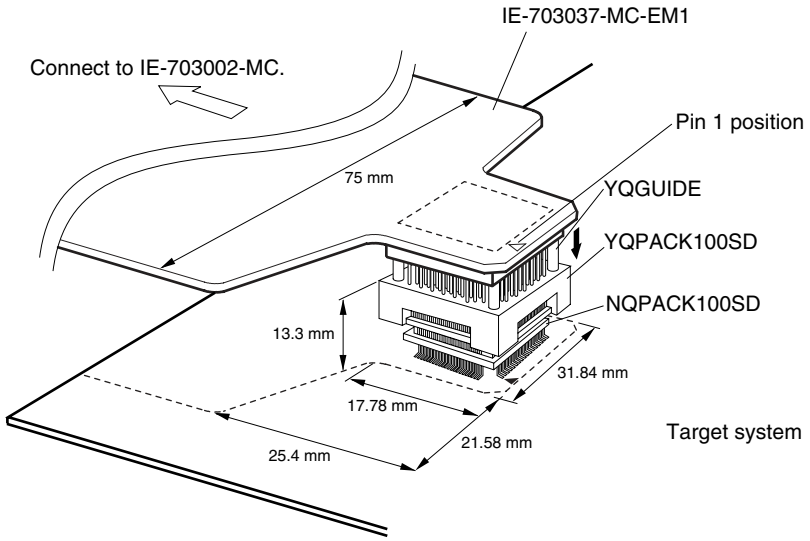


Note YQSOCKET100SDN (included with IE-703002-MC) can be inserted here to adjust the height (height: 3.2 mm).

Top view

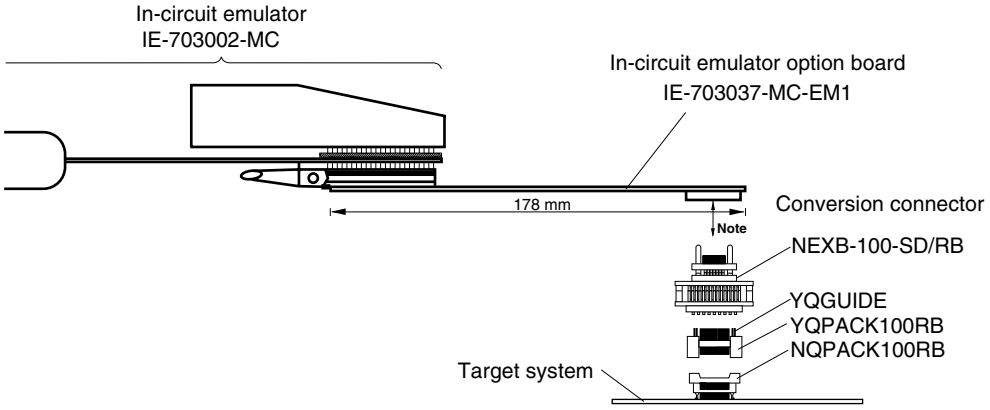


Connection condition diagram



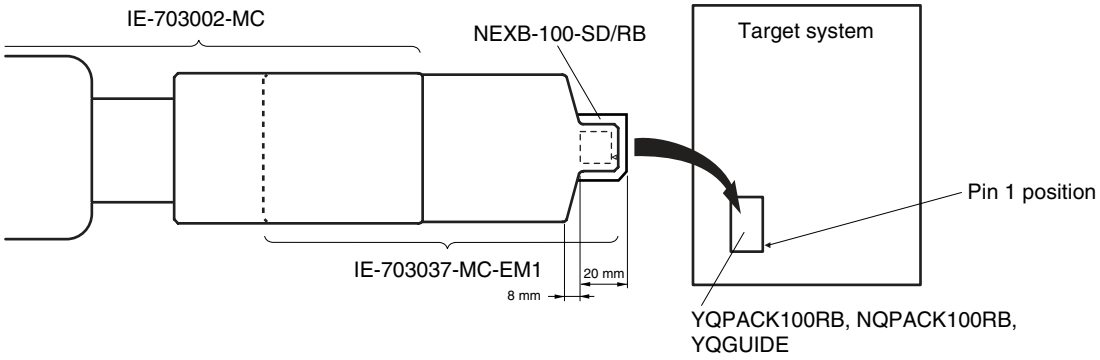
Appendix-2. 100-pin Plastic QFP (14 × 20)

Side view

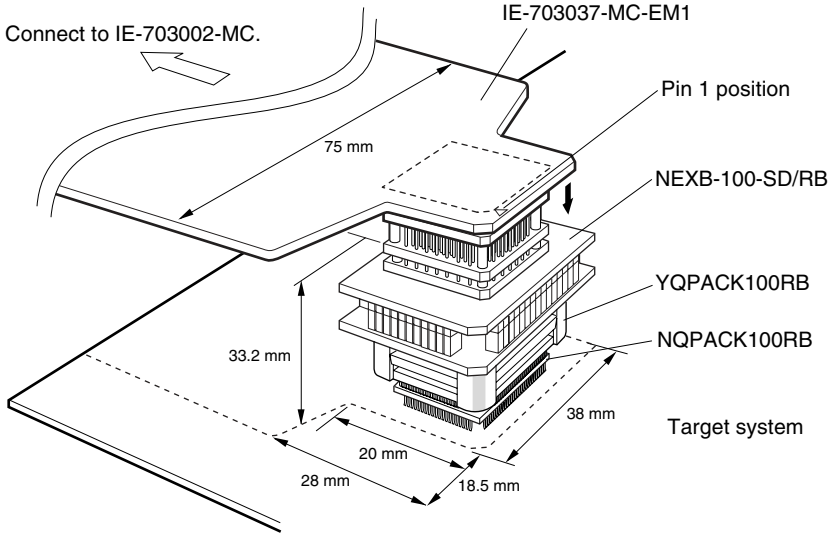


Note YQSOCKET100SDN (included with IE-703002-MC) to this portion for adjusting the height (height: 3.2 mm).

Top view



Connection condition diagram



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Caution Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Related document μPD703032A, 703032AY, 70F3032A, 70F3032AY Data Sheet (U14893E)

The related documents in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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