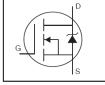
Source

HEXFET® Power MOSFET



- Logic -Level Gate Drive
- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ©
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

$V_{ t DSS}$	100V
$R_{DS(on)}$	0.18Ω
I _D	8.1A



Gate

Drain

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low onresistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Full Pak eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heat sink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heat sink using a single clip or by a single screw fixing.

Page Part Number Deckare Type		Standar	Ordershie Bert Number		
Base Part Number	Package Type	Form	Quantity	Orderable Part Number	
IRLI520NPbF	TO-220 Full-Pak	Tube	50	IRLI520NPbF	

Absolute Maximu		May	Huita
Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, V _{GS} @ 10V	8.1	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	5.7	A
I _{DM}	Pulsed Drain Current ① ⑥	35	
P _D @T _C = 25°C	Maximum Power Dissipation	30	W
	Linear Derating Factor	0.20	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②⑥	85	mJ
I _{AR}	Avalanche Current ①⑥	6.0	A
E _{AR}	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt36	5.0	V/ns
T _J	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
·	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{ heta JC}$	Junction-to-Case		5.0	°C/W
$R_{ heta JA}$	Junction-to-Ambient		65	C/VV



Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.11		V/°C	Reference to 25°C, I _D = 1mA ®
				0.18		$V_{GS} = 10V, I_D = 6.0A$
R _{DS(on)}	Static Drain-to-Source On-Resistance			0.22	Ω	$V_{GS} = 5.0V, I_D = 6.0A$
				0.26		$V_{GS} = 4.0V, I_D = 5.0A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0		2.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
gfs	Forward Trans conductance	3.1				V _{DS} = 25V, I _D = 6.0A®
	Drain to Source Leakage Current			25		$V_{DS} = 100V, V_{GS} = 0V$
I _{DSS}	Drain-to-Source Leakage Current			250	μA	$V_{DS} = 80V, V_{GS} = 0V, T_{J} = 150^{\circ}C$
1	Gate-to-Source Forward Leakage			100	nA	V _{GS} = 16V
I _{GSS}	Gate-to-Source Reverse Leakage			-100	IIA	$V_{GS} = -16V$
Qg	Total Gate Charge			20		$I_{D} = 6.0A$
Q_{gs}	Gate-to-Source Charge			4.6	nC	V _{DS} = 80V
Q_{gd}	Gate-to-Drain Charge			10		V _{GS} = 5.0V , See Fig. 6 and 13⊕⊚
$t_{d(on)}$	Turn-On Delay Time		40			V _{DD} = 50V
t _r	Rise Time		35		200	$I_{D} = 6.0A$
$t_{d(off)}$	Turn-Off Delay Time		23		ns	$R_G = 11\Omega, V_{GS} = 5.0V$
t _f	Fall Time		22			R _D = 8.2Ω, See Fig. 10④⑥
L _D	Internal Drain Inductance		4.5		l l	Between lead, 6mm (0.25in.)
L _S	Internal Source Inductance		7.5			from package and center of die contact
C _{iss}	Input Capacitance		440			$V_{GS} = 0V$
C _{oss}	Output Capacitance		97		pF	V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance		50		μr	f = 1.0MHz, See Fig. 5⑥
С	Drain to Sink Capacitance		12			f = 1.0MHz

Source-Drain Ratings and Characteristics

C G G G G	Journal Francisco					
	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current (Body Diode)			8.1		MOSFET symbol showing the
I _{SM}	Pulsed Source Current (Body Diode) ① ©			35		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 6.0A, V_{GS} = 0V $ ④
t _{rr}	Reverse Recovery Time		110	160	ns	$T_J = 25^{\circ}C$, $I_F = 6.0A$
Q _{rr}	Reverse Recovery Charge		410	620	nC	di/dt = 100A/µs ④⑥
t _{on}	Forward Turn-On Time	Intrinsio	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)			

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25$ °C, L = 4.7mH, $R_G = 25\Omega$, $I_{AS} = 6.0$ A (See fig. 12)
- $\label{eq:local_state} \mbox{ } \mbo$
- 4 Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.
- ⑤ t=60s, *f*=60Hz
- © Uses IRL520N data and test conditions.



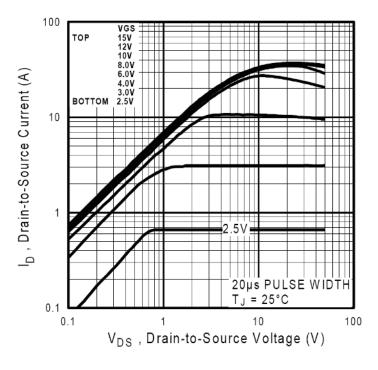


Fig. 1 Typical Output Characteristics

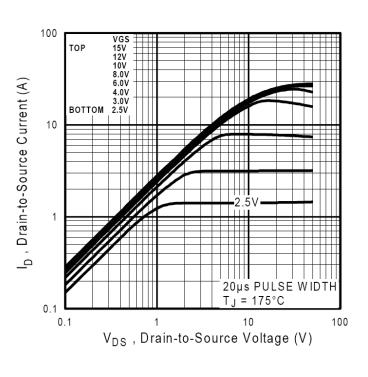


Fig. 2 Typical Output Characteristics

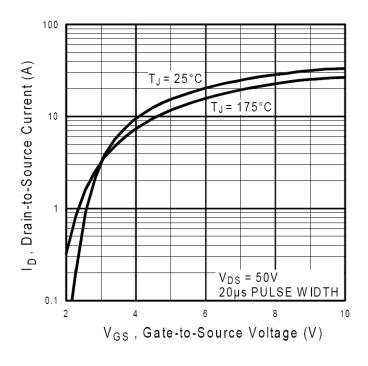


Fig. 3 Typical Transfer Characteristics

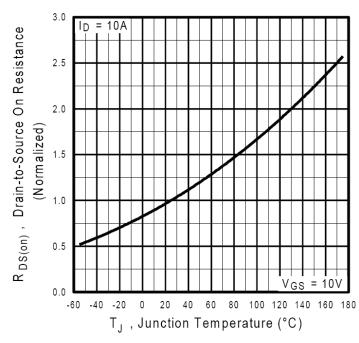


Fig. 4 Normalized On-Resistance vs. Temperature

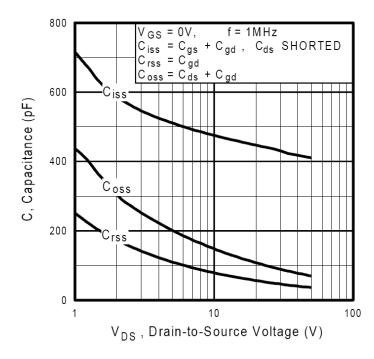


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

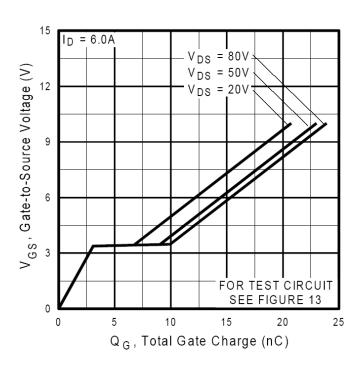


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

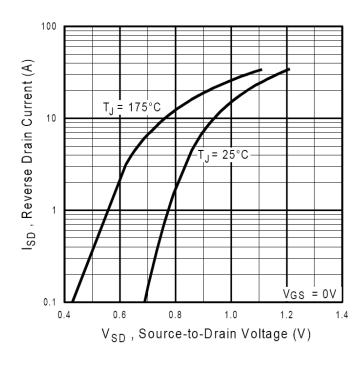


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

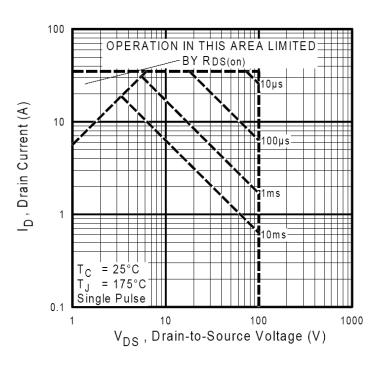


Fig 8. Maximum Safe Operating Area

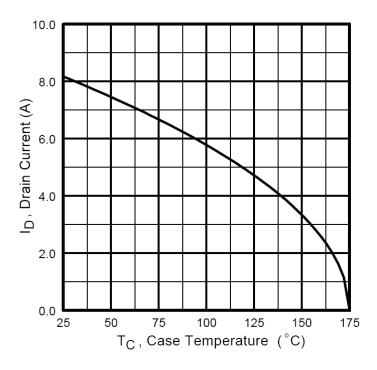


Fig 9. Maximum Drain Current vs. Case Temperature

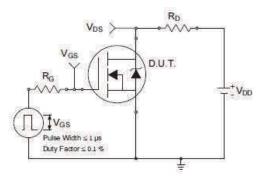


Fig 10a. Switching Time Test Circuit

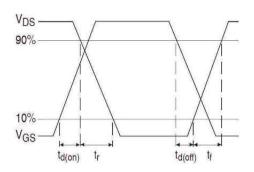


Fig 10b. Switching Time Waveforms

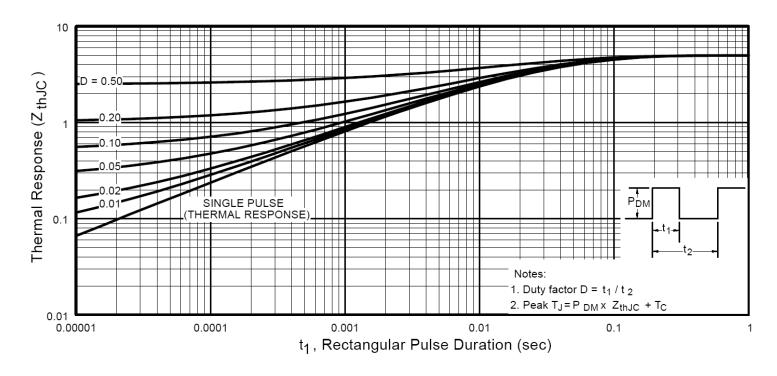


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



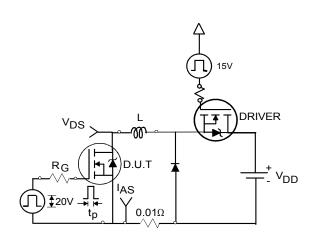


Fig 12a. Unclamped Inductive Test Circuit

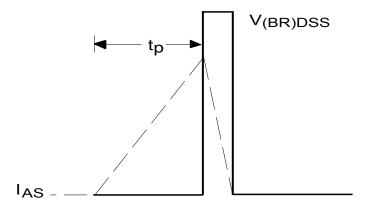


Fig 12b. Unclamped Inductive Waveforms

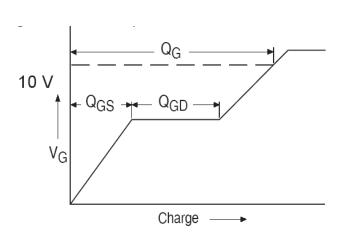


Fig 13a. Gate Charge Waveform

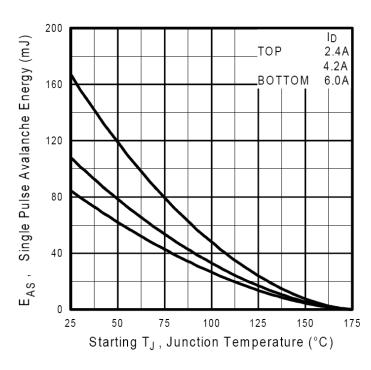


Fig 12c. Maximum Avalanche Energy vs. Drain Current

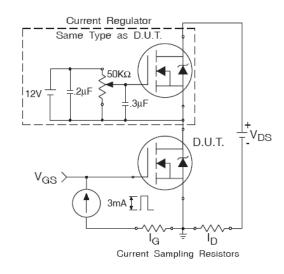
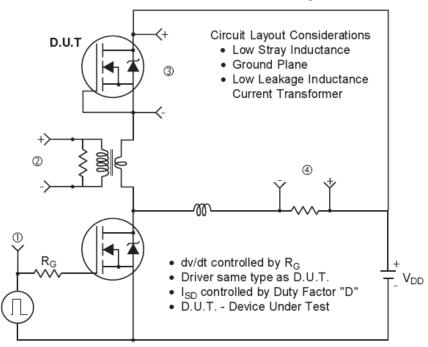


Fig 13b. Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



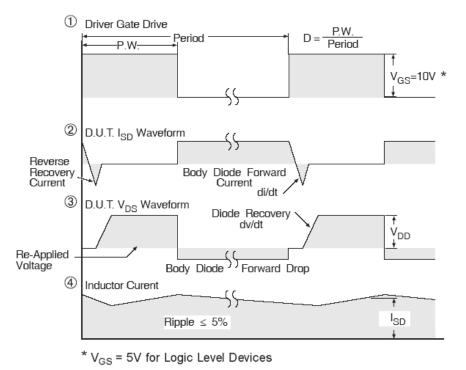
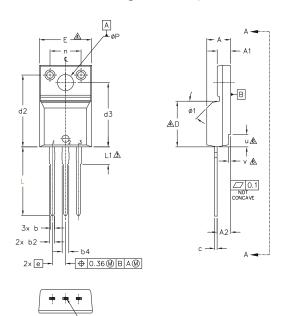
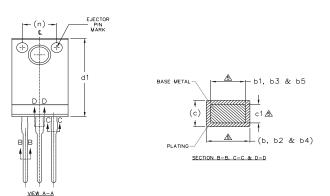


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))





NOTES:

1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.

2,0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.

DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.

50 DIMENSION 61, 63, 65 & c1 APPLY TO BASE METAL ONLY.

 $\cancel{6.0}$ STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.

7.0 CONTROLLING DIMENSION: INCHES.

S	DIMENSIONS				Ň	
M B O	MILLIMETERS		INC	INCHES		
L	MIN.	MAX.	MIN.	MAX.	O T E S	
А	4.57	4.83	.180	.190		
A1	2.57	2.82	.101	.111		
A2	2.51	2.92	.099	.115		
Ь	0.61	0.94	.024	.037		
ь1	0.61	0.89	.024	.035	5	
b2	0.76	1.27	.030	.050		
ь3	0.76	1.22	.030	.048	5	
Ь4	1.02	1.52	.040	.060		
b5	1.02	1.47	.040	.058	5	
С	0.33	0.63	.013	.025		
c1	0.33	0.58	.013	.023	5	
D	8.66	9.80	.341	.386	4	
d1	15.80	16.13	.622	.635		
d2	13.97	14.22	.550	.560		
d3	12.29	12.93	.484	.509		
E	9.63	10.74	.379	.423	4	
е		BSC		BSC		
L	13.21	13.72	.520	.540		
L1	3.10	3.68	.122	.145	3	
n	6.05	6.60	.238	.260		
ØΡ	3.05	3.45	.120	.136		
u	2.39	2.49	.094	.098	6	
V	0.41	0.51	.016	.020	6	
Ø1	_	45°	_	45°		

LEAD ASSIGNMENTS

<u>HEXFET</u>

1.- GATE

2. – DRAIN

3.- SOURCE

IGBTs, CoPACK

1.- GATE

2.- COLLECTOR

3.- EMITTER

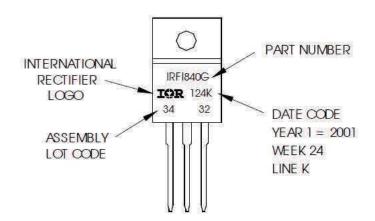
TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G WITH ASSEMBLY

LOT CODE 3432

ASSEMBLED ON WW 24, 2001 IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at http://www.irf.com/package/



Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) [†]			
Moisture Sensitivity Level	TO-220 Full-Pak N/A			
RoHS Compliant	Yes			

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments		
4/27/17	 Changed datasheet with Infineon logo - all pages. Corrected Package Outline on page 8. Added disclaimer on last page. 		

Trademarks of Infineon Technologies AG

HVIC™, µIPM™, µPFC™, AU-ConvertIR™, AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolDP™, CoolGaN™, COOLIR™, CoolMOS™, CoolSET™, CoolSET™, CoolSiC™, DAVE™, DI-POL™, DirectFET™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, GaNpowIR™, HEXFET™, HITFET™, HybridPACK™, iMOTION™, IRAM™, ISOFACE™, IsoPACK™, LEDrivIR™, LITIX™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OPTIGA™, OptiMOS™, ORIGA™, PowIRaudio™, PowIRStage™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, SmartLEWIS™, SOLID FLASH™, SPOC™, StrongIRFET™, SupIRBuck™, TEMPFET™, TRENCHSTOP™, TriCore™, UHVIC™, XHP™, XMC™

Trademarks updated November 2015

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2016-04-19 Published by Infineon Technologies AG 81726 Munich, Germany

© 2016 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference ifx1

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or **characteristics ("Beschaffenheitsgarantie").**

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

Please note that this product is not qualified according to the AEC Q100 or AEC Q101 documents of the Automotive Electronics Council.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.