

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R053-93.	93-01-07	M. A. Frye
B	Changes in accordance with NOR 5962-R060-94.	93-12-06	M. A. Frye
C	Changes in accordance with NOR 5962-R041-95	94-11-30	M. A. Frye
D	Redrawn with changes. Add case outline X. Technical and editorial changes throughout.	95-03-24	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

<p>PMIC N/A</p> <p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p>AMSC N/A</p>	PREPARED BY Rick C Officer	<p align="center">DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</p> <p align="center">MICROCIRCUIT, LINEAR, CMOS QUAD, SPST ANALOG SWITCH, MONOLITHIC SILICON</p>	
	CHECKED BY Charles E Besore		
	APPROVED BY Michael A Frye		
	DRAWING APPROVAL DATE 92-01-13		
	REVISION LEVEL D		
	SIZE A	CAGE CODE 67268	5962-90731
	SHEET 1	OF 14	

1.3 Absolute maximum ratings. 1/

V+ to V-	44 V dc
Ground to V-	25 V dc
Logic supply voltage (V _L) to V-	(Ground -0.3 V dc) to 44 V dc 2/
Digital inputs, V _S , V _D	(V-) -2.0 V dc to (V+) +2.0 V dc or 30 mA, whichever occurs first 2/
Continuous current (any terminal)	30 mA
Source or drain current (pulsed, 1.0 ms, 10% duty cycle)	100 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation, T _A = +25°C (P _D):	
Case E	900 mW 3/
Case F and X	485 mW 4/
Case 2	750 mW 5/
Thermal resistance, junction-to-case (Θ _{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Unipolar supply voltage:	
V+	12 V dc
V-	0 V dc
Bipolar supply voltage:	
V+	15 V dc
V-	-15 V dc
Logic supply voltage (V _L)	5.25 V dc
Ambient operating temperature range (T _A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- 3/ Derate above T_A = +75°C at 12 mW/°C.
- 4/ Derate above T_A = +70°C at 6.06 mW/°C.
- 5/ Derate above T_A = +75°C at 10 mW/°C.

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HANDBOOK

MILITARY

MIL-HDBK-788 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Drain-to-source ON resistance	r _{DS(ON)}	V ₊ = 13.5 V, V ₋ = -13.5 V, I _S = -10 mA, V _D = ±8.5 V	V _{IN} = 0.8 V	1,3	01	0	35	Ω
				2		0	45	
			V _{IN} = 2.4 V	1,3	02	0	35	
				2		0	45	
			V _{IN} = 0.8 V or 2.4 V <u>2/</u>	1,3	03	0	35	
				2		0	45	
	V ₊ = 10.8 V, V ₋ = 0 V, I _S = -10 mA, V _D = 3.0 V and 8.0 V	V _{IN} = 0.8 V	1,3	01	0	80		
			2		0	100		
		V _{IN} = 2.4 V	1,3	02	0	80		
			2		0	100		
		V _{IN} = 0.8 V or 2.4 V <u>2/</u>	1,3	03	0	80		
			2		0	100		
Source OFF Leakage current	I _{S(OFF)}	V ₊ = 16.5 V, V ₋ = -16.5 V, V _D = -15.5 V, V _S = 15.5 V	V _{IN} = 2.4 V	1	01	-0.25	+0.25	nA
				2,3		-20	+20	
			V _{IN} = 0.8 V	1	02	-0.25	+0.25	
				2,3		-20	+20	
			V _{IN} = 0.8 V or 2.4 V <u>2/</u>	1	03	-0.25	+0.25	
				2,3		-20	+20	
	V ₊ = 16.5 V, V ₋ = -16.5 V, V _D = 15.5 V, V _S = -15.5 V	V _{IN} = 2.4 V	1	01	-0.25	+0.25		
			2,3		-20	+20		
		V _{IN} = 0.8 V	1	02	-0.25	+0.25		
			2,3		-20	+20		
		V _{IN} = 0.8 V or 2.4 V <u>2/</u>	1	03	-0.25	+0.25		
			2,3		-20	+20		

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Drain OFF leakage current	I _{D(OFF)}	V ₊ = 16.5 V, V ₋ = -16.5 V, V _D = -15.5 V, V _S = 15.5 V	V _{IN} = 2.4 V	1	01	-0.25	+0.25	nA
				2,3		-20	+20	
			V _{IN} = 0.8 V	1	02	-0.25	+0.25	
				2,3		-20	+20	
			V _{IN} = 0.8 V or 2.4 V 2/	1	03	-0.25	+0.25	
				2,3		-20	+20	
	V ₊ = 16.5 V, V ₋ = -16.5 V, V _D = 15.5 V, V _S = -15.5 V	V _{IN} = 2.4 V	1	01	-0.25	+0.25		
			2,3		-20	+20		
		V _{IN} = 0.8 V	1	02	-0.25	+0.25		
			2,3		-20	+20		
		V _{IN} = 0.8 V or 2.4 V 2/	1	03	-0.25	+0.25		
			2,3		-20	+20		
Channel ON leakage current	I _{D(ON)} +	V ₊ = 16.5 V, V ₋ = -16.5 V, V _S = V _D = ±15.5 V	V _{IN} = 0.8 V	1	01	-0.4	+0.4	nA
				2,3		-40	+40	
	I _{S(ON)}		V _{IN} = 2.4 V	1	02	-0.4	+0.4	
				2,3		-40	+40	
			V _{IN} = 0.8 V or 2.4 V 2/	1	03	-0.4	+0.4	
				2,3		-40	+40	
Input current with V _{IN} low	I _{IL}	Input under test = 0.8 V, all others = 2.4 V	1,2,3	ALL	-0.5	+0.5	μA	
Input current with V _{IN} high	I _{IH}	Input under test = 2.4 V, all others = 0.8 V	1,2,3	ALL	-0.5	+0.5	μA	
Turn ON time	t _{ON}	See figure 4, R _L = 300Ω, C _L = 35 pF, V _S = ±10 V	9,11	ALL	0	175	ns	
			10		0	240		
		See figure 4, R _L = 300Ω, V ₊ = 12 V, V ₋ = 0 V, C _L = 35 pF, V _S = +8 V	9,11	ALL	0	250	ns	
			10		0	400		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Turn OFF time	t _{OFF}	See figure 4, R _L = 300Ω, C _L = 35 pF, V _S = ±10 V	9,11	ALL	0	145	ns
			10		0	160	
		See figure 4, R _L = 300Ω, V ₊ = 12 V, V ₋ = 0 V, C _L = 35 pF, V _S = +8 V,	9,11	ALL	0	125	ns
			10		0	140	
Charge injection 3/	Q	V _{GEN} = 0 V, R _{GEN} = 0Ω, T _A = +25°C, C _L = 10 nF, see figure 5	9	ALL	-100	+100	pC
		V _{GEN} = 6.0 V, R _{GEN} = 0Ω, T _A = +25°C, C _L = 10 nF, V ₊ = 12 V, V ₋ = 0 V, see figure 5	9		-100	+100	
Positive supply current	I ₊	V ₊ = 16.5 V, V ₋ = -16.5 V, V _{IN} = 0 V or 5.0 V	1	ALL		+1.0	μA
			2,3			+5.0	
		V ₊ = 13.2 V, V ₋ = 0 V, V _{IN} = 0 V or 5.0 V, V _L = 5.25 V	1	ALL		+1.0	μA
			2,3			+5.0	
Negative supply current	I ₋	V ₊ = 16.5 V, V ₋ = -16.5 V, V _{IN} = 0 V or 5.0 V	1	ALL	-1.0		μA
			2,3			-5.0	
		V ₊ = 13.2 V, V ₋ = 0 V, V _{IN} = 0 V or 5.0 V, V _L = 5.25 V	1	ALL	-1.0		μA
			2,3			-5.0	
Logic supply current	I _L	V ₊ = 16.5 V, V ₋ = -16.5 V, V _{IN} = 0 V or 5.0 V	1	ALL		+1.0	μA
			2,3			+5.0	
		V ₊ = 13.2 V, V ₋ = 0 V, V _{IN} = 0 V or 5.0 V, V _L = 5.25 V	1	ALL		+1.0	μA
			2,3			+5.0	
Ground current	I _{GND}	V ₊ = 16.5 V, V ₋ = -16.5 V, V _{IN} = 0 V or 5.0 V	1	ALL	-1.0		μA
			2,3			-5.0	
		V ₊ = 13.2 V, V ₋ = 0 V, V _{IN} = 0 V or 5.0 V, V _L = 5.25 V	1	ALL	-1.0		μA
			2,3			-5.0	
Functional tests		See figure 2 and 4.4.1	7,8				

1/ V₊ = 15 V, V₋ = -15 V, V_L = 5 V and GND = 0 V, unless otherwise specified.

2/ V_{IN} = input voltage to perform proper function.

3/ Parameter shall be guaranteed to the limits specified, if not tested.

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Device types	01, 02, and 03	
Case outlines	E, F, X	2
Terminal number	Terminal symbol	
1	INPUT 1 (IN_1)	NC
2	DRAIN 1 (D_1)	INPUT 1 (IN_1)
3	SOURCE 1 (S_1)	DRAIN 1 (D_1)
4	V-	SOURCE 1 (S_1)
5	GROUND (GND)	V-
6	SOURCE 4 (S_4)	NC
7	DRAIN 4 (D_4)	GROUND (GND)
8	INPUT 4 (IN_4)	SOURCE 4 (S_4)
9	INPUT 3 (IN_3)	DRAIN 4 (D_4)
10	DRAIN 3 (D_3)	INPUT 4 (IN_4)
11	SOURCE 3 (S_3)	NC
12	V _L	INPUT 3 (IN_3)
13	V ₊	DRAIN 3 (D_3)
14	SOURCE 2 (S_2)	SOURCE 3 (S_3)
15	DRAIN 2 (D_2)	V _L
16	INPUT 2 (IN_2)	NC
17	---	V ₊
18	---	SOURCE 2 (S_2)
19	---	DRAIN 2 (D_2)
20	---	INPUT 2 (IN_2)

FIGURE 1. Terminal connections.

Device type 01

Logic	Switch 1, 2, 3, and 4
0	ON
1	OFF

Device type 02

Logic	Switch 1, 2, 3, and 4
0	OFF
1	ON

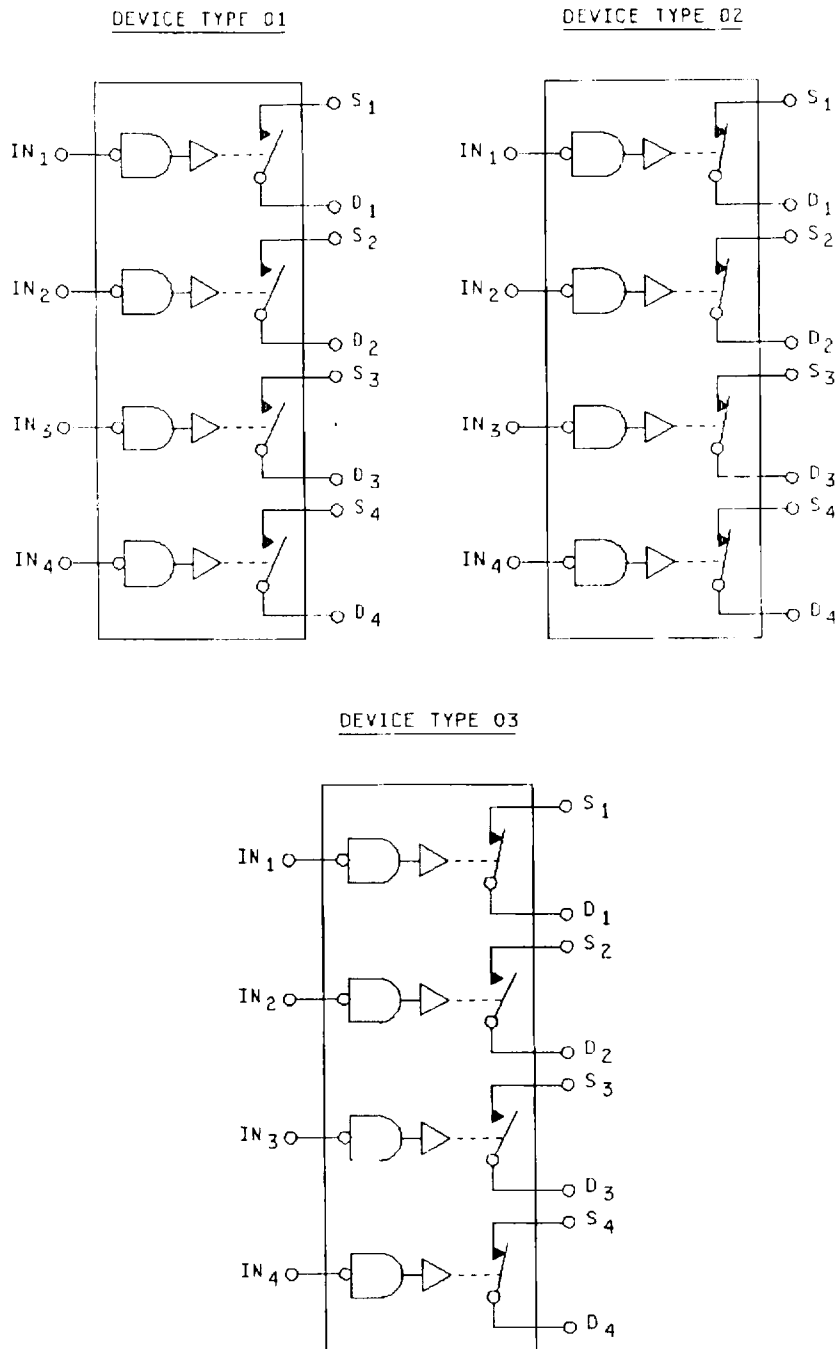
Device type 03

Logic	Switch 1 and 4	Switch 2 and 3
0	OFF	ON
1	ON	OFF

Logic "0" \leq 0.8 V
 Logic "1" \geq 2.4 V

FIGURE 2. Truth tables.

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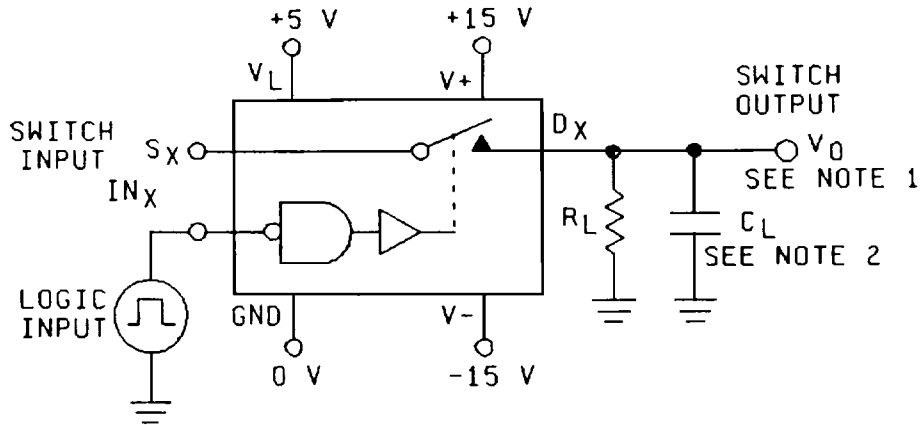


NOTE: All switches are shown for logic "1" input.

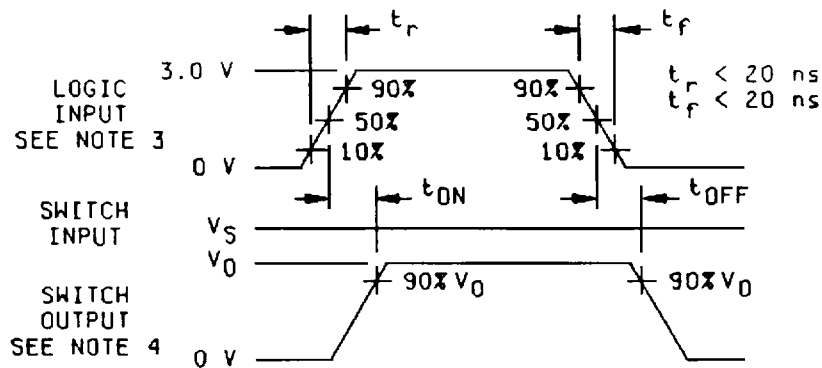
FIGURE 3. Block diagrams.

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Device types 01, 02, and 03
TEST CIRCUIT



SWITCHING WAVEFORMS



NOTES:

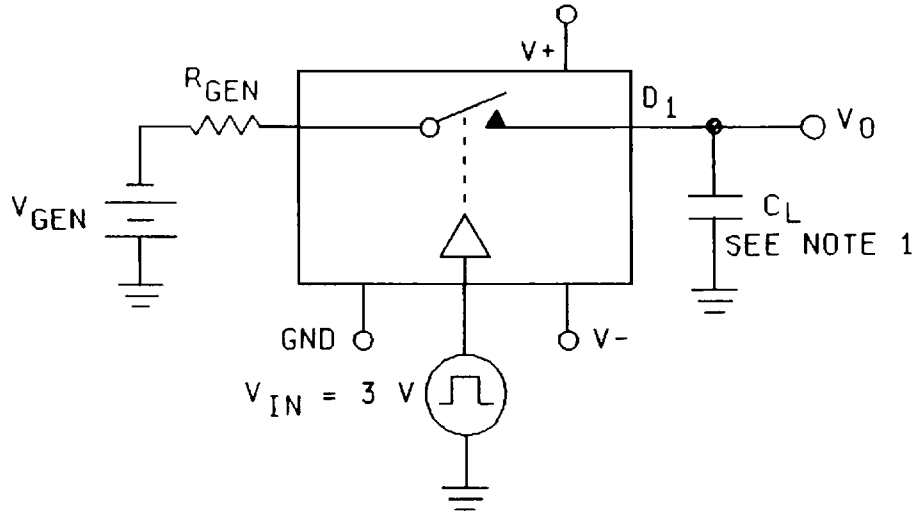
1. $V_0 = V_S \frac{R_L}{R_L + R_{DS(ON)}}$
2. C_L includes fixture and stray capacitance.
3. LOGIC INPUT waveform is inverted for switches that have the opposite logic sense.
4. V_0 is the steady state output with the switch ON. Feed through via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

FIGURE 4. Switching times test circuit and waveforms.

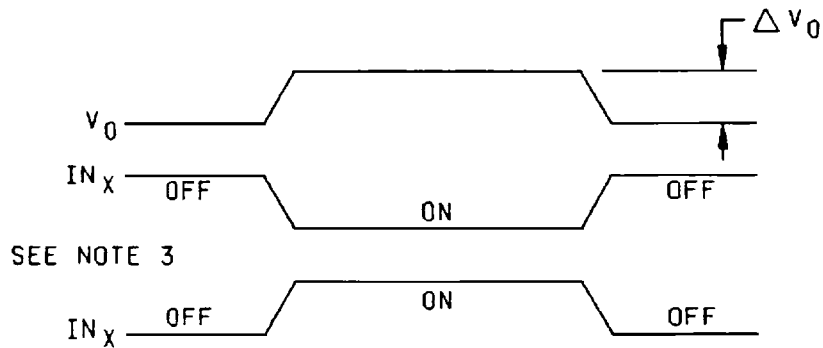
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Device types 01, 02, and 03

TEST CIRCUIT



CHARGE INJECTION WAVEFORMS (SEE NOTE 2)



NOTES:

1. C_L includes fixture and stray capacitance.
2. Charge injection $\Delta(Q) = \Delta V_O C_L$.
3. Input polarity determined by sense of switch.

FIGURE 5. Charge injection test circuit and waveform.

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3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 82 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	1	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, F, G, L, R, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Microcircuit and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document Listing</u>
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-03-24

Approved sources of supply for SMD 5962-90731 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-9073101MEX	17856 1ES66 34371	DG411AK/883 DG411AK/883B DG411AK/883
5962-9073101MFX	<u>2/</u>	DG411AL/883B
5962-9073101MXX	1ES66	DG411AL/883B
5962-9073101M2X	17856 1ES66	DG411AZ/883 DG411AZ/883B
5962-9073102MEX	17856 1ES66 34371	DG412AK/883 DG412AK/883B DG412AK/883
5962-9073102MFX	<u>2/</u>	DG412AL/883B
5962-9073102MXX	1ES66	DG412AL/883B
5962-9073102M2X	1ES66	DG412AZ/883
5962-9073103MEX	17856 1ES66 34371	DG413AK/883 DG413AK/883B DG413AK/883
5962-9073103MFX	<u>2/</u>	DG413AL/883B
5962-9073103MXX	1ES66	DG413AL/883B
5962-9073103M2X	1ES66	DG413AL/883B

1/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source of supply.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
17856	Siliconix 2201 Laurelwood Road Santa Clara, CA 95054-2754
1ES66	Maxim 120 San Gabriel Drive Sunnyvale, CA 94086-5126
34371	Harris Semiconductor PO Box 883 Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.