BGS12SL6

0.1 - 6.0 GHz SPDT Switch in ultra small package with 0.77mm^2 footprint

Data Sheet

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Final

Power Management & Multimarket

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Revision History

Document No.: BGS12SL6.pdf

Previous Version: Revision 1.1, October 22, 2013

Page	Subjects (major changes since last revision)
10	Updated Temperature Range in Table 6

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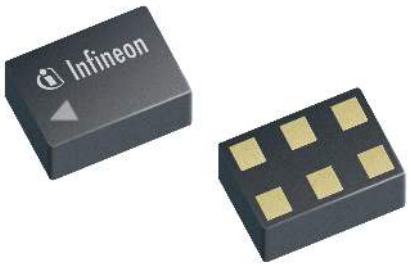
1 Features



- 2 high-linearity TRx paths with power handling capability of up to 27.5 dBm
- High switching speed, ideal for WLAN and Bluetooth applications
- All ports fully bi-directional
- Low insertion loss
- Low harmonic generation
- High port-to-port isolation
- 0.1 to 6 GHz coverage
- High ESD robustness
- On-chip control logic
- Very small leadless and halogen free package TSLP-6-4 (0.7x1.1mm^2) with super low height of 0.31 mm
- No decoupling capacitors required if no DC applied on RF lines
- RoHS compliant package

RoHS

2 Product Description

The BGS12SL6 RF MOS switch is a general purpose 0.1 - 6.0 *GHz* SPDT Switch suitable for band/mode switching in cellular systems and WLAN applications. Any of the 2 ports can be used as termination of the diversity antenna handling up to 27.5 dBm.

This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. The 0.1 dB compression point exceeds the switch's maximum input power level, resulting in linear performance at all signal levels. The RF switch has a very low insertion loss of 0.25 dB in the 1 GHz and 0.35 dB in the 2.5 GHz range.

The BGS12SL6 RF switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness.

The device has a very small size of only 0.7x1.1mm^2 and a low height of 0.31mm. No decoupling capacitors are required in typical applications as long as no DC is applied to any RF port.

Table 1: Ordering Information

Type	Package	Marking
BGS12SL6	TSLP-6-4	S

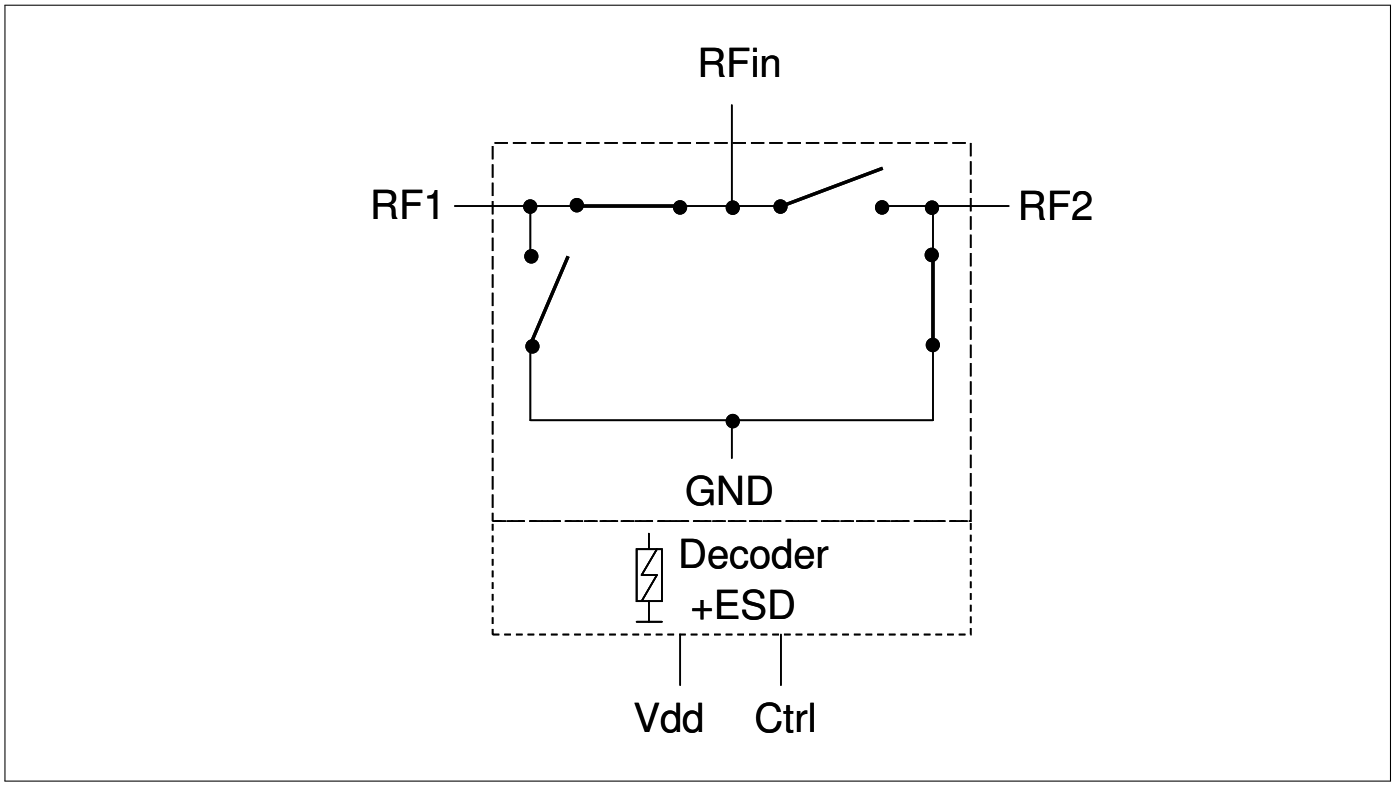


Figure 1: BGS12SL6 Block Diagram

Table 2: Truth Table

Switched Paths	Ctrl
RFin - RF1	0
RFin - RF2	1

3 Maximum Ratings

Table 3: Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{dd}	-0.5	–	5.5	V	–
Control Voltage	V_{Ctrl}	-0.3	–	3.6	V	–
Storage Temperature Range	T_{STG}	-55	–	150	°C	–
RF Input Power	P_{RF}	–	–	29	dBm	–
Junction Temperature	T_j	–	–	125	°C	–
ESD Capability						
Human Body Model [1]	V_{ESD_HBM}	−1	–	+1	kV	–
ESD Capability RFin Port [2]	V_{ESD_RFin}	−8	–	+8	kV	RFin versus GND, with 27 nH shunt inductor

[1] Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
[2] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Attention:
Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A	-40	25	85	°C	–
RF Frequency	f	0.1	–	6	GHz	–
Supply Voltage	V_{dd}	2.4	–	3.6	V	–
Control Voltage Low	V_{Ctrl_L}	-0.3	–	0.3	V	–
Control Voltage High	V_{Ctrl_H}	1.4	–	V_{dd}	V	–

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF Input Power (50Ω)	P_{In}	–	–	27.5	dBm	–

5 RF Characteristics

Table 6: RF Characteristics

Test Conditions (unless otherwise specified):

- Terminating port impedance: Z_0 = 50 Ω
- Temperature range: T_A = -40 ... +85 °C
- Supply voltage: V_{dd} = 2.4 ... 3.6 V
- Input power: P_{IN} = 0 dBm

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss						
All RF Ports	*IL*	0.15	0.25	0.40	dB	824-915 MHz
		0.20	0.30	0.50	dB	1710-1910 MHz
		0.28	0.35	0.60	dB	2170-2690 MHz
		0.78	1.00	1.40	dB	5000 MHz
		1.30	1.50	2.00	dB	6000 MHz
Insertion Loss[1]						
All RF Ports	*IL*	0.24	0.25	0.30	dB	824-915 MHz
		0.28	0.30	0.38	dB	1710-1910 MHz
		0.30	0.35	0.50	dB	2170-2690 MHz
		0.85	1.00	1.28	dB	5000 MHz
		1.35	1.50	1.80	dB	6000 MHz
Return Loss						
All RF Ports	*RL*	23	27	33	dB	824-915 MHz
		19	22	24	dB	1710-1910 MHz
		15	20	22	dB	2170-2690 MHz
		11	14	20	dB	5000 MHz
		10	12	18	dB	6000 MHz
Isolation						
RFin to RF1/RF2 Port	$ISO_{RFin-RFx}$	32	36	38	dB	824-915 MHz
		26	29	32	dB	1710-1910 MHz
		22	26	30	dB	2170-2690 MHz
		13	16	18	dB	5000 MHz
		12	15	17	dB	6000 MHz
RF1 to RF2 Port / RF2 to RF1 Port	$ISO_{Port-Port}$	45	48	50	dB	824-915 MHz
		33	35	38	dB	1710-1910 MHz
		27	29	32	dB	2170-2690 MHz
		15	18	20	dB	5000 MHz
		14	17	19	dB	6000 MHz

[1] T_A = +25 °C, V_{dd} = 3 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation up to 12.75 GHz[1]						
All RF Ports, 2nd Harmonic	P_{Harm}	–	-85	-80	dBc	f = 824 *MHz*, P_{in} = 27.5 *dBm*, 50 % duty cycle, 50Ω
All RF Ports, 3rd Harmonic		–	-80	-75	dBc	
Intermodulation Distortion in Rx Band[1]						
IMD2	*IMD*2	–	-110	-100	dBm	Tx_{LB} = 15 dBm, Tx_{HB} = 10 dBm, Interferer = -15 dBm, 50Ω
IMD3	*IMD*3	–	-120	-110	dBm	
Switching Time and Current Consumption						
RF Rise Time	$t_{10\%-90\%}$	–	35	100	ns	10% - 90% of RF Signal
Ctrl to RF Time	$t_{Ctrl-RF}$	–	125	350	ns	50% of Ctrl Signal to 90% of RF Signal
Supply Current	I_{dd}	–	150	200	µA	T_A = *+25 °C*
Control Current	I_{Ctrl}	–	1	10	µA	–

Note: All electrical characteristics are measured with all RF ports terminated by 50 Ω loads.

[1] T_A = *+25 °C*, V_{dd} = 3 *V*

6 Pin Description

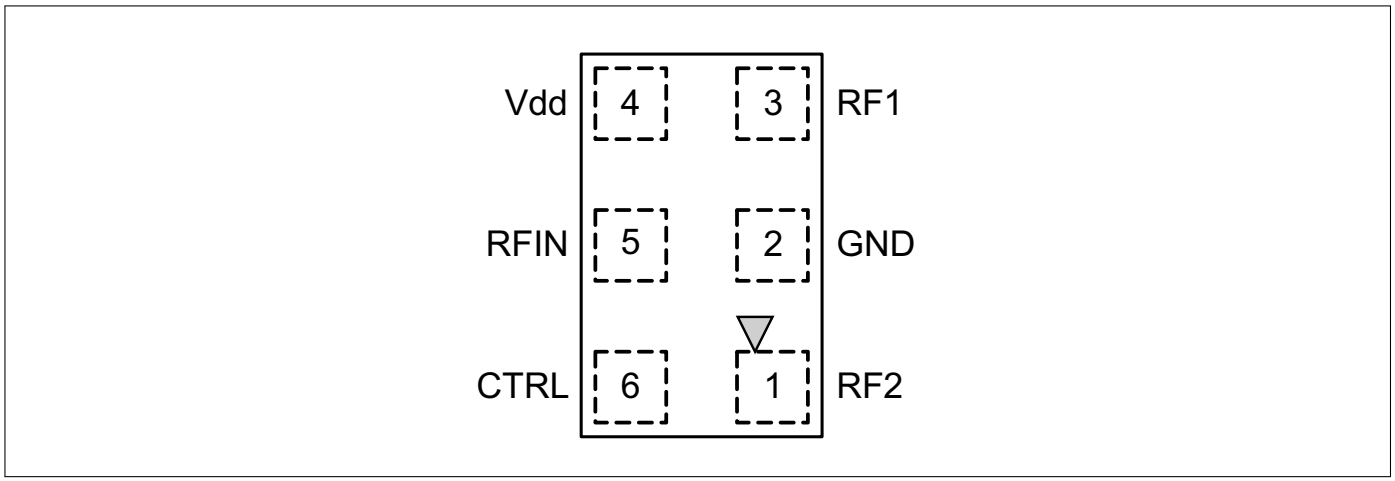


Figure 2: Pin Configuration

Table 7: Pin Description

Pin No.	Name	Pin Type	Buffer Type	Function
1	RF2	I/O		RF Port 2
2	GND	GND		Ground
3	RF1	I/O		RF Port 1
4	Vdd	PWR		Supply Voltage
5	RFIN	I/O		RF Port In
6	CTRL	I		Control Pin

7 Package Information

Table 8: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	*X*	0.7 $\pm$ 0.05	*mm*
Y-Dimension	*Y*	1.1 $\pm$ 0.05	*mm*
Size	*Size*	0.77	mm^2
Height	*H*	$0.31^{+0.01/-0.02}$	*mm*

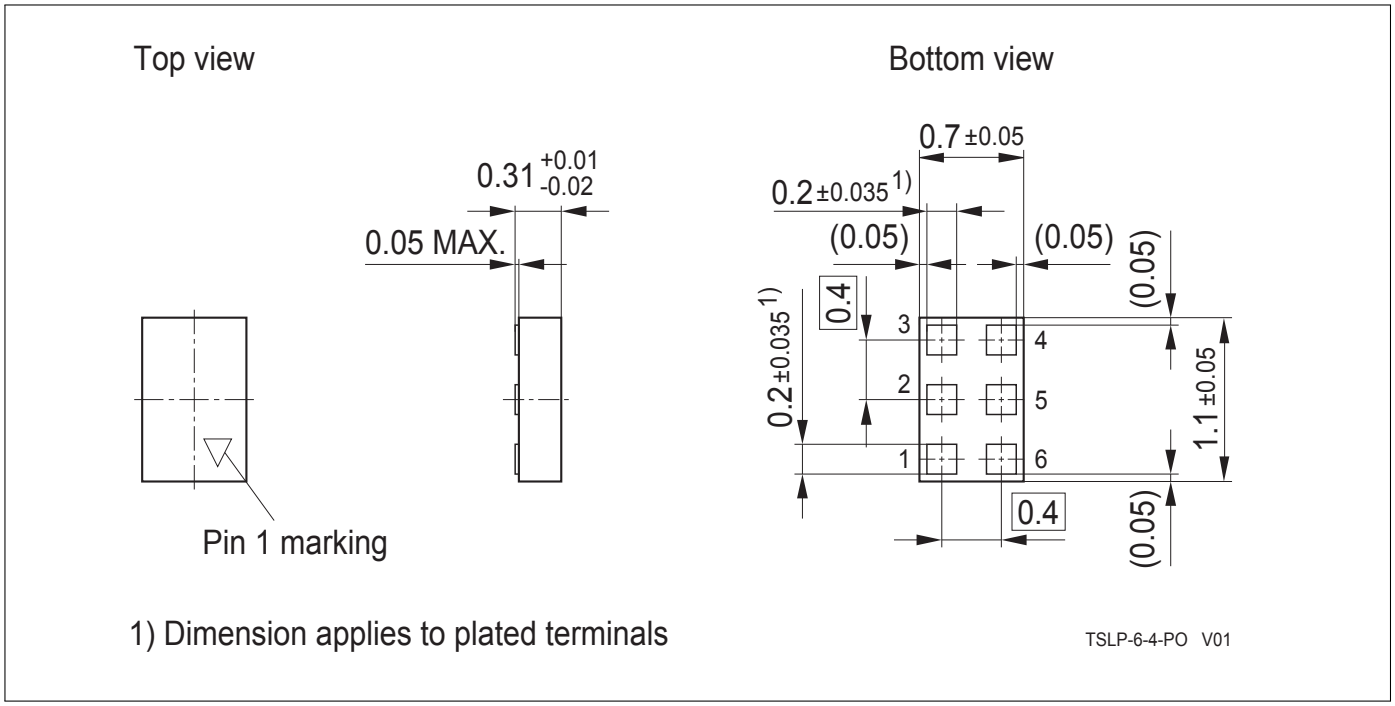


Figure 3: Package Outline

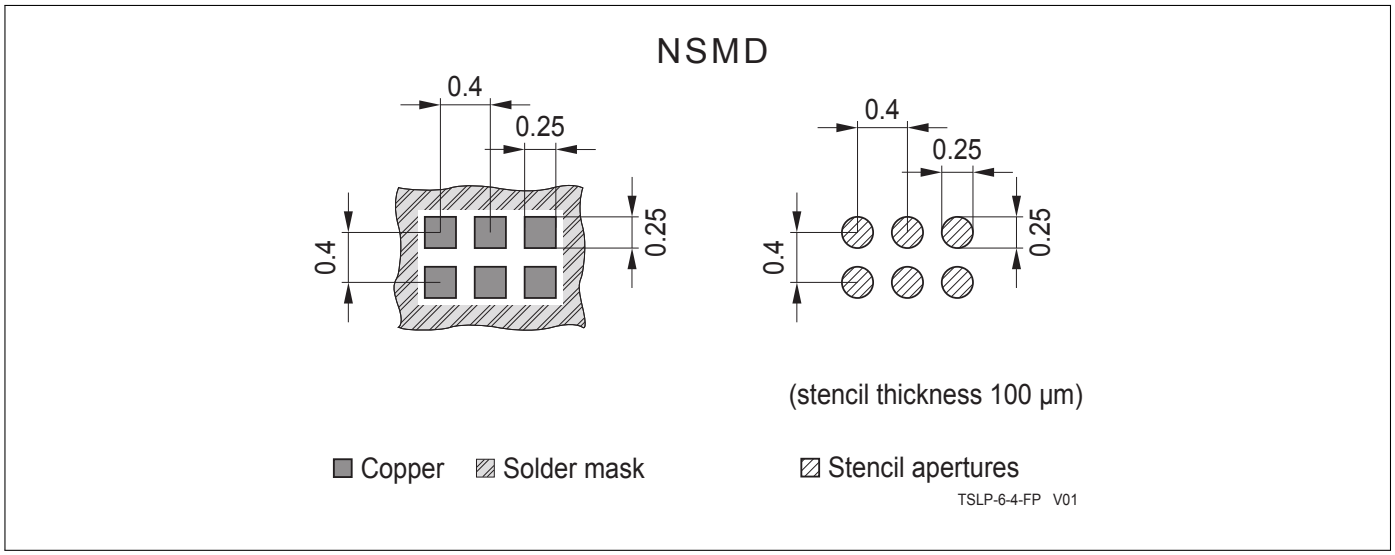


Figure 4: Footprint

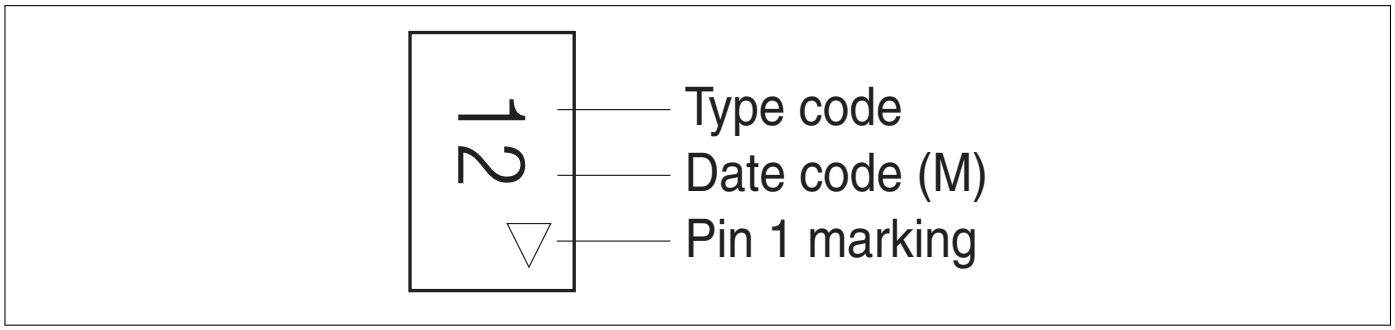


Figure 5: Pin 1 Marking (top view)

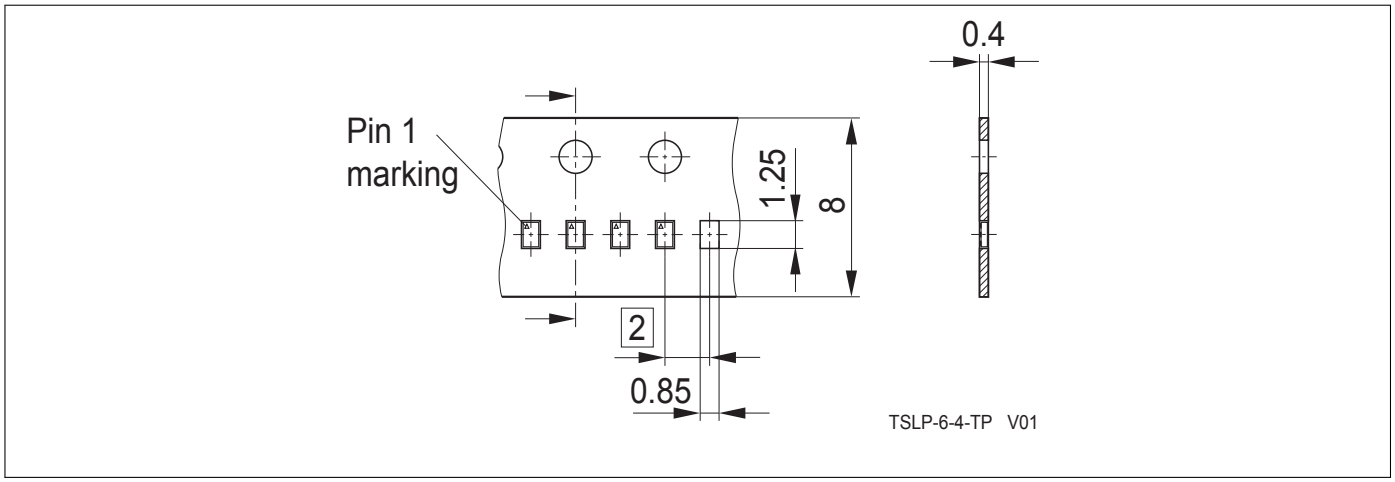


Figure 6: Tape Drawing for TSLP-6-4

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