

## N-channel 100 V, 0.065 $\Omega$ typ., 4 A STripFET™ II Power MOSFET in SO-8 package

Datasheet — production data

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STS4NF100	100 V	0.070 $\Omega$	4 A

- Exceptional dv/dt capability
- 100 % avalanche tested
- Application oriented characterization

### Applications

- Switching applications

### Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

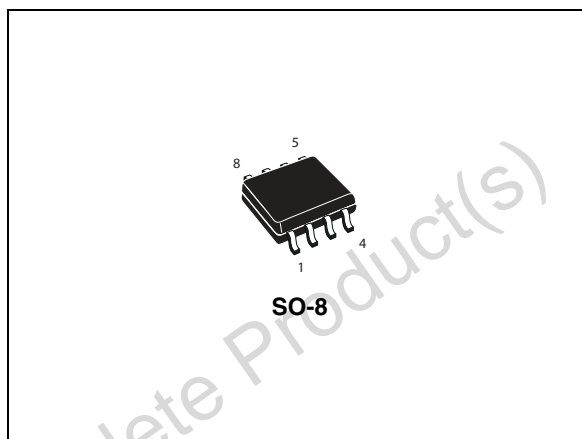


Figure 1. Internal schematic diagram

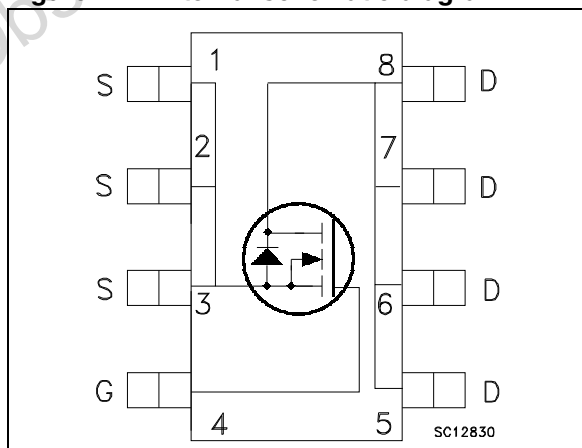


Table 1. Device summary

Order code	Marking	Package	Packaging
STS4NF100	4NF100	SO-8	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate- source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}$	Total dissipation at $T_{amb} = 25^\circ\text{C}$	2.5	W
$T_J$	Max. operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

1. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-a}$	Thermal resistance junction-ambient max <sup>(1)</sup>	50	$^\circ\text{C}/\text{W}$

1. Mounted on FR-4 board (t 10 sec.)

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100 V$ $V_{DS} = 100 V, T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V, I_D = 2 A$		0.065	0.070	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 2 A$	-	10		S
$C_{iss}$	Input capacitance		-	870		pF
$C_{oss}$	Output capacitance	$V_{DS} = 25 V, f = 1 MHz,$ $V_{GS} = 0$	-	125		pF
$C_{rss}$	Reverse transfer capacitance		-	52		pF
$Q_g$	Total gate charge	$V_{DD} = 80 V, I_D = 4 A,$ $V_{GS} = 10 V$	-	30	41	nC
$Q_{gs}$	Gate-source charge		-	6		nC
$Q_{gd}$	Gate-drain charge		-	10		nC

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time rise time	$V_{DD} = 50 V, I_D = 4 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see <a href="#">Figure 14</a> )	-	58 45	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time fall time	$V_{DD} = 50 V, I_D = 4 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see <a href="#">Figure 14</a> )	-	49 17	-	ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4 \text{ A}, V_{GS} = 0$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4 \text{ A}, V_{DD} = 30 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s},$ $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	100		ns
$Q_{rr}$	Reverse recovery charge			375		nC
$I_{RRM}$	Reverse recovery current			7.5		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

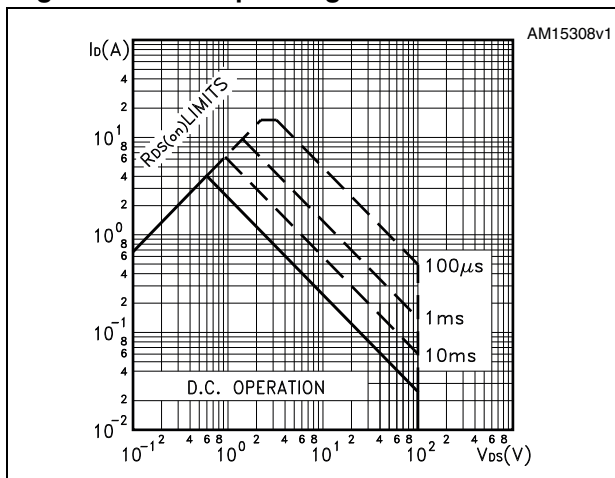


Figure 3. Thermal impedance

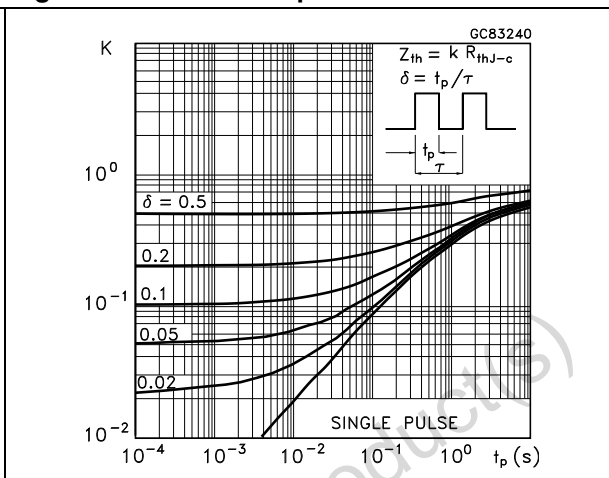


Figure 4. Output characteristics

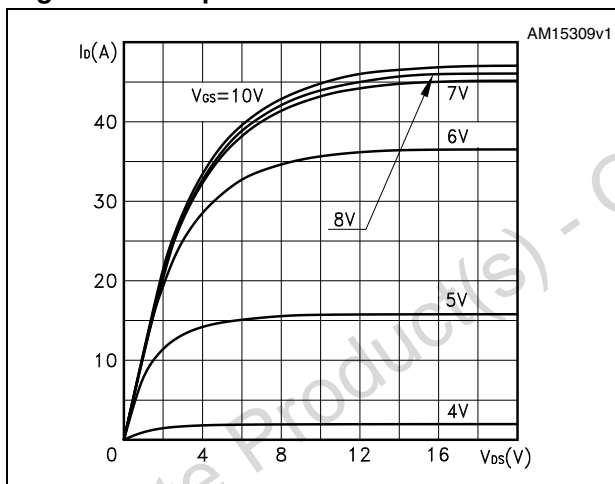


Figure 5. Transfer characteristics

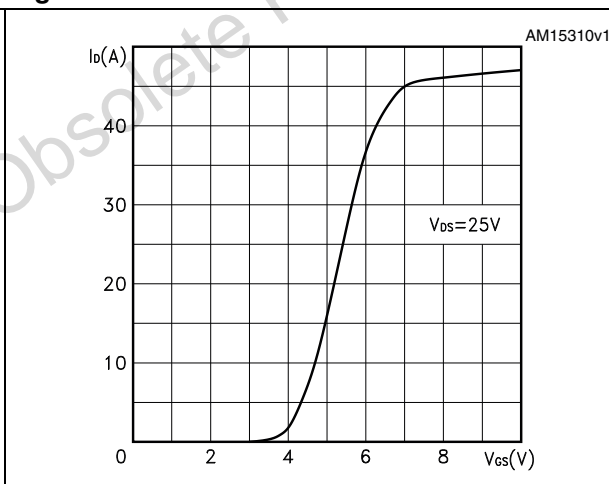


Figure 6. Transconductance

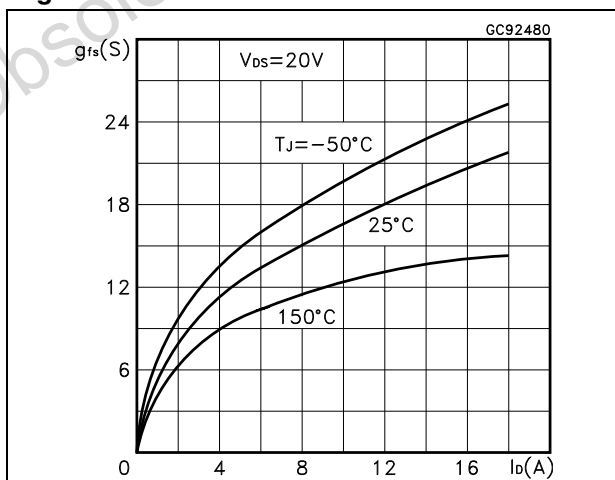


Figure 7. Static drain-source on-resistance

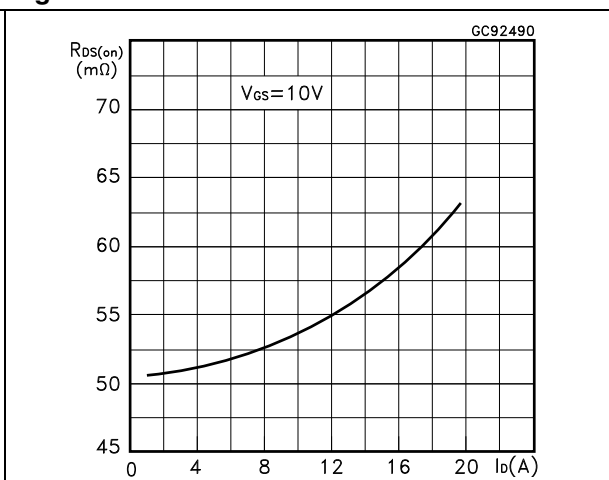


Figure 8. Gate charge vs gate-source voltage    Figure 9. Capacitance variations

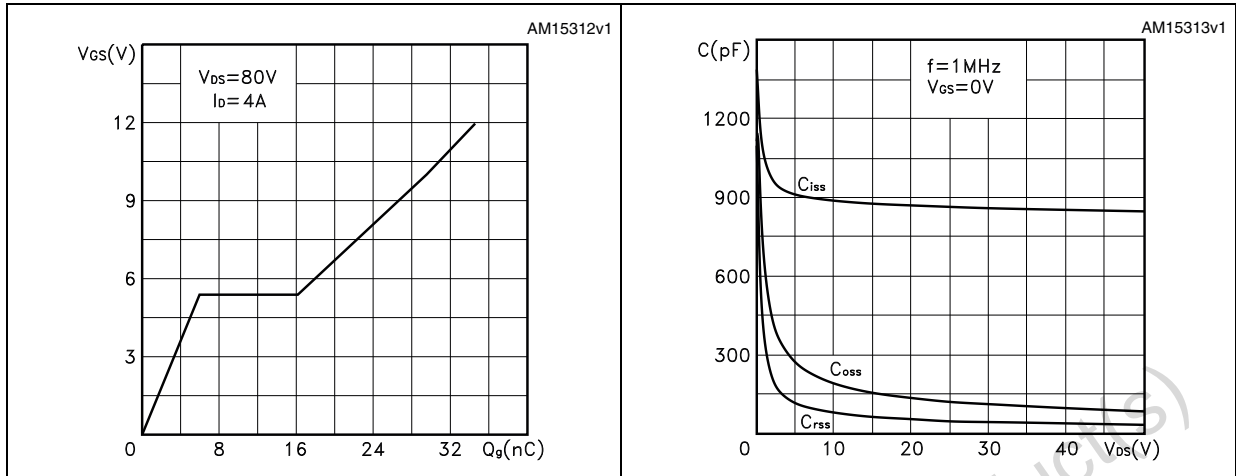


Figure 10. Normalized gate threshold voltage vs temperature    Figure 11. Normalized on-resistance vs temperature

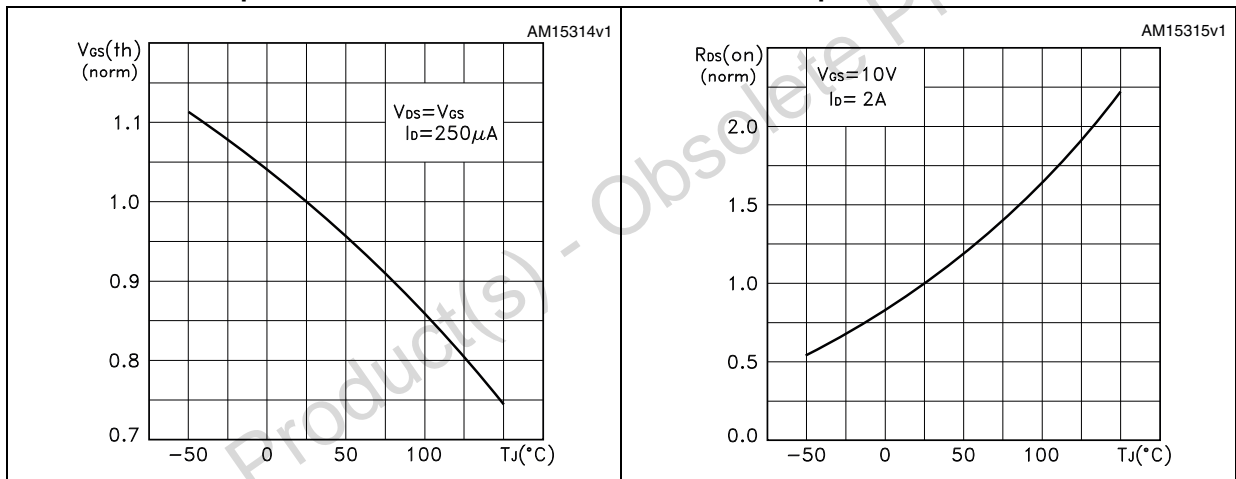
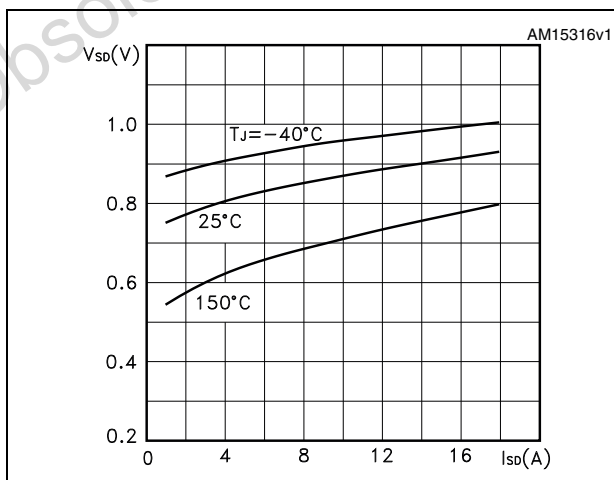


Figure 12. Source-drain diode forward characteristics



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

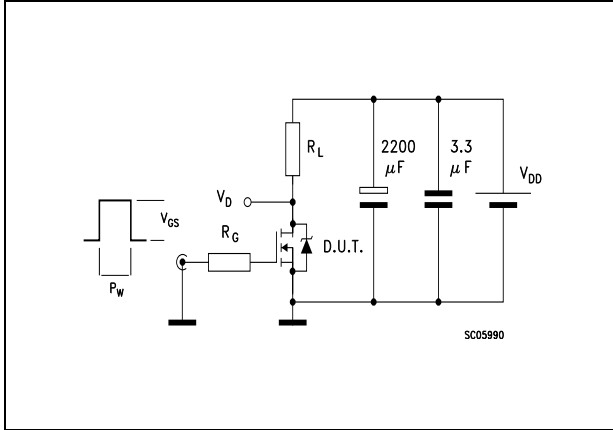


Figure 14. Gate charge test circuit

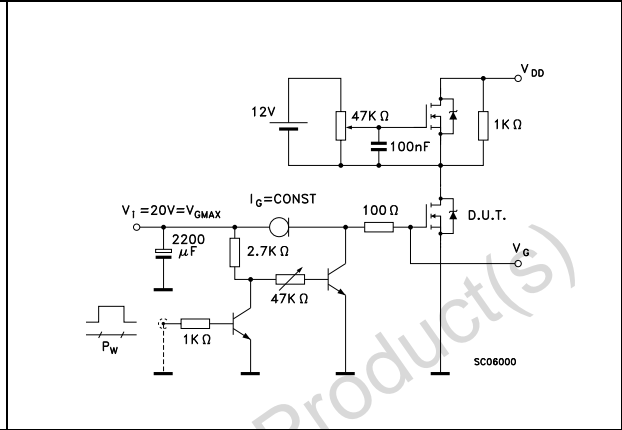


Figure 15. Test circuit for inductive load switching and diode recovery times

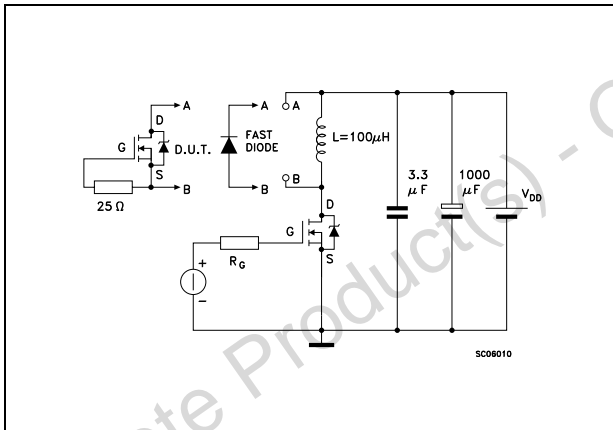


Figure 16. Unclamped Inductive load test circuit

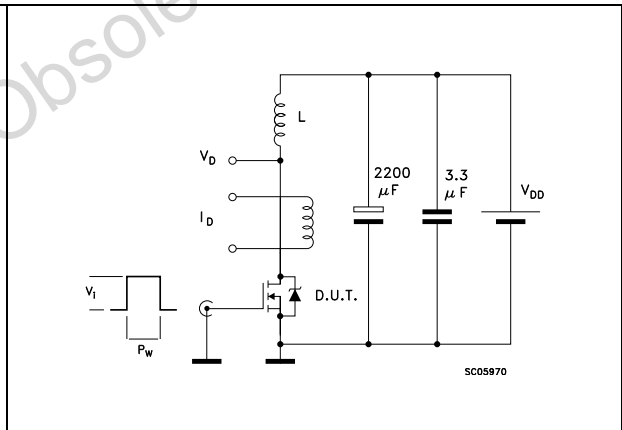


Figure 17. Unclamped inductive waveform

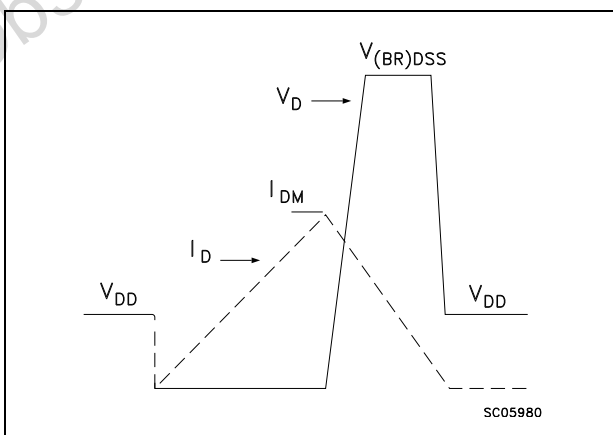
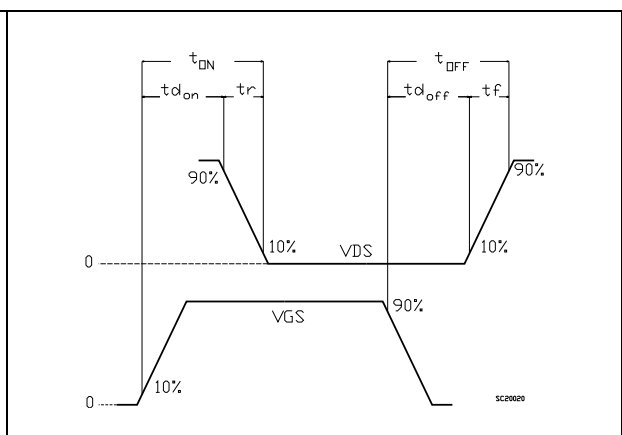


Figure 18. Switching time waveform





## 4 Package mechanical data

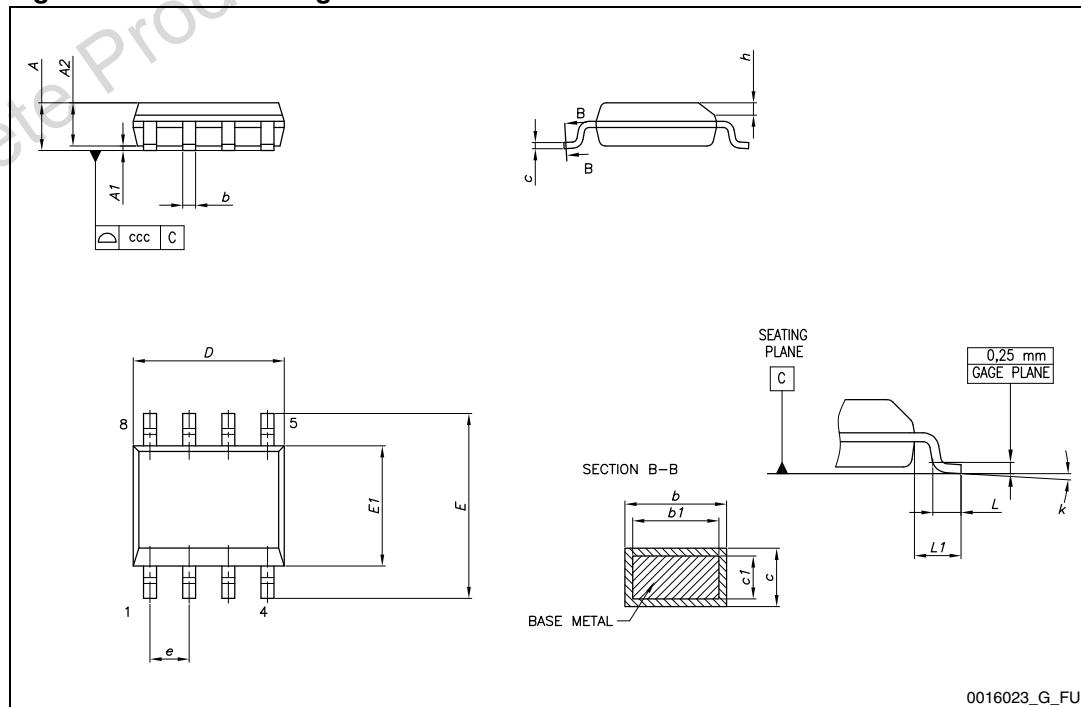
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

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Table 8. SO-8 mechanical data

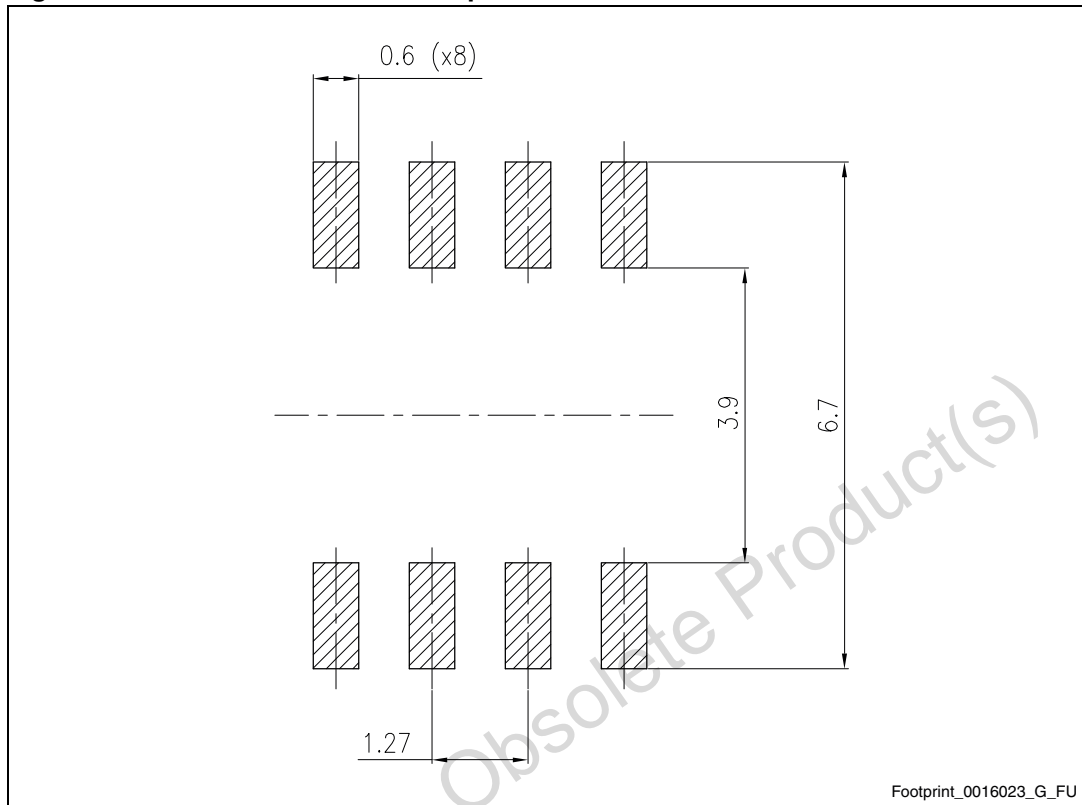
Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 19. SO-8 drawing



0016023\_G\_FU

Figure 20. SO-8 recommended footprint<sup>(a)</sup>



a. All dimensions are in millimeters.

## 5 Revision history

**Table 9. Revision history**

Date	Revision	Changes
11-Sep-2006	1	First release
15-Nov-2006	2	The document has been reformatted
26-Jan-2007	3	Typo mistake on <a href="#">Table 3</a> .
19-Nov-2012	4	Changed: marking in cover page

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