

SN74LVC1G123 Single Retriggerable Monostable Multivibrator With Schmitt-Trigger Inputs

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 8 ns at 3.3 V
- Supports Mixed-Mode Voltage Operation on All Ports
- Supports Down Translation to V_{CC}
- Schmitt-Trigger Circuitry on \bar{A} and B Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop PCs or Notebook PCs
- Digital Radio and Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Attached Storage (NAS)
- Personal Digital Assistant (PDA)
- Server PSU
- Solid-State Drive (SSD): Client and Enterprise
- Video Analytics Servers
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN74LVC1G123 device is a single retriggerable monostable multivibrator designed for 1.65-V to 5.5-V V_{CC} operation.

This monostable multivibrator features output pulse-duration control by three methods. In the first method, the A input is low, and the B input goes high. In the second method, the B input is high, and the A input goes low. In the third method, the A input is low, the B input is high, and the clear (\overline{CLR}) input goes high.

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking CLR low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The A and B inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G123	SSOP (8)	2.95 mm × 2.80 mm
	VSSOP (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

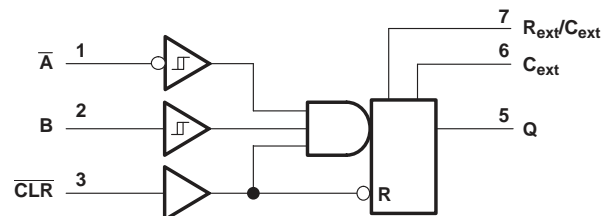


Table of Contents

1	Features	1	8	Detailed Description	11
2	Applications	1	8.1	Overview	11
3	Description	1	8.2	Functional Block Diagram	11
4	Revision History	2	8.3	Feature Description	11
5	Pin Configuration and Functions	3	8.4	Device Functional Modes	12
6	Specifications	4	9	Application and Implementation	13
6.1	Absolute Maximum Ratings	4	9.1	Application Information	13
6.2	ESD Ratings	4	9.2	Typical Application	13
6.3	Recommended Operating Conditions	4	10	Power Supply Recommendations	15
6.4	Thermal Information	5	11	Layout	15
6.5	Electrical Characteristics	5	11.1	Layout Guidelines	15
6.6	Timing Requirements	6	11.2	Layout Example	16
6.7	Switching Characteristics, $C_L = 15$ pF, -40°C to 85°C	7	12	Device and Documentation Support	16
6.8	Switching Characteristics, $C_L = 50$ pF, -40°C to 85°C	7	12.1	Documentation Support	16
6.9	Switching Characteristics, $C_L = 50$ pF, -40°C to 125°C	7	12.2	Community Resources	16
6.10	Operating Characteristics	7	12.3	Trademarks	16
6.11	Typical Characteristics	8	12.4	Electrostatic Discharge Caution	16
7	Parameter Measurement Information	9	12.5	Glossary	16
			13	Mechanical, Packaging, and Orderable Information	16

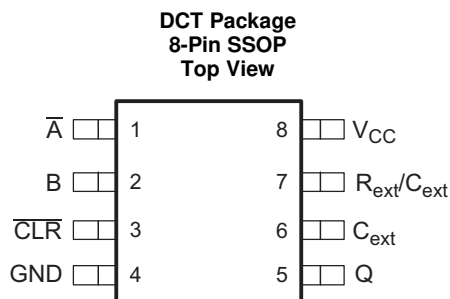
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

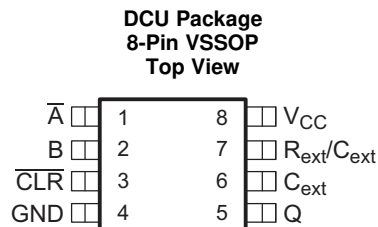
Changes from Revision C (October 2013) to Revision D	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Removed duplicate <i>Timing Requirements</i> table	6

Changes from Revision B (January 2007) to Revision C	Page
• Updated document to new TI data sheet format	1
• Updated <i>Features</i>	1
• Updated operating temperature range.	4
• Added <i>Thermal Information</i> table.	5

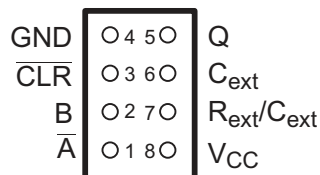
5 Pin Configuration and Functions



See mechanical drawings for dimensions.



**YZP Package
8-Pin DSBGA
Bottom View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
\bar{A}	1	I	Falling edge sensitive input; requires B and $\overline{\text{CLR}}$ to be held high.
B	2	I	Rising edge sensitive input; requires \bar{A} to be held low and $\overline{\text{CLR}}$ to be held high.
$\overline{\text{CLR}}$	3	I	Clear, Active Low; also can operate as rising edge sensitive input if \bar{A} is held low and B is held high.
GND	4	—	Ground
Q	5	O	Output
C_{ext}	6	—	Connects only to the external capacitor
$R_{\text{ext}}/C_{\text{ext}}$	7	—	Connects to the external capacitor and resistor
V_{CC}	8	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	-0.5	6.5	V	
V _I	Input voltage ⁽²⁾	-0.5	6.5	V	
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V	
V _O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	+2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	+1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 3 V to 3.6 V	2	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.8	
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-4	mA
		V _{CC} = 2.3 V	-8	
		V _{CC} = 3 V	-16	
		V _{CC} = 4.5 V	-24	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	8	
		$V_{CC} = 3\text{ V}$	16	
			24	
$V_{CC} = 4.5\text{ V}$	32			
	$R_{ext}^{(2)}$	External timing resistance	$V_{CC} = 2\text{ V}$	5
$V_{CC} \geq 3\text{ V}$			1	
T_A	Operating free-air temperature	-40	125	$^{\circ}\text{C}$

(2) R_{ext}/C_{ext} is an I/O and must not be connected directly to GND or V_{CC} .

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G123			UNIT
	DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	
	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance			$^{\circ}\text{C}/\text{W}$
	220	227	102	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C TO 85°C			-40°C TO 125°C			UNIT	
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX		
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	1.65 V to 5.5 V	$V_{CC} - 0.1$			$V_{CC} - 0.1$			V	
		1.65 V	1.2			1.2				
		2.3 V	1.9			1.9				
		3 V	2.4			2.4				
			2.3			2.3				
		4.5 V	3.8			3.8				
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 5.5 V	0.1			0.1			V	
		1.65 V	0.45			0.45				
		2.3 V	0.3			0.3				
		3 V	0.4			0.4				
			0.55			0.55				
		4.5 V	0.55			0.55				
I_I	$R_{ext}/C_{ext}^{(2)}$ $\overline{A}, B, \overline{CLR}$	B = GND, $\overline{A} = \overline{CLR} = V_{CC}$ $V_I = 5.5\text{ V or GND}$	± 0.25			± 0.25			μA	
			± 1			± 1				
I_{off}	$\overline{A}, B, Q, \overline{CLR}$	V_I or $V_O = 5.5\text{ V}$	0			± 10			μA	
I_{CC}	Quiescent	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			μA	
I_{CC}	Active state	$V_I = V_{CC}$ or GND, $R_{ext}/C_{ext} = 0.5\ V_{CC}$	1.65 V	165			165			μA
			2.3 V	220			220			
			3 V	280			280			
			4.5 V	650			650			
			5.5 V	975			975			
C_I		$V_I = V_{CC}$ or GND	3.3 V			3			pF	

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$.

(2) This test is performed with the terminal in the OFF-state condition.

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8)

PARAMETER		TEST CONDITIONS	-40°C TO 125°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
t _W IN	Pulse duration	$\overline{\text{CLR}}$	8		4		3		2.5		ns
		$\overline{\text{A}}$ or B trigger	8		4		3		2.5		
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ	C _{ext} = 100 pF					5.5	4.5	ns	
			C _{ext} = 100 μF					1.4	1.1	μs	
		R _{ext} = 5 kΩ	C _{ext} = 100 pF	75		45					ns
			C _{ext} = 100 μF	1.8		1.4					μs

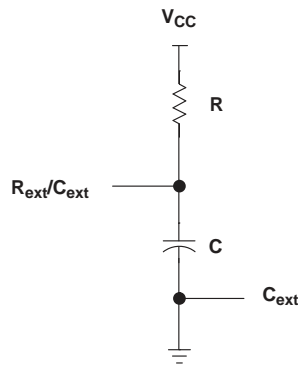


Figure 1. Required Timing Circuit

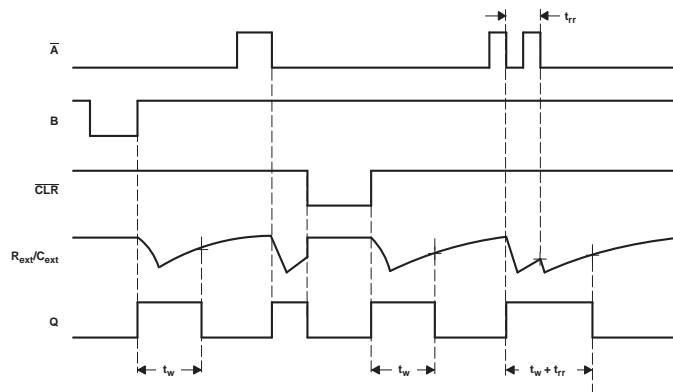


Figure 2. Input/Output Timing Diagram

6.7 Switching Characteristics, $C_L = 15\text{ pF}$, -40°C to 85°C

over recommended operating free-air temperature range, $C_L = 15\text{ pF}$ (unless otherwise noted) (see Figure 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C								UNIT	
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN		MAX
t_{pd}	\bar{A} or B	Q	7	18.5	52	4	17	3	11.5	2	7.6	ns
	$\overline{\text{CLR}}$		5	12.4	34	3	11.5	2	8	1.5	5.5	
	$\overline{\text{CLR}}$ trigger		7	17.4	54	4	15.5	3	10.5	2	7	

6.8 Switching Characteristics, $C_L = 50\text{ pF}$, -40°C to 85°C

over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	-40°C TO 85°C								UNIT	
				$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
				MIN	TYP ⁽¹⁾	MAX	MIN	MAX	MIN	MAX	MIN		MAX
t_{pd}	\bar{A} or B	Q		6	18.6	57	3	18.5	2	12.5	1.5	8.2	ns
	$\overline{\text{CLR}}$		4	11.6	36.5	2	12.5	1.5	8.6	1.5	6		
	$\overline{\text{CLR}}$ trigger		5	17.3	59	2.5	17	2	11.5	1.5	7.5		
$t_{wOUT}^{(2)}$		Q	$C_{ext} = 28\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$		225	600	190	220	170	200	150	180	ns
			$C_{ext} = 0.01\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$		100	110	100	110	100	110	100	110	μs
			$C_{ext} = 0.1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$		1	1.1	1	1.1	1	1.1	1	1.1	ms

(1) $T_A = 25^\circ\text{C}$

(2) t_w = Duration of pulse at Q output

6.9 Switching Characteristics, $C_L = 50\text{ pF}$, -40°C to 125°C

over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	-40°C TO 125°C								UNIT	
				$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
				MIN	TYP ⁽¹⁾	MAX	MIN	MAX	MIN	MAX	MIN		MAX
t_{pd}	\bar{A} or B	Q		6		58	3	19.5	2	13.2	1.5	8.7	ns
	$\overline{\text{CLR}}$		4		37	2	13.5	1.5	9.2	1.5	6.5		
	$\overline{\text{CLR}}$ trigger		5		60	2.5	18	2	12	1.5	8		
$t_{wOUT}^{(2)}$		Q	$C_{ext} = 28\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$		225	600	190	220	170	200	150	180	ns
			$C_{ext} = 0.01\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$		100	110	100	110	100	110	100	110	μs
			$C_{ext} = 0.1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$		1	1.1	1	1.1	1	1.1	1	1.1	ms

(1) $T_A = 25^\circ\text{C}$

(2) t_w = Duration of pulse at Q output

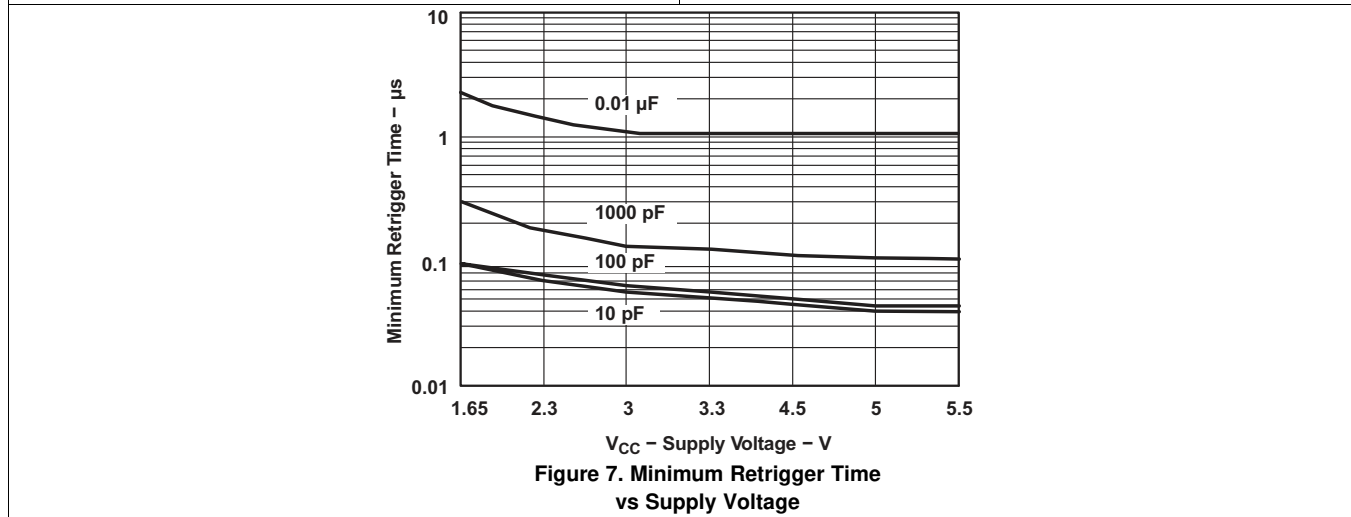
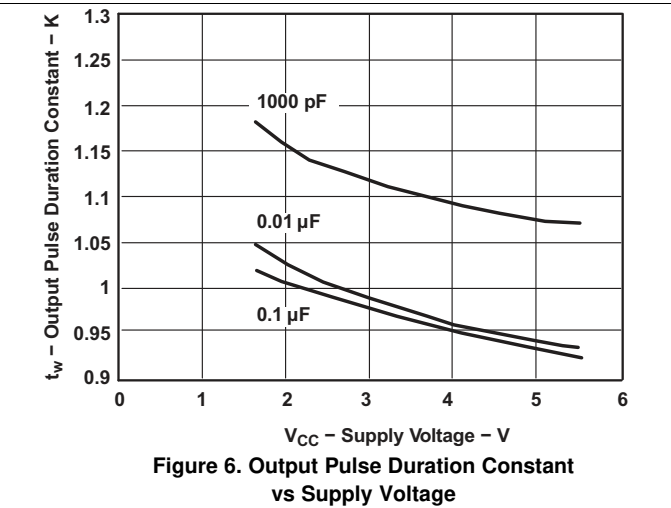
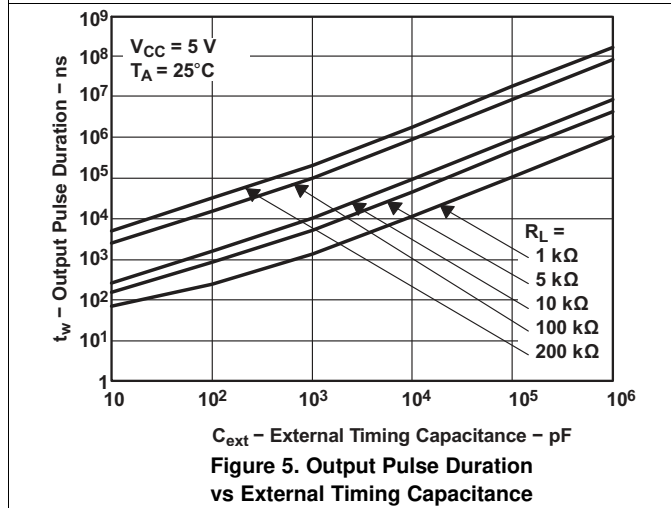
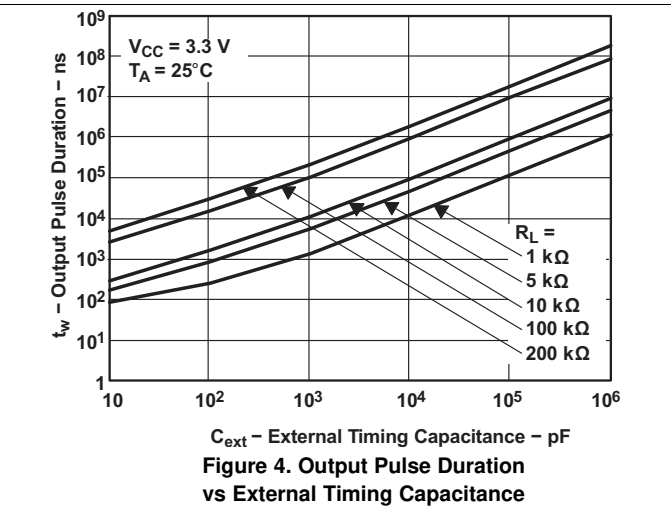
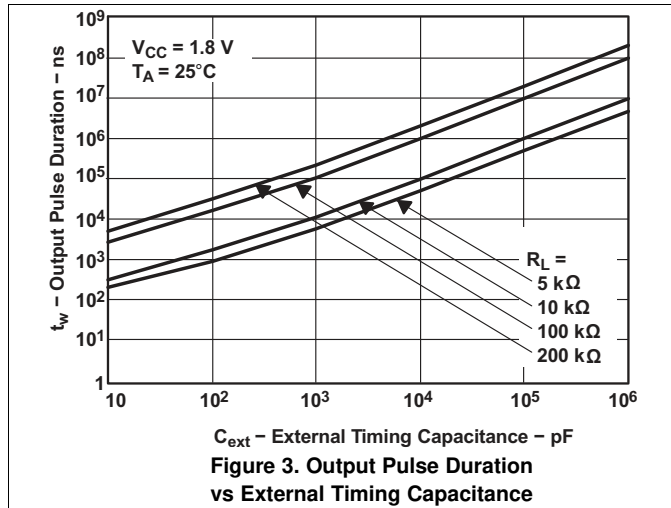
6.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$

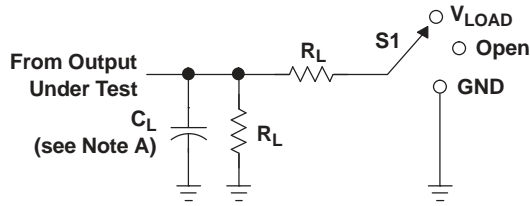
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT	
		TYP	TYP	TYP	TYP		
C_{pd} Power dissipation capacitance	$\bar{A} = \text{low}$, $B = \text{high}$, $\overline{\text{CLR}} = 10\text{ MHz}$	$R_{ext} = 1\text{ k}\Omega$, No C_{ext}			35	37	pF
		$R_{ext} = 5\text{ k}\Omega$, No C_{ext}	41	40			

6.11 Typical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)



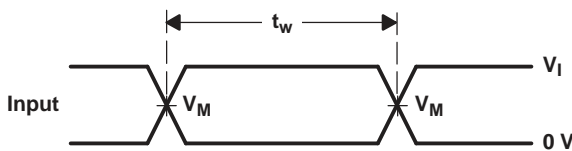
7 Parameter Measurement Information



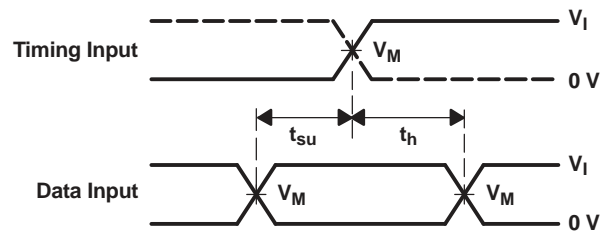
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

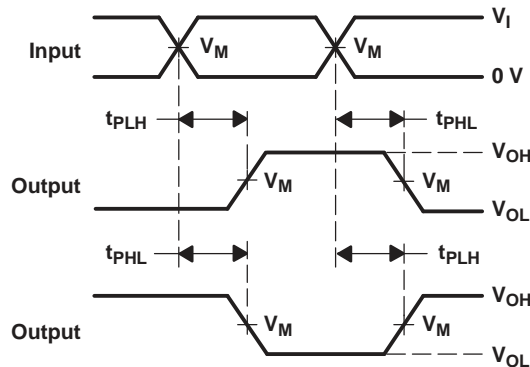
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



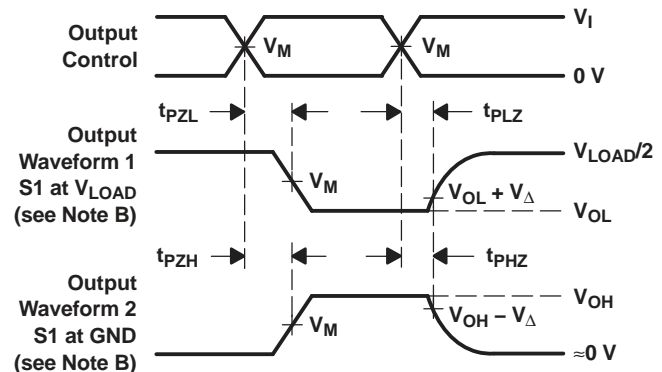
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



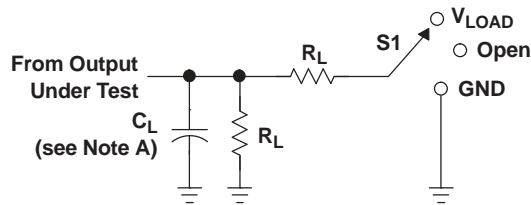
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

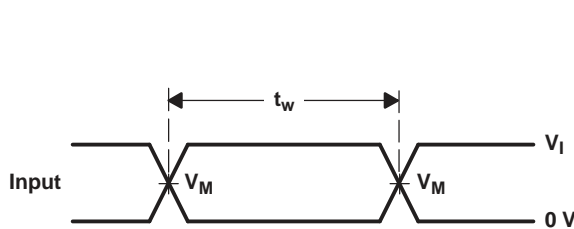
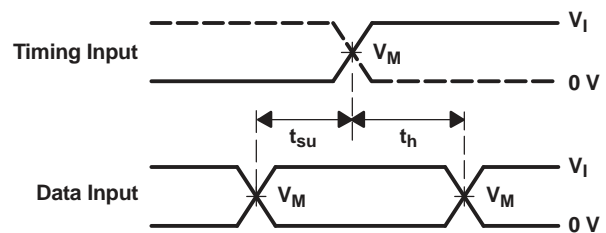
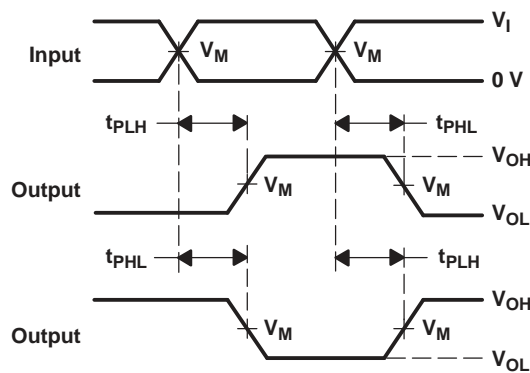
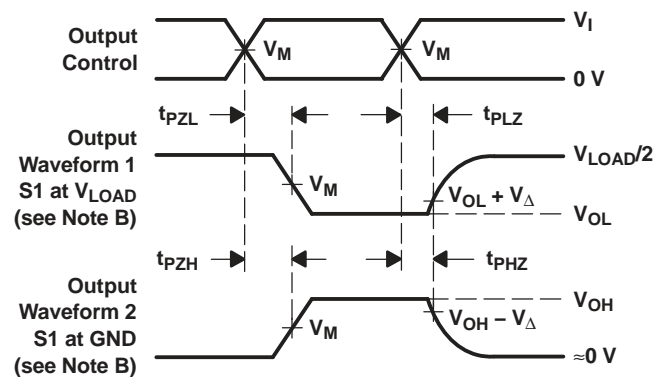
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 8. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 9. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G123 device is a single retriggerable monostable multivibrator designed for 1.65-V to 5.5-V V_{CC} operation.

This monostable multivibrator features output pulse-duration control by three methods. In the first method, the \overline{A} input is low, and the B input goes high. In the second method, the B input is high, and the \overline{A} input goes low. In the third method, the \overline{A} input is low, the B input is high, and the clear (\overline{CLR}) input goes high.

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking \overline{CLR} low.

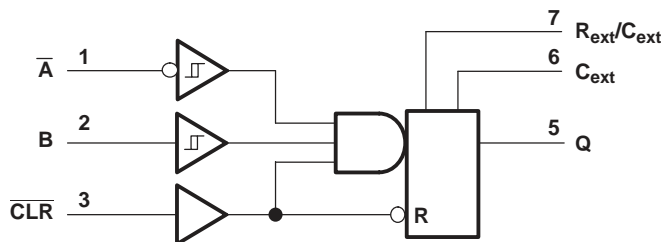
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \overline{A} and B inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active (\overline{A}) or high-level-active (B) input. Pulse duration can be reduced by taking \overline{CLR} low. \overline{CLR} can be used to override \overline{A} or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

The SN74LVC1G123 device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

8.2 Functional Block Diagram



8.3 Feature Description

This part is available in the Texas Instruments NanoFree™ package. It supports 5-V V_{CC} operation and accepts inputs up to 5.5 V. The max t_{pd} is 8 ns at 3.3 V. It supports mixed-mode voltage operation on all ports.

Down translation can be achieved to V_{CC} from up to 5.5 V.

Schmitt-trigger circuitry on \overline{A} and B inputs allows for slow input transition rates. The device can be edge triggered from active-high or active-low gated logic inputs. It can support up to 100% duty cycle from retriggering.

Clear can be used to terminate the output pulse early.

Glitch-free power-up reset is on all outputs.




I_{off} supports live insertion, partial-power-down mode, and back-drive protection.

Latch-up performance exceeds 100 mA per JESD 78, Class II.

8.4 Device Functional Modes

Table 1 lists the functional modes for the SN74LVC1G123.

Table 1. Function Table

INPUTS			OUTPUTS Q
CLR	\bar{A}	B	
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	
H	↓	H	
↑	L	H	

- (1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G123 can be used for many applications. The application shown here is a switch debounce circuit. Many switches produce multiple triggers when pressed, and the debounce circuit turns the many triggers into one. This circuit takes advantage of the retrigger capability of the SN74LVC1G123 in that the output pulse length only has to be longer than the longest individual bounce (typically less than 1 ms).

9.2 Typical Application

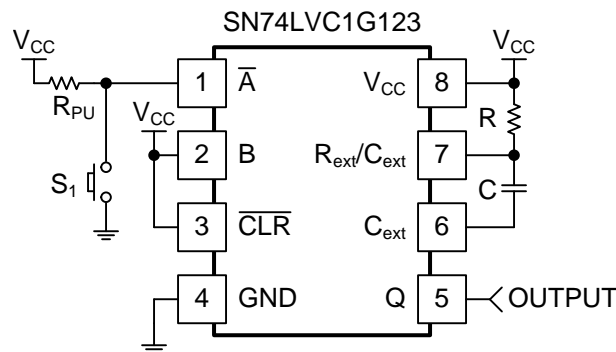


Figure 10. Typical Application of the SN74LVC1G123

9.2.1 Design Requirements

- Recommended Input Conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
 - Inputs and outputs are overvoltage tolerant, allowing them to go as high as 4.6 V at any valid V_{CC} .
- Recommended Output Conditions:
 - Load current should not exceed values listed in [Recommended Operating Conditions](#).

9.2.2 Detailed Design Procedure

The values for V_{CC} , R_{PU} , R , and C must be selected for proper operation.

V_{CC} is selected at 1.8 V. This value is usually driven by the logic voltage of the system, but is arbitrary in this case.

R_{PU} is selected at 10 k Ω .

R and C are selected via the plots in [Application Curves](#) and are based on the time desired for the output pulse. In this case, the output pulse will be 1 ms. Since the supply voltage has been selected at 1.8 V, [Figure 11](#) is used to determine the R and C values required. First convert the desired pulse width (t_w), 1 ms, to ns. This yields 10^6 ns. Next follow that line across to see which R and C values intersect it.

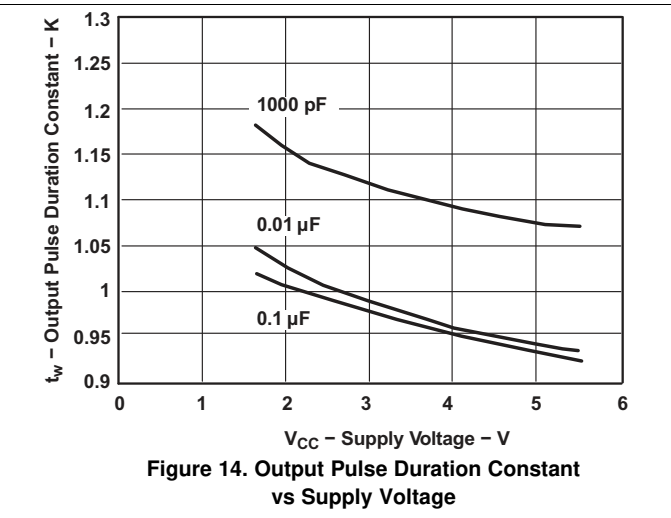
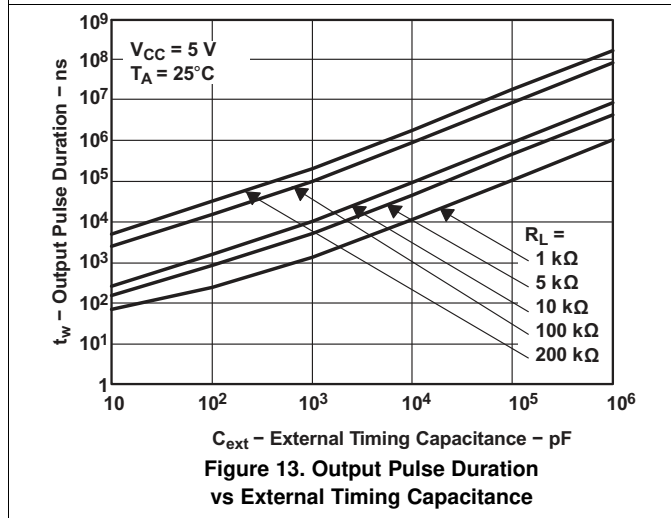
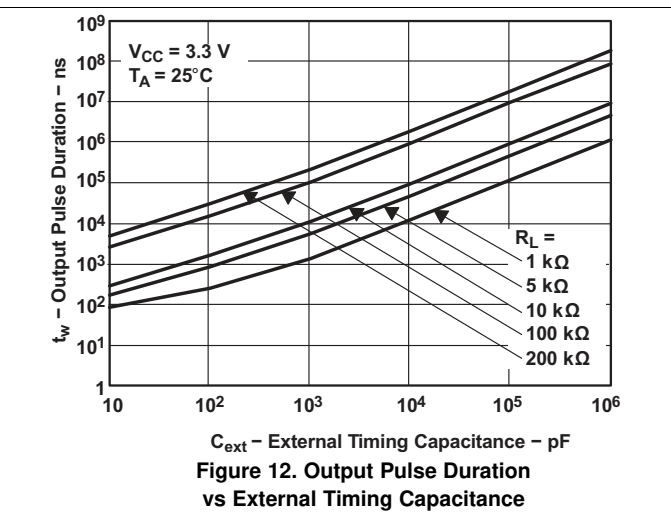
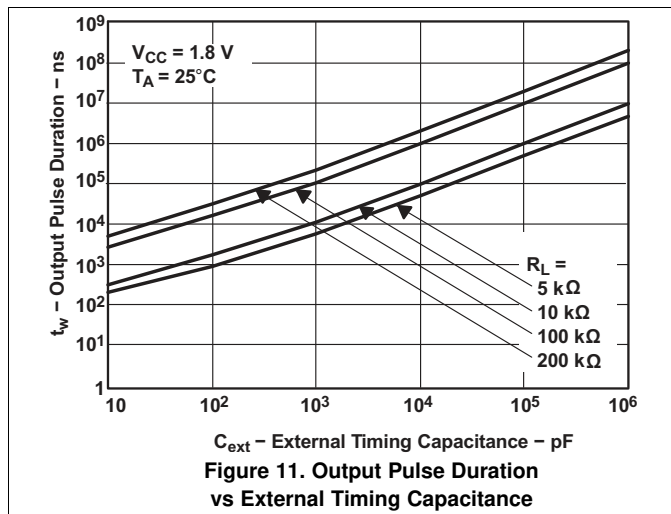
R is selected at 10 k Ω because that line intersects nicely with 10^6 ns and 10^5 pF, making the selection of C at 0.1 μ F easy.

Table 2. Application Specific Values

PARAMETER	VALUE
V_{CC}	1.8 V
R_{PU}	10 k Ω
t_w	1 ms
R (R_{ext})	10 k Ω
C (C_{ext})	0.1 μ F

In addition to the shown components, a 0.1- μ F decoupling capacitor from V_{CC} to ground should be placed as close as possible to the device.

9.2.3 Application Curves



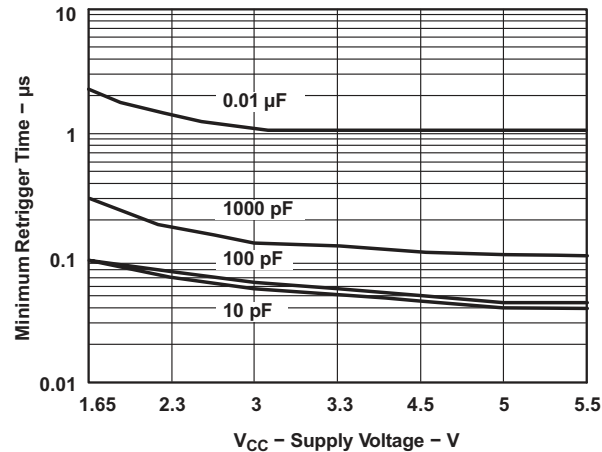


Figure 15. Minimum Retrigger Time vs Supply Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μF or 0.022- μF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 16](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

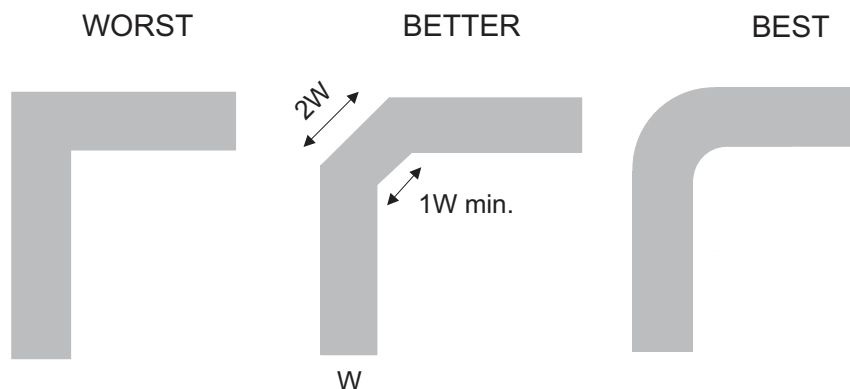


Figure 16. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G123DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)	Samples
74LVC1G123DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)	Samples
74LVC1G123DCTTE4	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)	Samples
74LVC1G123DCTTG4	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)	Samples
74LVC1G123DCURE4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R	Samples
74LVC1G123DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R	Samples
74LVC1G123DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R	Samples
SN74LVC1G123DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)	Samples
SN74LVC1G123DCTT	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)	Samples
SN74LVC1G123DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(22FT, C23Q, C23R)	Samples
SN74LVC1G123DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C23J, C23Q, C23R)	Samples
SN74LVC1G123YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(D87, D8N)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

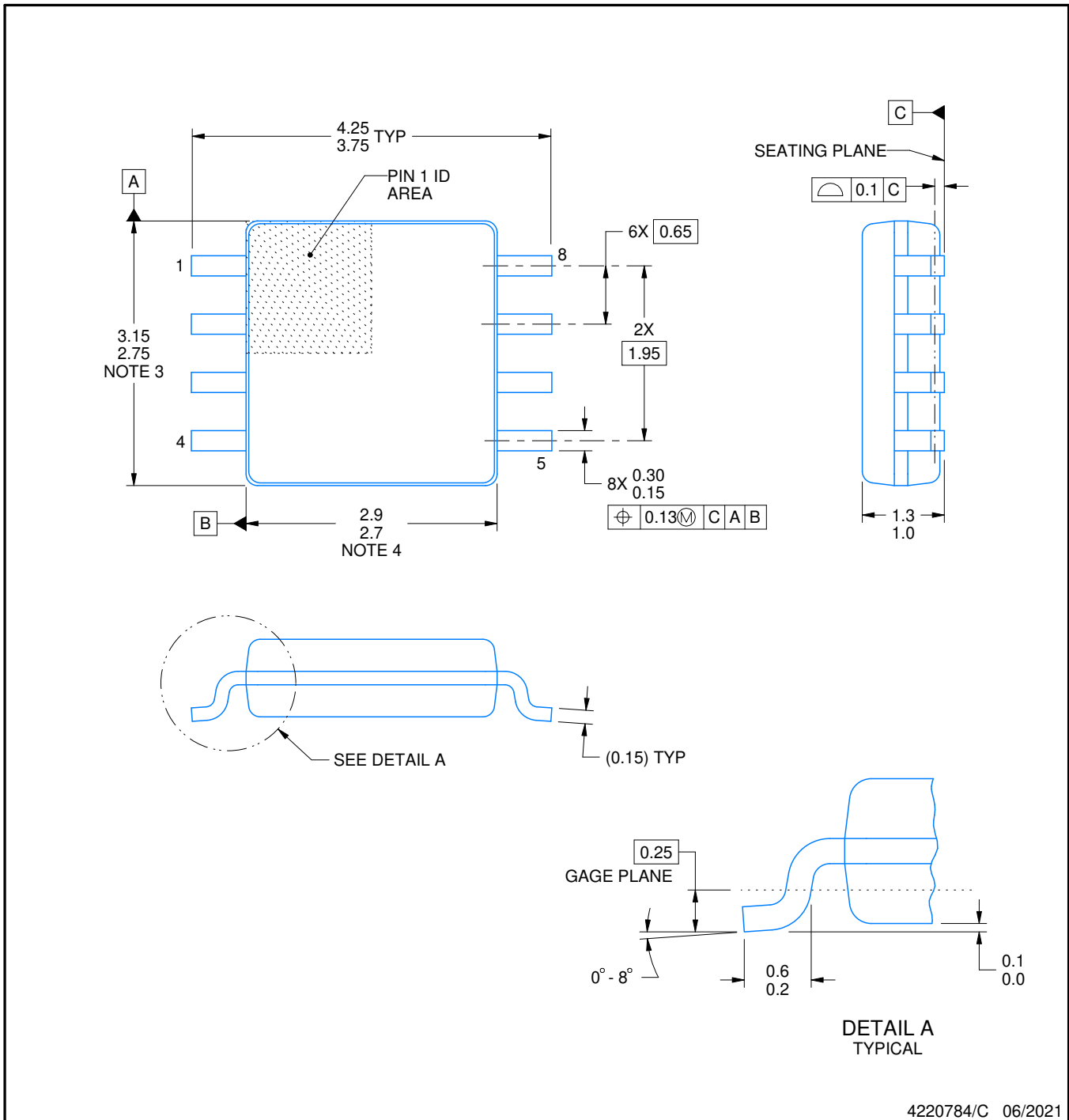

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G123DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
74LVC1G123DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1G123DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G123DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
74LVC1G123DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G123DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC1G123DCTT	SM8	DCT	8	250	182.0	182.0	20.0
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1G123YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



NOTES:

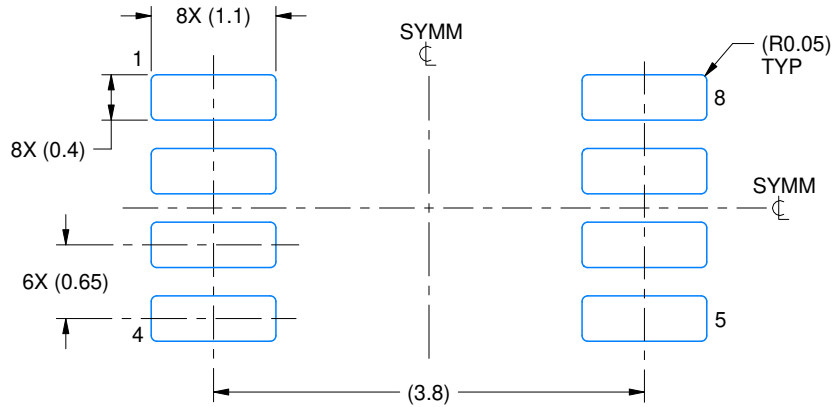
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

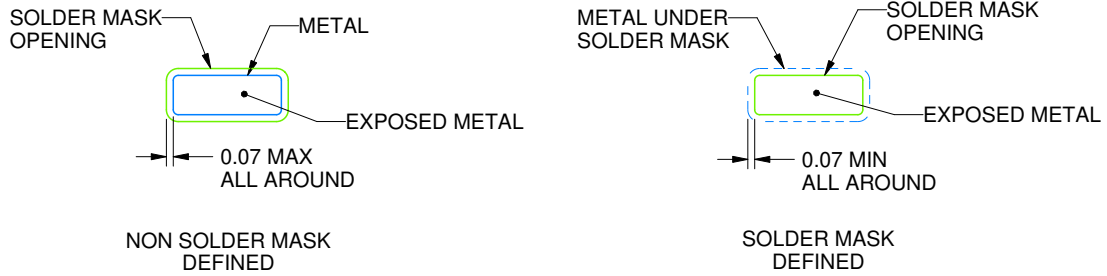
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

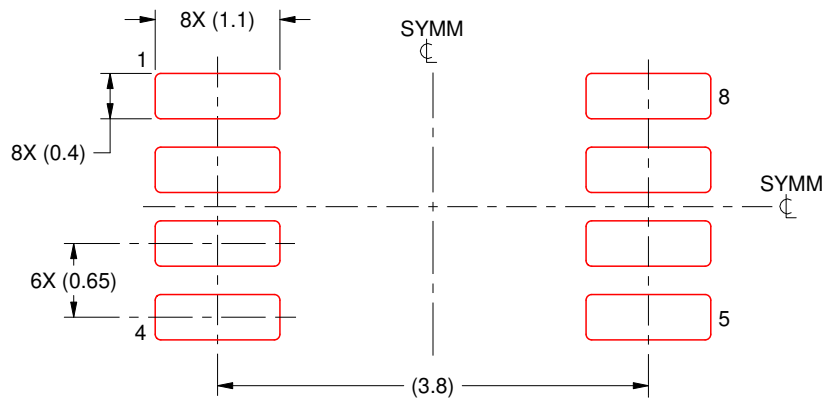
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

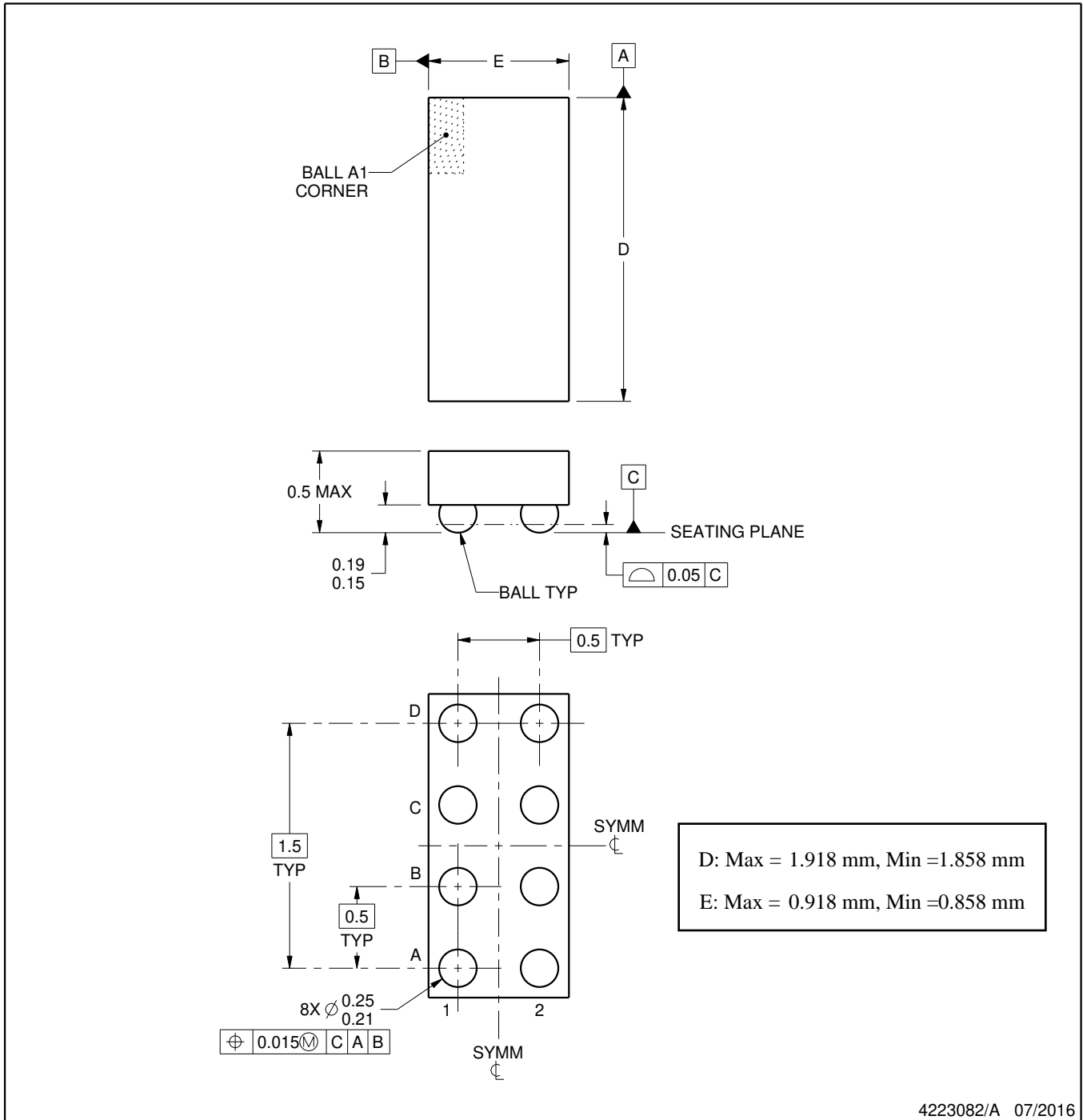
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

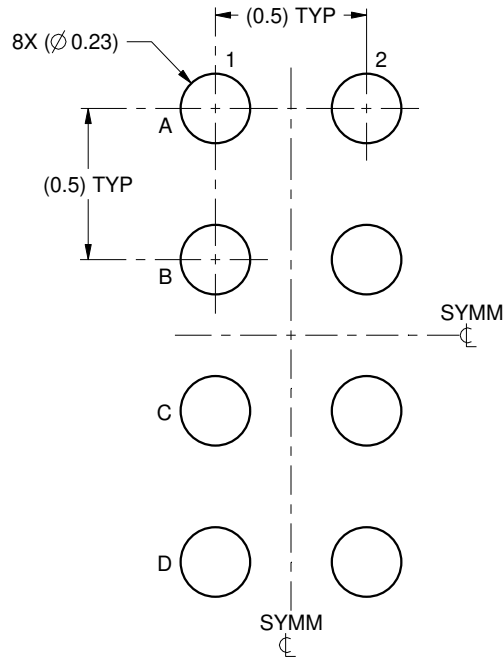
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

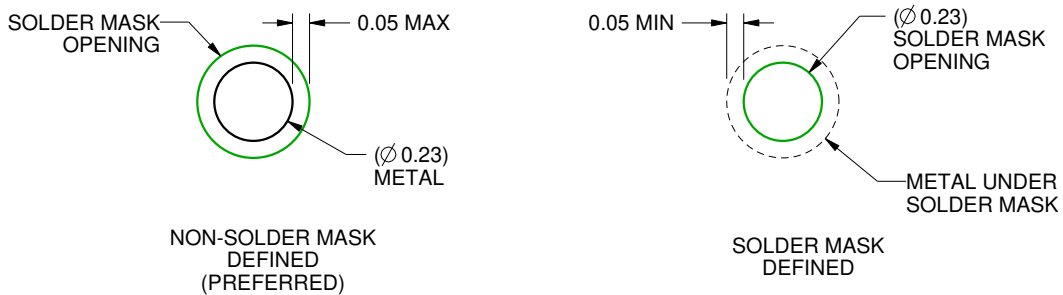
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

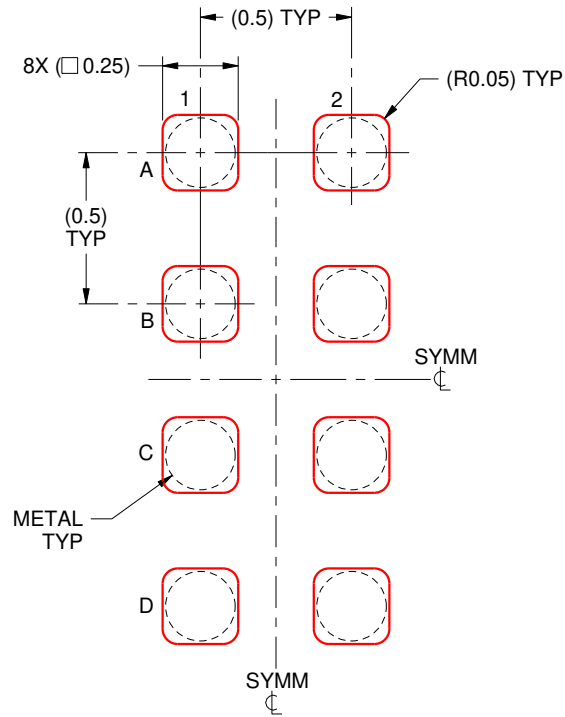
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

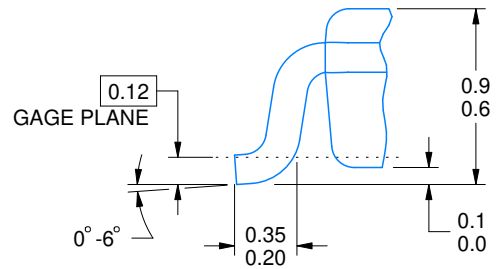
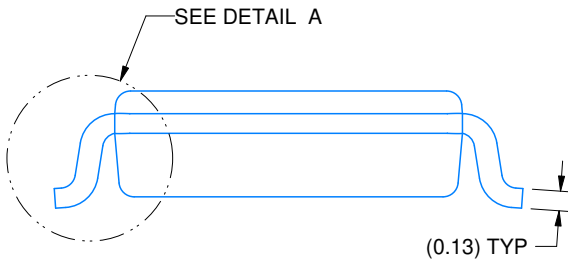
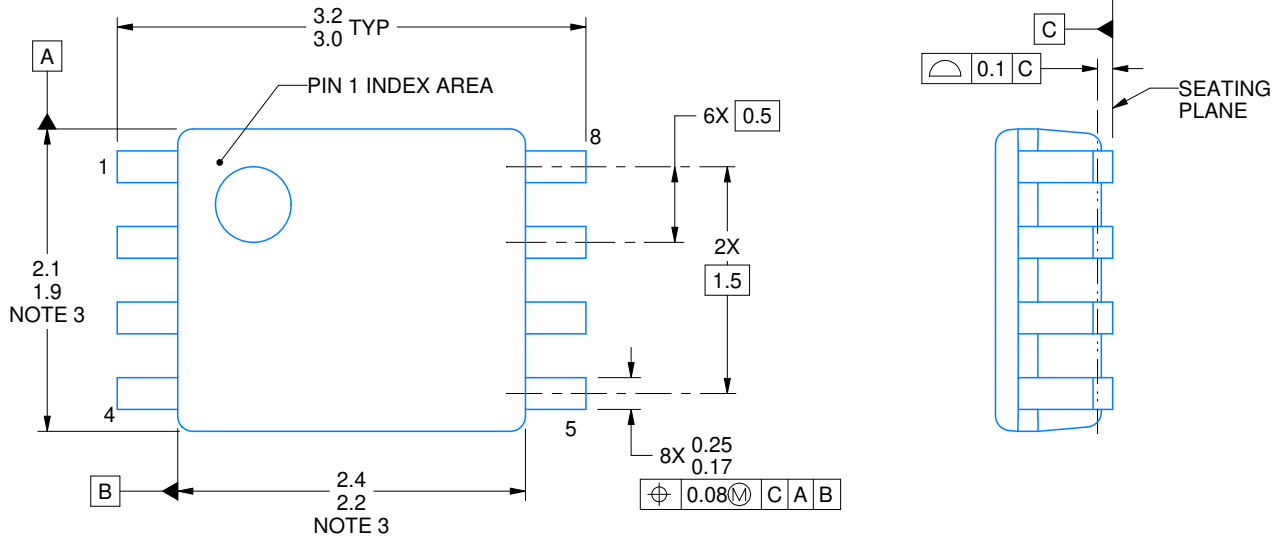


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4225266/A 09/2014

NOTES:

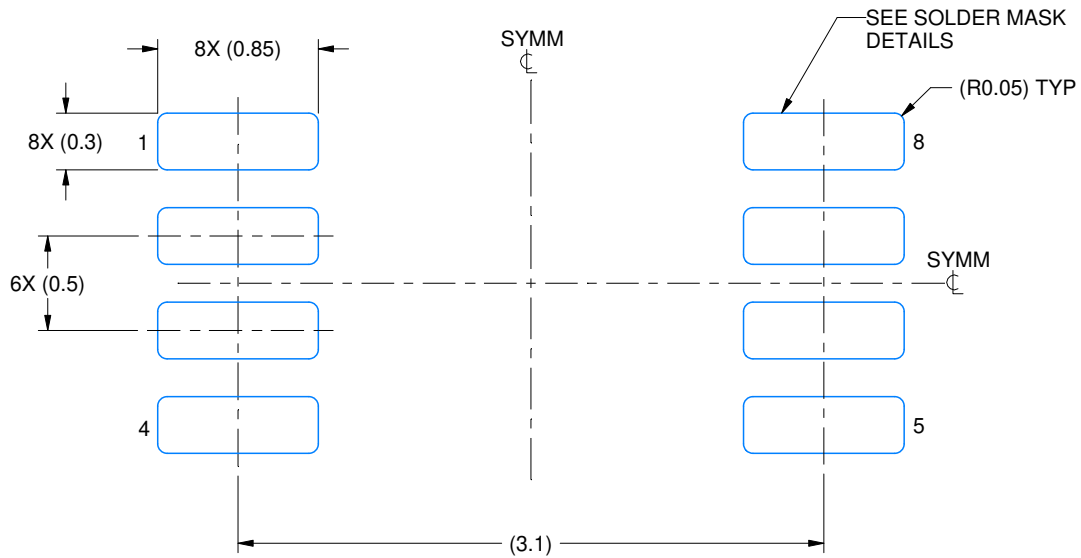
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

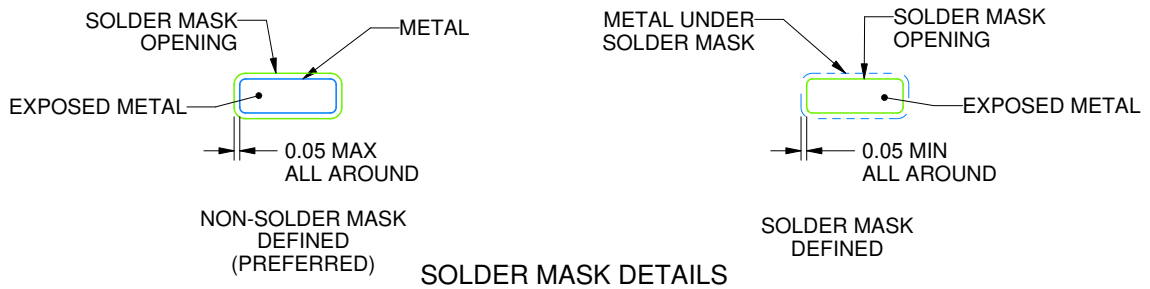
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

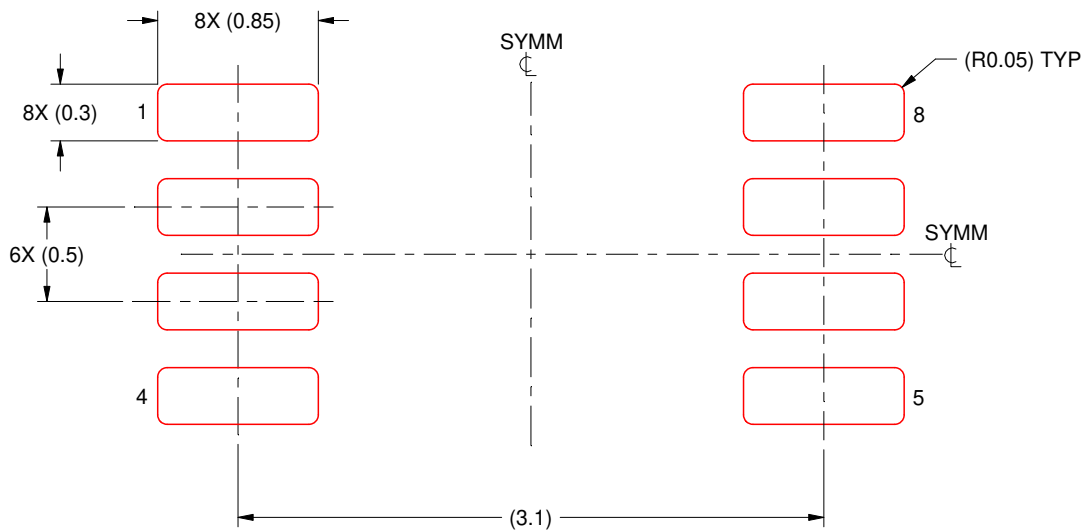
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated