User's Guide

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TPS735xxEVM-276

This user's guide describes the characteristics, operation, and use of the TPS735xxEVM-276 evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS735xx a low dropout (LDO) linear regulator that is capable of 500 mA at both fixed and adjustable output voltage levels. This user's guide includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials, and printed-circuit board layout drawings for the EVM.

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1 Introduction

The TPS735xxEVM-276 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS735xx family. The TPS735xx is a 500-mA, low quiescent current, ultra-low noise, high PSRR, fast start-up LDO linear regulator with excellent line and load transient response.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS735xxEVM.

2.1 Input/Output Connector Descriptions

2.1.1 J1 –VIN

This is the positive input supply voltage. The leads to the input supply must be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance must be added between J1 and J2 if the supply leads are greater than six inches. An additional 47-µF or greater capacitor improves the transient response of the TPS735xx and helps to reduce ringing on the input when long supply wires are used.

2.1.2 J2 –GND

This is the return connection for the input power supply of the regulator.

2.1.3 J3 –VOUT

This is the positive connection from the output. Connect this pin to the positive input of the load.

2.1.4 J4 –GND

This is the return connection for the output.

2.1.5 J5 –ENABLE

This jumper enables or disables the regulator. Connecting the shorting jumper between pin 1 and pin 2 (ENABLE and EN) enables the converter. Connecting the shorting jumper between pin 2 and pin 3 (DISABLE and GND) disables the converter. Never leave this pin floating.

2.2 Soldering Guidelines

Any soldering work on the TPS753xxEVM must be performed using a hot air system to avoid damaging the integrated circuit (IC). A hot air system must be used when soldering or de-soldering any external components such as the feedback network as well as the IC. A hot air system heats all of the traces on the board equally, which equalizes the thermal expansion of the traces on the board and thus reduces stress. Heating only one trace, such as with a soldering iron, allows one trace to expand more than the others and to cause shear stress on the pins of the QFN package. The shear stress on a single pin can be enough to break the pin of the IC, thus causing an IC failure.

3 Operation

This section provides information about the operation of the TPS735xxEVM.

3.1 Operation

Connect the positive input power supply to J1. Connect the input power return (ground) to J2. The TPS735xxEVM has an absolute maximum input voltage of 7 V. The recommended maximum operating voltage is 6.5 V. The actual highest input voltage may be less than 6.5 V due to thermal conditions. See the Thermal Considerations section of this manual to determine if the highest input voltage.

Connect the desired load between J3 (positive lead) and J4 (negative lead). Configure jumper JP1 as required. The function of JP1 is described in the Setup section (2.1.5) of this manual.

4 Thermal Guidelines

This section provides guidelines for the thermal management of the TPS735xxEVM-276 board.

4.1 Thermal Considerations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. To better help you design the TPS735xx family into your application, use the following formula to approximate the maximum power dissipation at a particular ambient temperature:

$$T_J = T_A + P_d \times \theta_{JA} \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, P_d is the power dissipation in the IC, and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius.

The thermal resistance from junction to ambient for the TPS735xxEVM has a typically value of 27.5°C/W. The recommended maximum operating junction temperature specified in the data sheet for the TPS735xx family is 125°C. With these two pieces of information, the maximum power dissipation can be found by using Equation 1.

Example Calculation:

For example, what is the maximum input voltage that can be applied to a TPS73525 (fixed 2.5-V output) if the ambient temperature is 85°C and the full 500 mA of load current is required?

$$\text{Given: } T_J = 125°C,\ T_A = 85°C,\ \theta_{JA} = 27.5°C/W \tag{2}$$

Using Equation 1, substitute in the preceding given values and find that the maximum power dissipation for the part is P_d = 1.45 W.

$$125°C = 85°C + P_d\ (27.5°C/W) \tag{3}$$

This means that the total power dissipation of the TPS73525 must be less than 1.45 W. Now, the input voltage can be calculated.

$$P_d = (V_{in} - V_{out}) \times I_{out} = (Vin - 2.5V) \times 0.5\ A = 1.45\ W \tag{4}$$

So, the maximum input voltage needs to be 5.4 V or less in order to maintain a safe junction temperature.

Similar analysis can be performed to determine the maximum ambient temperature over a range of operation. The maximum recommended input voltage for the TPS735xx is 6.5 V. You can calculate the highest ambient temperature allowed and still provide full output current. The answer depends on the output voltage.

Output Voltage (V)	Maximum Ambient Temperature °C
1.8	60.3
2.5	70
3.3	81

5 Board Layout

This section provides the TPS735xxEVM-276 board layout and illustrations

5.1 Layout

When laying out the board for the TPS735xx, TI recommends that the board be designed with separate ground planes for Vin and Vout which are only connected at the GND pin of the device. Also, the ground connection for the bypass capacitor must be connected directly to the GND pin of the device. By following the foregoing two guidelines, you can improve the PSRR performance of the TPS735xx. See the TPS735xx data sheet (SBVS087) for specific layout guidelines.

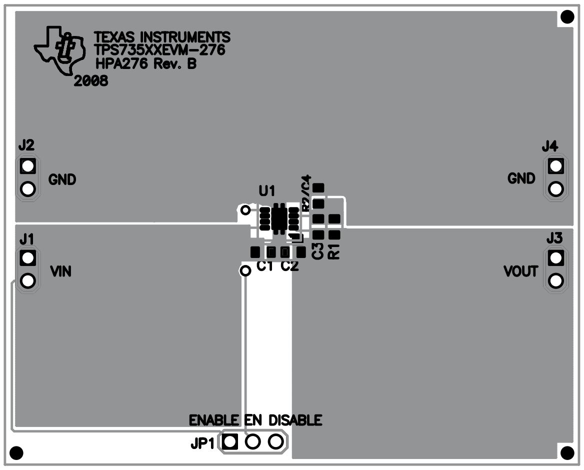


Figure 1. Assembly Layer

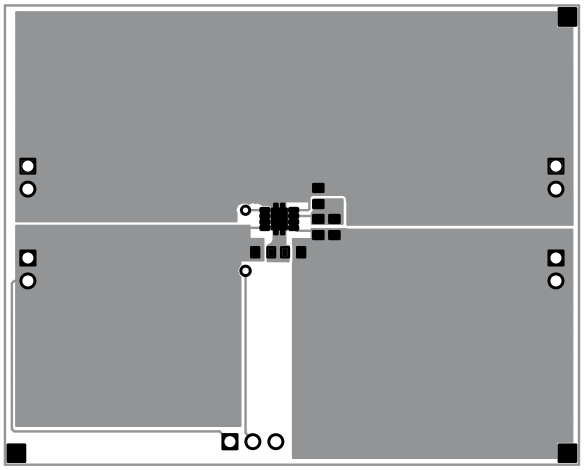


Figure 2. Top Layer Routing

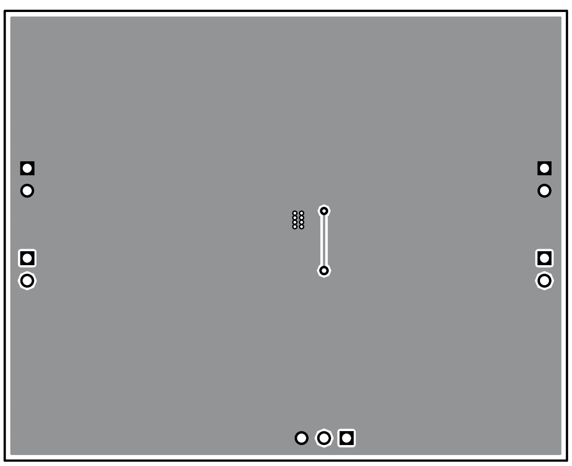
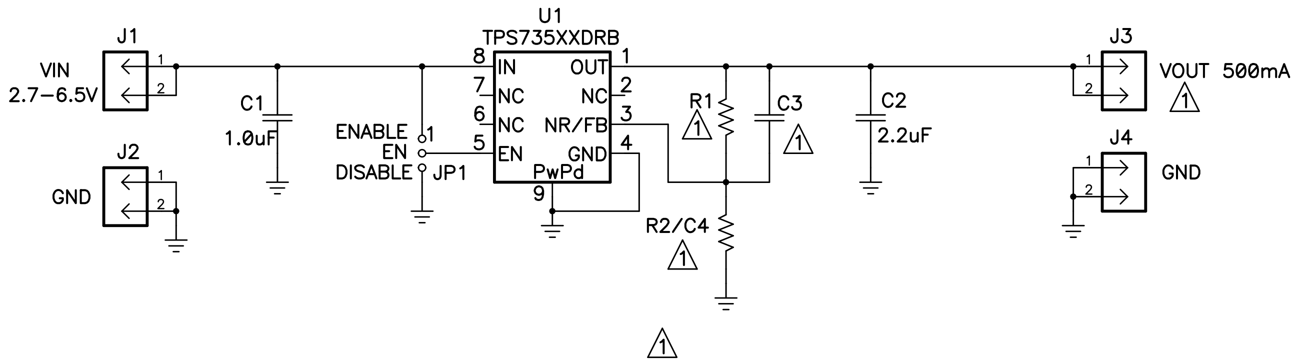


Figure 3. Bottom Layer Routing

6 Schematic and Bill of Materials

This section provides the TPS735xxEVM-276 schematic and bill of materials.

6.1 Schematic



ASSY	U1	R1	R2/C4	C3	VOUT
–001	TPS73501DRB	56.2K	110K	22pF	1.80V
–002	TPS73525DRB	Open	0.01uF	Open	2.50V

Figure 4. TPS735xxEVM-276 Schematic

6.2 Bill of Materials

Table 1. TPS735xxEVM-276 Bill of Materials

-001	-002	RefDes	Value	Description	Size	Part Number	MFR
1	1	C1	1.0 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	C1608X5R1A105K	TDK
1	1	C2	2.2 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	Std	Std
1	0	C3	22 pF	Capacitor, Ceramic, 16V, X5R, 10%	0603	Std	Std
0	0	C3	Open				
0	1	C4	0.01 µF	Capacitor, Ceramic, 16V, X5R, 10%	0603	Std	Std
4	4	J1–J4	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch × 2	PTC36SAAN	Sullins
1	1	JP1	PTC36SAAN	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 inch × 3	PTC36SAAN	Sullins
1	0	R1	56.2K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	R1	Open				
1	0	R2	110K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	0	U1	TPS73501DRB	IC, 500mA, Low Quiescent Current, Ultra-Low Noise, High PSRR LDO, adjustable	SON-8	TPS73501DRB	TI
0	1	U1	TPS73525DRB	IC, 500mA, Low Quiescent Current, Ultra-Low Noise, High PSRR LDO, 2.5V	SON-8	TPS73525DRB	TI
1	1		HPA276	PCB, 2.0" × 2.5" × 0.062"		HPA276	Any
1	1	—		Shunt, 100 mil, Black	0.100	929950-00	3M

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7 V to 6.5 V and the output voltage range of 1.193 V to 6.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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