Precision Low Noise Operational Amplifier

ISL76627

The ISL76627 is a very high precision amplifier featuring very low noise, low offset voltage, low input bias current and low temperature drift making it the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for ISL76627 include precision active filters, precision power supply controls, data acquisition signal conditioning, sensor interface, instrumentation and high grade audio.

Of particular interest for automotive applications is the wide range operating voltage of this op-amp combined with the combination of precision and speed.

The ISL76627 is available in an 8 Ld SOIC package. The device is offered in standard pin configurations and operates over the extended temperature range of -40°C to +125°C.

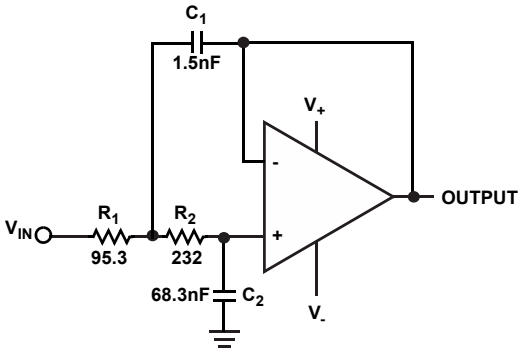
The ISL76627 is fully TS16949 compliant and tested to AEC-Q100 specifications.

Features

- Very Low Voltage Noise 2.5nV/Hz
- Low Input Offset . . . . . 70µV, Max.
- Superb Offset Drift . . . . . 0.5µV/°C, Max.
- Input Bias Current . . . . . 10nA, Max.
- Wide Supply Range . . . . . .4.5V to 40V
- Gain-bandwidth Product . . . . . 10MHz Unity Gain Stable
- No Phase Reversal

Applications

- Precision Active Filters
- Instrumentation
- Sensor Interface
- PLL Loop Filtering
- Precision Signal Conditioning
- High Grade Audio



SALLEN-KEY LOW PASS FILTER (1MHz)

FIGURE 1. TYPICAL APPLICATION

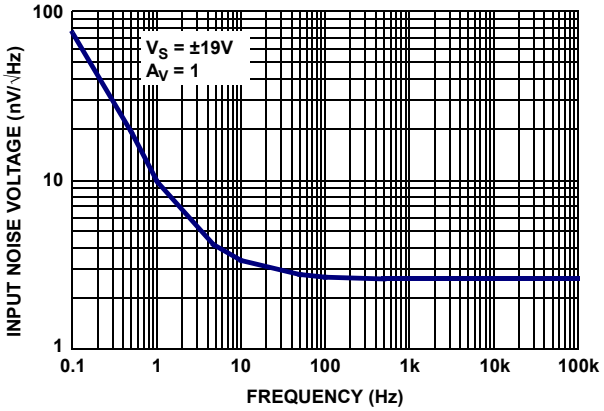


FIGURE 2. INPUT NOISE VOLTAGE SPECTRAL DENSITY

Ordering Information

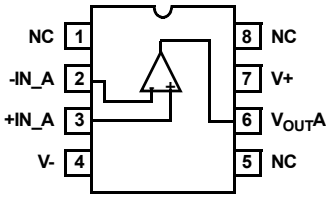
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OS} (MAX) (µV)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL76627ABZ	76627 ABZ	70	-40 to +125	8 Ld SOIC	M8.15

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL76627. For more information on MSL please see techbrief TB363.

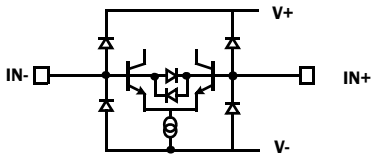
Pin Configuration

ISL76627
(8 LD SOIC)
TOP VIEW

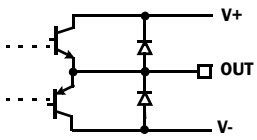


Pin Descriptions

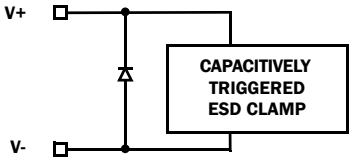
ISL76627 (8 LD SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	V-	Circuit 3	Negative power supply
7	V+	Circuit 3	Positive power supply
6	$V_{OUT}A$	Circuit 2	Amplifier A output
2	-IN_A	Circuit 1	Amplifier A inverting input
1, 5, 8	NC	-	Not Connected – This pin is not electrically connected internally.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 0.5V
Min/Max Input Voltage . . . . . V-- 0.5V to V+ + 0.5V
Max/Min Input Current for
  Input Voltage >V+ or <V- . . . . . ±20mA
Output Short-Circuit Duration
  (1 Output at a Time) . . . . . Indefinite
ESD Tolerance
  Human Body Model (Tested per JESD22-A114F) 4.0kV
  Machine Model (Tested per EIA/JESD22-A115-A) 500V
  Charged Device Model (Tested per JESD22-C101D) 1.5kV
Di-electrically Isolated PR40 process . . . . . Latch-up free

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC (Note 4, 5)	120	60

Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Offset Voltage		-70	10	70	µV
			-120	-	**120**	µV
TCV_{OS}	Offset Voltage Drift		**-0.5**	0.1	**0.5**	µV/°C
I_{OS}	Input Offset Current		-10	1	10	nA
			-12	-	**12**	nA
I_B	Input Bias Current		-10	1	10	nA
			-12	-	**12**	nA
V_{CM}	Input Voltage Range	Guaranteed by CMRR	-13	-	13	V
			-12	-	**12**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	115	120	-	dB
		V_{CM} = -12V to +12V	**115**	-	-	dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	115	125	-	dB
		V_S = ±3V to ± 20V	**115**	-	-	dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V R_L = 10kΩ to ground	1000	1500	-	V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.65	-	V
			13.2	-	-	V
		R_L = 2kΩ to ground	13.4	13.5	-	V
			13.1	-	-	V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground	-	-13.65	-13.5	V
			-	-	**-13.2**	V
		R_L = 2kΩ to ground	-	-13.5	-13.4	V
			-	-	**-13.1**	V

Electrical Specifications V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_S	Supply Current/Amplifier		-	2.2	2.8	mA
			-	-	**3.7**	mA
I_{SC}	Short-Circuit	R_L = 0Ω to ground	-	±45	-	mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	±2.25	-	±20	V
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product		-	10	-	MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz	-	85	-	nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz	-	3	-	nV/√Hz
e_n	Voltage Noise Density	f = 100Hz	-	2.8	-	nV/√Hz
e_n	Voltage Noise Density	f = 1kHz	-	2.5	-	nV/√Hz
e_n	Voltage Noise Density	f = 10kHz	-	2.5	-	nV/√Hz
in	Current Noise Density	f = 10kHz	-	0.4	-	pA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 2kΩ	-	0.00022	-	%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 10, R_L = 2kΩ, V_O = 4V_{P-P}	-	±3.6	-	V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}	-	36	-	ns
	Fall Time 90% to 10% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}	-	38	-	ns
t_S	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	A_V = -1 V_{OUT} = 10V_{P-P}, R_g = R_f =10k, R_L = 2kΩ to V_{CM}	-	3.4	-	µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 10V_{P-P}, R_L = 2kΩ to V_{CM}	-	3.8	-	µs
t_{OL}	Output Overload Recovery Time	A_V = 100, V_{IN} = 0.2V R_L = 2kΩ to V_{CM}	-	1.7	-	µs

Electrical Specifications V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Offset Voltage		-70	10	70	µV
			-120	-	**120**	µV
TCV_{OS}	Offset Voltage Drift		**-0.5**	0.1	**0.5**	µV/°C
I_{OS}	Input Offset Current		-10	1	10	nA
			-12	-	**12**	nA
I_B	Input Bias Current		10	1	10	nA
			-12	-	**12**	nA
V_{CM}	Common Mode Input Voltage Range	Guaranteed by CMRR	-3	-	3	V
			-2	-	**2**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	115	120	-	dB
		V_{CM} = -2V to +2V	**115**	-	-	dB

Electrical Specifications V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	115	125	-	dB
		V_S = ±3V to ±5V	**115**	-	-	dB
A_{VOL}	Open-Loop Gain	V_O = -3V to +3V R_L = 10kΩ to ground	1000	1500	-	V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.65	-	V
			3.2	-	-	V
		R_L = 2kΩ to ground	3.4	3.5	-	
			3.1	-	-	V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground	-	-3.65	-3.5	V
			-	-	**-3.2**	V
		R_L = 2kΩ to ground	-	-3.5	-3.4	
			-	-	**-3.1**	V
I_S	Supply Current/Amplifier		-	2.2	2.8	mA
			-	-	**3.7**	mA
I_{SC}	Short-Circuit		-	±45	-	mA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product		-	10	-	MHz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, Vo = 2.5V_{RMS}, R_L = 2kΩ	-	0.0034	-	%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 10, R_L = 2kΩ	-	±3.6	-	V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}	-	36	-	ns
	Fall Time 90% to 10% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}	-	38	-	ns
t_S	Settling Time to 0.1%	A_V = -1, V_{OUT} = 4V_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}	-	1.6	-	µs
	Settling Time to 0.01%	A_V = -1, V_{OUT} = 4V_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}	-	4.2	-	µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

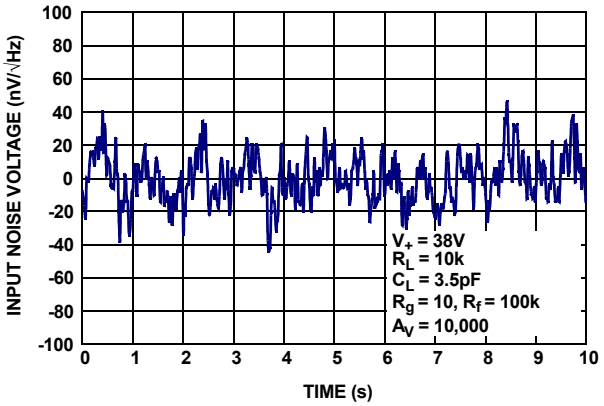


FIGURE 3. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

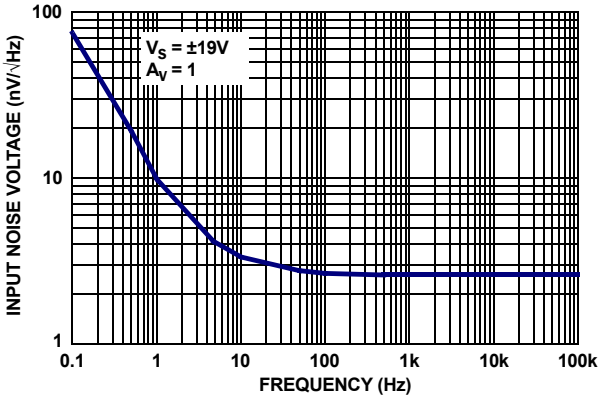


FIGURE 4. INPUT NOISE VOLTAGE SPECTRAL DENSITY

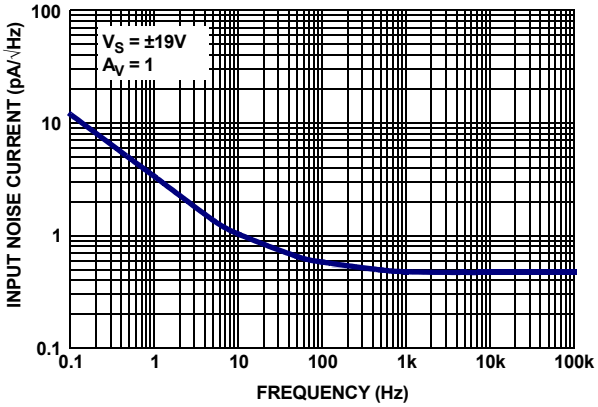


FIGURE 5. INPUT NOISE CURRENT SPECTRAL DENSITY

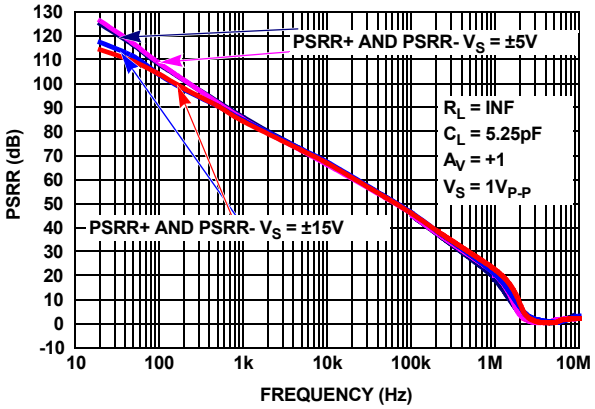


FIGURE 6. PSRR vs FREQUENCY, $V_S = \pm5V, \pm15V$

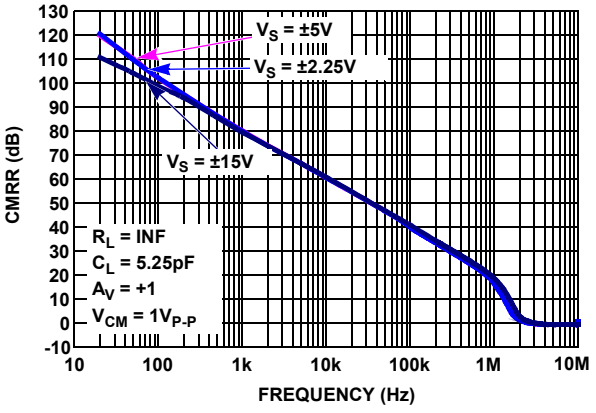


FIGURE 7. CMRR vs FREQUENCY, $V_S = \pm2.25, \pm5V, \pm15V$

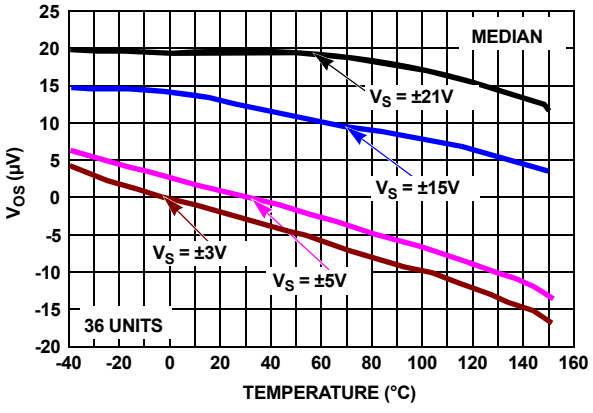


FIGURE 8. V_{OS} vs TEMPERATURE vs V_{SUPPLY}

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

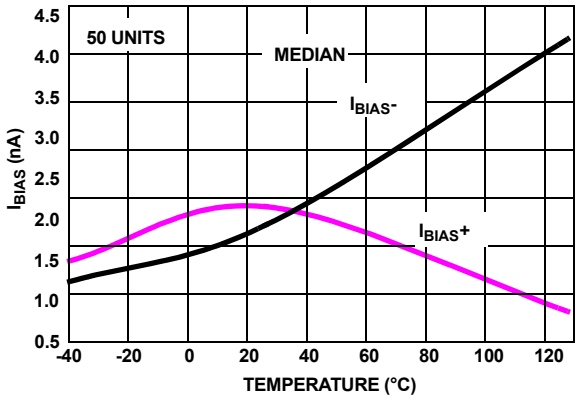


FIGURE 9. I_{IB} vs TEMPERATURE, $V_S = \pm15V$

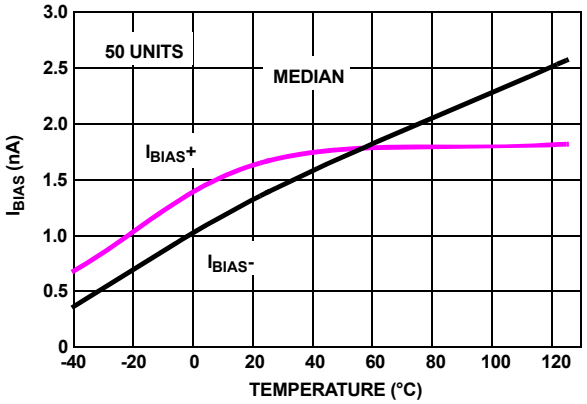


FIGURE 10. I_{IB} vs TEMPERATURE, $V_S = \pm5V$

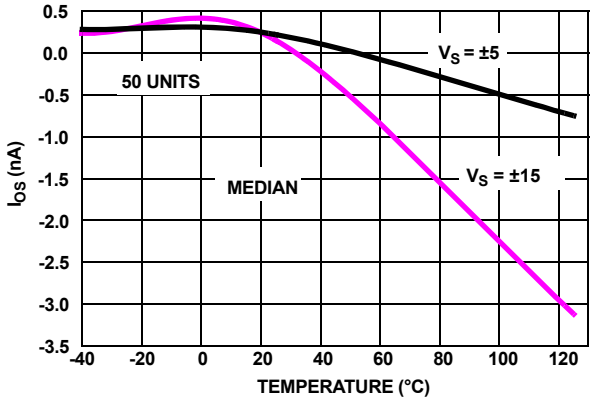


FIGURE 11. I_{OS} vs TEMPERATURE vs SUPPLY

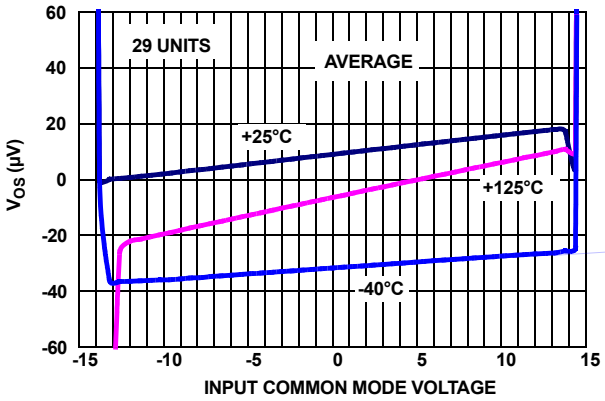


FIGURE 12. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, $V_S = \pm15V$

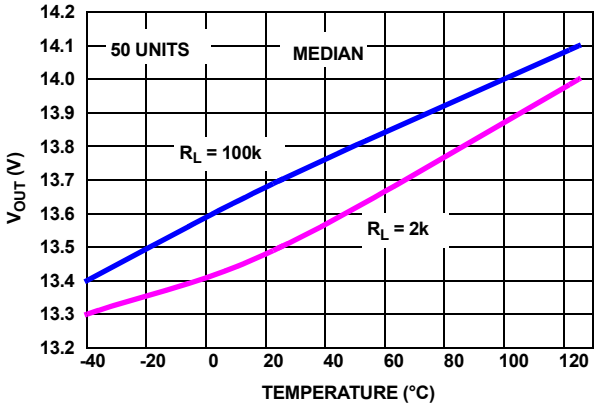


FIGURE 13. V_{OH} vs TEMPERATURE, $V_S = \pm15V$

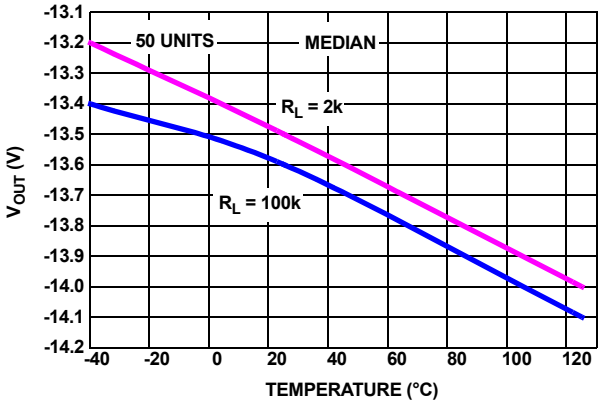


FIGURE 14. V_{OL} vs TEMPERATURE, $V_S = \pm15V$

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

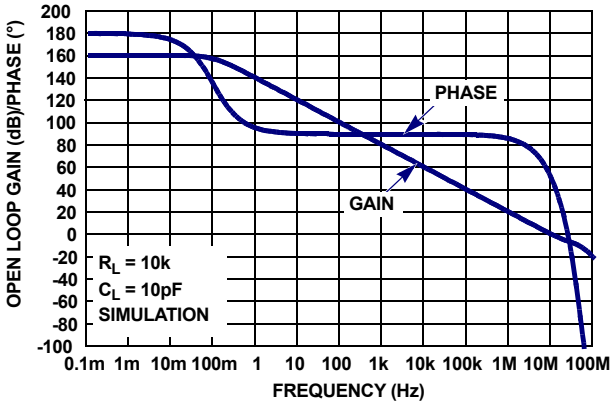


FIGURE 15. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 10k\Omega$, $C_L = 10pF$

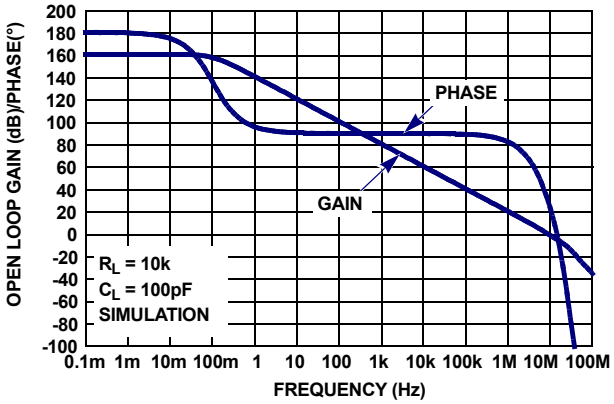


FIGURE 16. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 10k\Omega$, $C_L = 100pF$

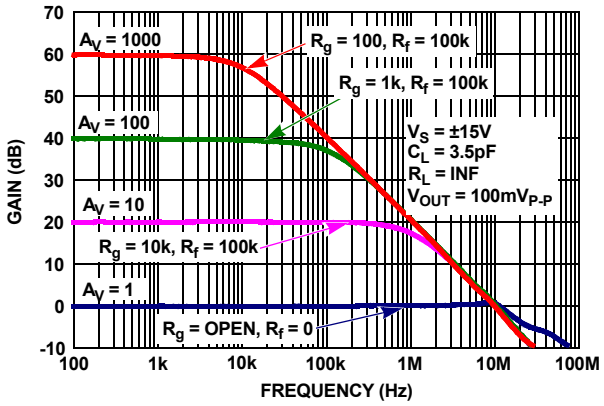


FIGURE 17. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

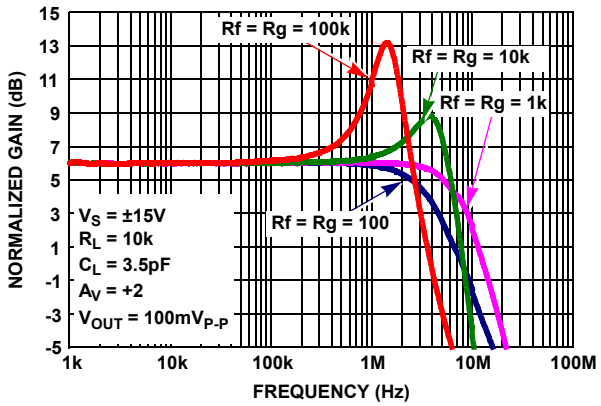


FIGURE 18. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

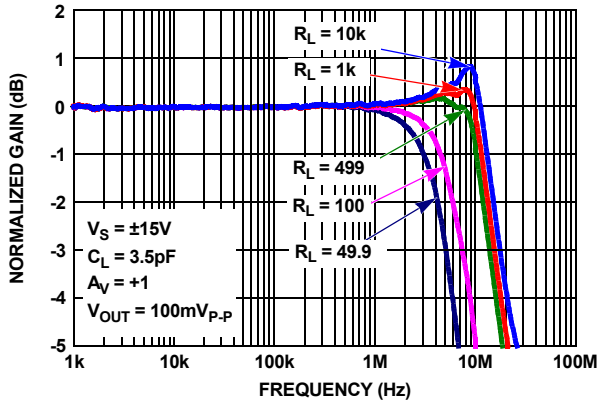


FIGURE 19. GAIN vs FREQUENCY vs R_L

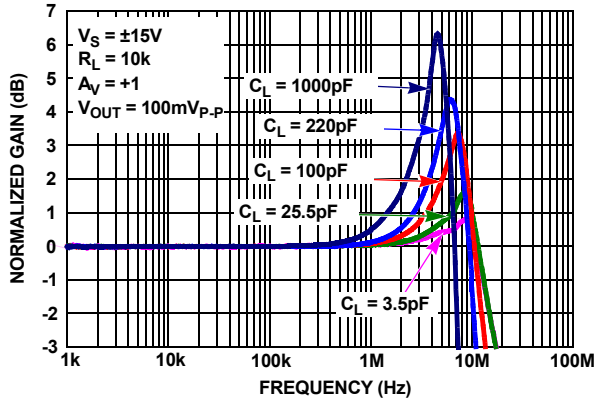


FIGURE 20. GAIN vs FREQUENCY vs C_L

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

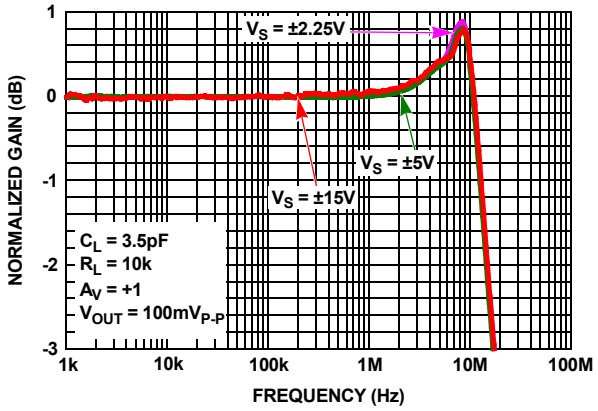


FIGURE 21. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

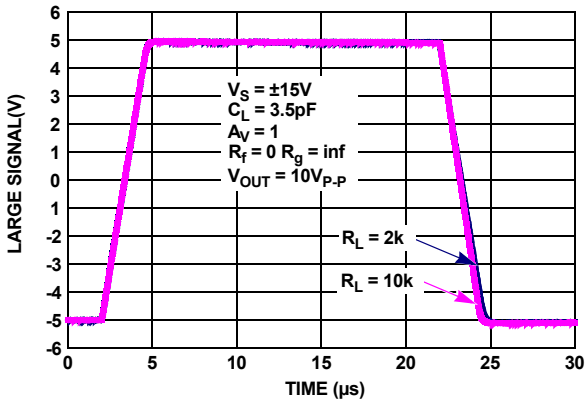


FIGURE 22. LARGE SIGNAL 10V STEP RESPONSE, V_S = ±15V

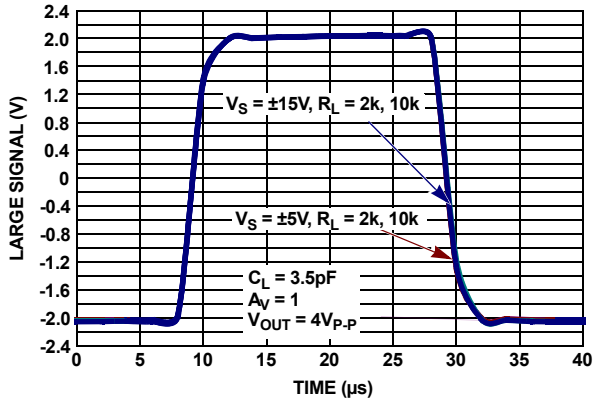


FIGURE 23. LARGE SIGNAL TRANSIENT RESPONSE vs R_L, V_S = ±5V, ±15V

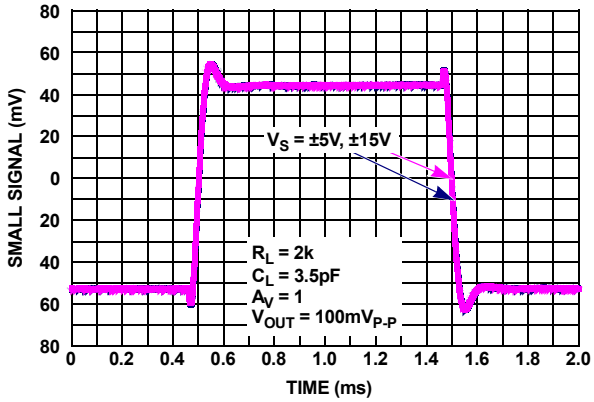


FIGURE 24. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

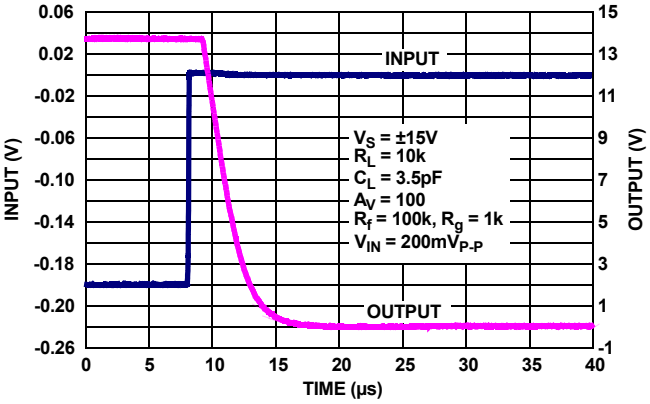


FIGURE 25. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

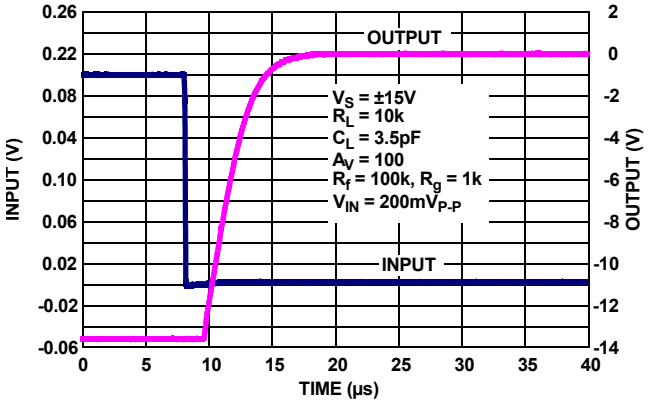


FIGURE 26. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

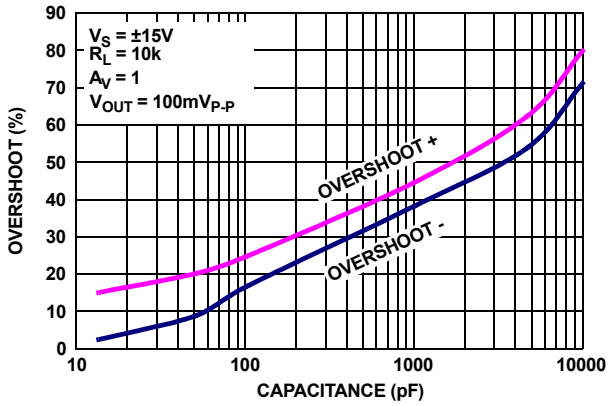


FIGURE 27. % OVERSHOOT vs LOAD CAPACITANCE, V_S = ±15V

Applications Information

Functional Description

The ISL76627 is a single, low noise 10MHz BW precision op amp. The device is fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (1nA typical), low input offset voltage (10µV typ), low input noise voltage (3nV/√Hz), and low 1/f noise corner frequency (5Hz). The amplifier also features high open loop gain (1500V/mV) for excellent CMRR (120dB) and THD+N performance (0.0002% @ 3.5V_{RMS}, 1kHz into 2kΩ). A complementary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The device is designed to operate over the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). Parameter variation with operating voltage is shown in the "Typical Performance Curves" beginning on page 6.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, and an additional anti-parallel diode pair across the inputs (see Figures 28 and 29).

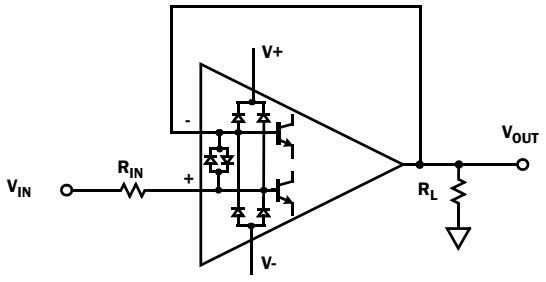


FIGURE 28. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

For unity gain applications (see Figure 28) where the output is connected directly to the non-inverting input, a current limiting resistor (R_{IN}) will be needed under the following conditions to protect the anti-parallel differential input protection diodes.

- The amplifier input is supplied from a low impedance source.
- The input voltage rate-of-rise (dV/dt) exceeds the maximum slew rate of the amplifier (±3.6V/µs).

If the output lags far enough behind the input, the anti-parallel input diodes can conduct. For example, if an input pulse ramps from 0V to +10V in 1µs, then the output of the ISL76627 will reach only +3.6V (slew rate = 3.6V/µs), while the input is at 10V. The input differential voltage of 6.4V will force input ESD diodes to conduct, dumping the input current directly into the output stage and the load. The resulting current flow can cause permanent damage to the ESD diodes. The ESD diodes are rated to 20mA, and in the previous example, setting R_{IN} to 1k resistor (see Figure 28) would limit the current to < 6.4mA, and provide additional protection up to ±20V at the input.

In applications where one or both amplifier input terminals are at risk of exposure to high voltage, current limiting resistors may be needed at each input terminal (see Figure 29 R_{IN}+, R_{IN}-) to limit current through the power supply ESD diodes to 20mA.

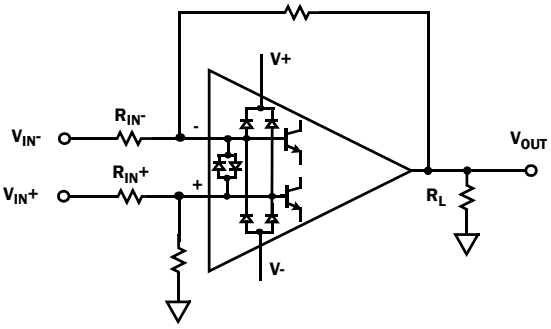


FIGURE 29. INPUT ESD DIODE CURRENT LIMITING - DIFFERENTIAL INPUT

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL76627 is immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAX} \quad \text{(EQ. 1)}$$

where:

- P_{DMAX} is the maximum power dissipation of the amplifier in the package, and can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of the amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

ISL76627 SPICE Model

Figure 30 shows the SPICE model schematic and Figure 31 shows the net list for the ISL76627 SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, Slew Rate, CMRR, Gain and Phase. The DC parameters are V_{OS}, I_{OS}, total supply current and output voltage swing. The model does not model input bias current. The model uses typical parameters given in the “Electrical Specifications” table beginning on page 3. The AVOL is adjusted for 128dB with the dominate pole at 5Hz. The CMRR is set higher than the “Electrical Specifications” table to better match design simulations (150dB,f = 50Hz). The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 32 through 47 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Closed Loop Gain vs Rf/Rg, Closed Loop Gain vs R_L, Closed Loop Gain vs C_L, Large Signal 10V Step Response, Open Loop Gain Phase and Simulated CMRR vs Frequency.

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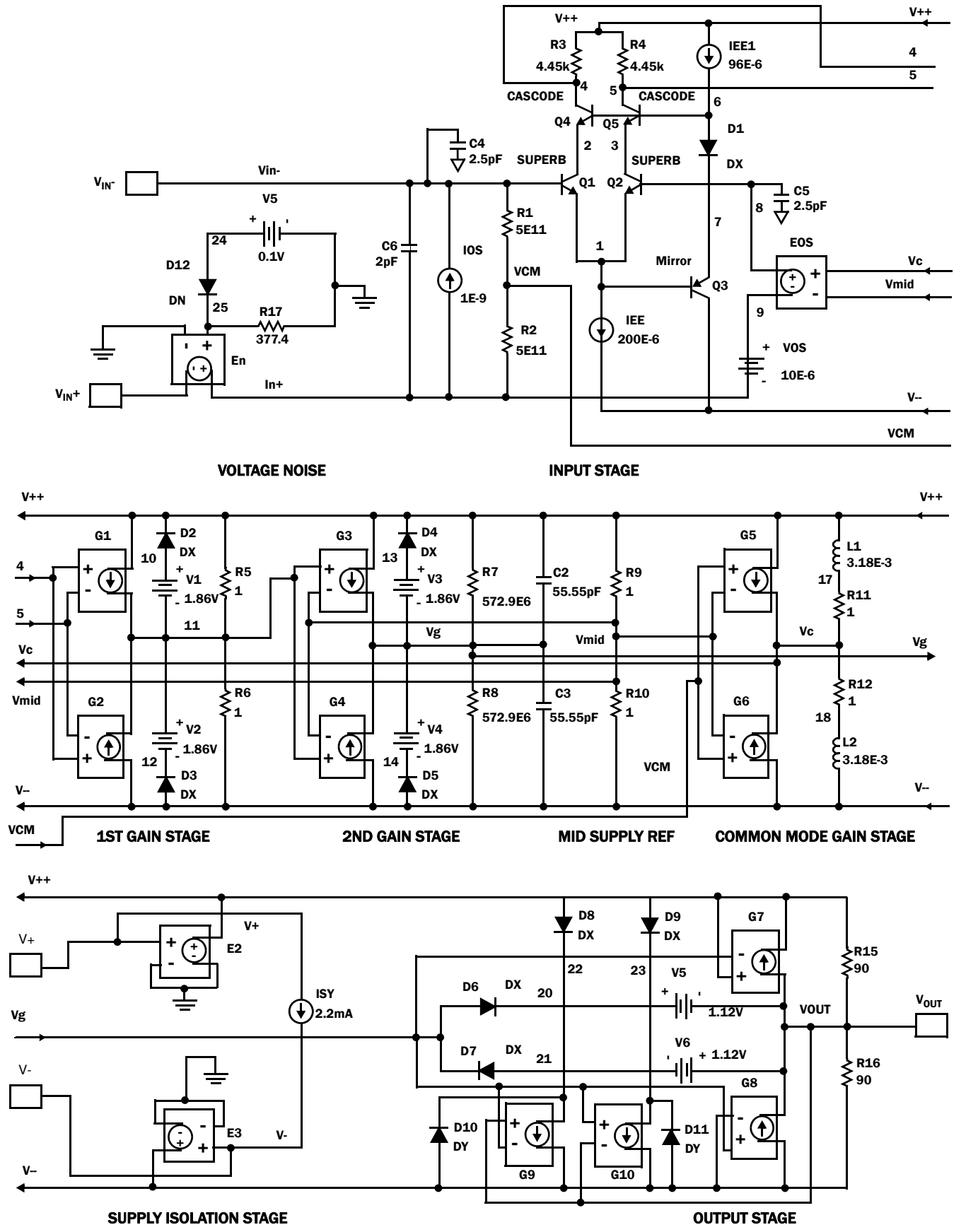

FIGURE 30. SPICE SCHEMATIC

```
* source ISL76627_SPICEmodel
* Revision D, October 24 2011 LaFontaine
* Model for Noise, supply currents, 150dB f=50Hz
CMRR, *128dB f=5Hz AOL
*Copyright 2009 by Intersil Corporation
*Refer to data sheet "LICENSE STATEMENT" Use of
*this model indicates your acceptance with the
*terms and provisions in the License Statement.
* Connections: +input
*               |    -input
*               |    |    +Vsupply
*               |    |    |    -Vsupply
*               |    |    |    |    output
*               |    |    |    |    |
.subckt ISL76627subckt Vin+ Vin- V+ V- VOUT
* source ISL76627_SPICEMODEL_0_0
*
*Voltage Noise
E_En          IN+ VIN+ 25 0 1
R_R17          25 0  377.4 TC=0,0
D_D12          24 25 DN
V_V7          24 0 0.1
*
*Input Stage
I_IOS          IN+ VIN- DC 1e-9
C_C6          IN+ VIN- 2E-12
R_R1          VCM VIN-  5e11 TC=0,0
R_R2          IN+ VCM  5e11 TC=0,0
Q_Q1          2 VIN- 1 SuperB
Q_Q2          3 8 1 SuperB
Q_Q3          V-- 1 7 Mirror
Q_Q4          4 6 2 Cascode
Q_Q5          5 6 3 Cascode
R_R3          4 V++ 4.45e3 TC=0,0
R_R4          5 V++ 4.45e3 TC=0,0
C_C4 VIN- 0  2.5e-12
C_C5 8 0  2.5e-12
D_D1          6 7 DX
I_IEE          1 V-- DC 200e-6
I_IEE1          V++ 6 DC 96e-6
V_VOS          9 IN+ 10e-6
E_EOS          8 9 VC VMID 1
*
*1st Gain Stage
G_G1          V++ 11 4 5 0.0487707
G_G2          V-- 11 4 5 0.0487707
R_R5          11 V++ 1 TC=0,0
R_R6          V-- 11  1 TC=0,0
D_D2          10 V++ DX
D_D3          V-- 12 DX
V_V1          10 11 1.86
V_V2          11 12 1.86
*
*2nd Gain Stage
G_G3          V++ VG 11 VMID 4.60767E-3
G_G4          V-- VG 11 VMID 4.60767E-3
R_R7          VG V++ 572.958E6 TC=0,0
R_R8          V-- VG  572.958E6 TC=0,0
C_C2          VG V++ 55.55e-12  TC=0,0
C_C3          V-- VG  55.55e-12  TC=0,0
D_D4          13 V++ DX
D_D5          V-- 14 DX
V_V3          13 VG 1.86
V_V4          VG 14 1.86
*
*Mid supply Ref
R_R9          VMID V++ 1 TC=0,0
R_R10          V-- VMID  1 TC=0,0
I_ISY     V+ V- DC 2.2E-3
E_E2          V++ 0 V+ 0 1
E_E3          V-- 0 V- 0 1
*
*Common Mode Gain Stage with Zero
G_G5          V++ VC VCM VMID 31.6228e-9
G_G6          V-- VC VCM VMID 31.6228e-9
R_R11          VC 17  1 TC=0,0
R_R12          18 VC  1 TC=0,0
L_L1          17 V++ 3.183e-3
L_L2          18 V-- 3.183e-3
*
*Output Stage with Correction Current Sources
G_G7          VOUT V++ V++ VG 1.11e-2
G_G8          V-- VOUT VG V-- 1.11e-2
G_G9          22 V-- VOUT VG 1.11e-2
G_G10          23 V-- VG VOUT 1.11e-2
D_D6          VG 20 DX
D_D7          21 VG DX
D_D8          V++ 22 DX
D_D9          V++ 23 DX
D_D10          V-- 22 DY
D_D11          V-- 23 DY
V_V5          20 VOUT 1.12
V_V6          VOUT 21 1.12
R_R15          VOUT V++ 9E1 TC=0,0
R_R16          V-- VOUT  9E1 TC=0,0
*
.model SuperB npn
+ is=184E-15 bf=30e3 va=15 ik=70E-3 rb=50
+ re=0.065 rc=35 cje=1.5E-12 cjc=2E-12
+ kf=0 af=0
.model Cascode npn
+ is=502E-18 bf=150 va=300 ik=17E-3 rb=140
+ re=0.011 rc=900 cje=0.2E-12 cjc=0.16E-12f
+ kf=0 af=0
.model Mirror pnp
+ is=4E-15 bf=150 va=50 ik=138E-3 rb=185
+ re=0.101 rc=180 cje=1.34E-12 cjc=0.44E-12
+ kf=0 af=0
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL76627subckt
```

FIGURE 31. SPICE NET LIST

Characterization vs Simulation Results

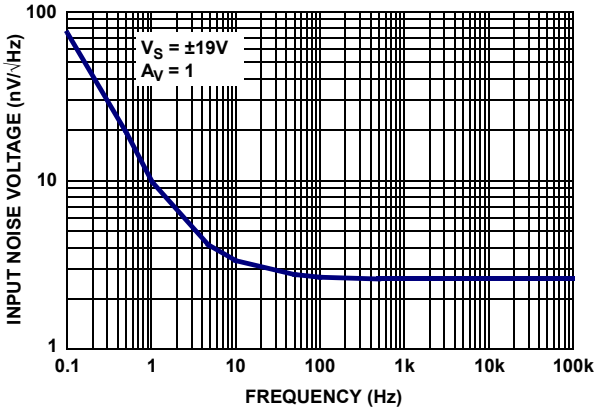

FIGURE 32. CHARACTERIZED INPUT NOISE VOLTAGE

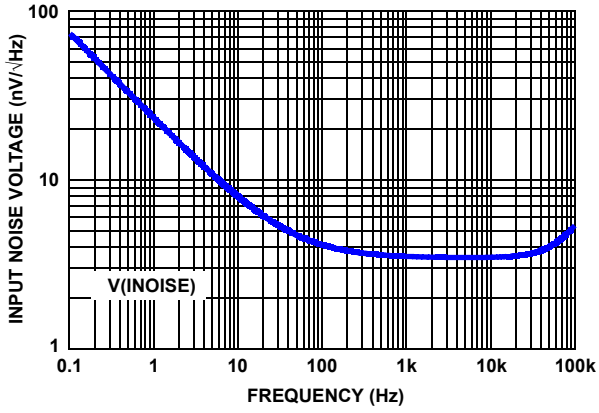

FIGURE 33. SIMULATED INPUT NOISE VOLTAGE

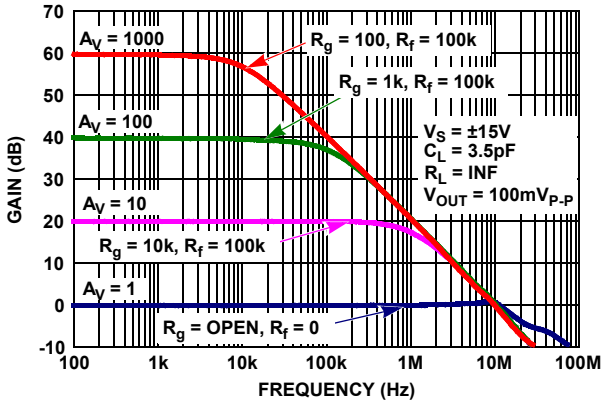

FIGURE 34. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

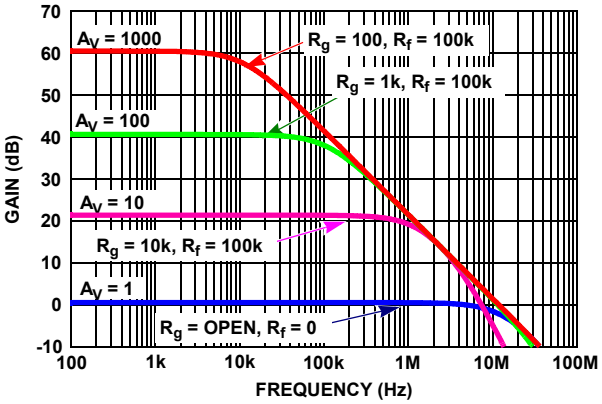

FIGURE 35. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

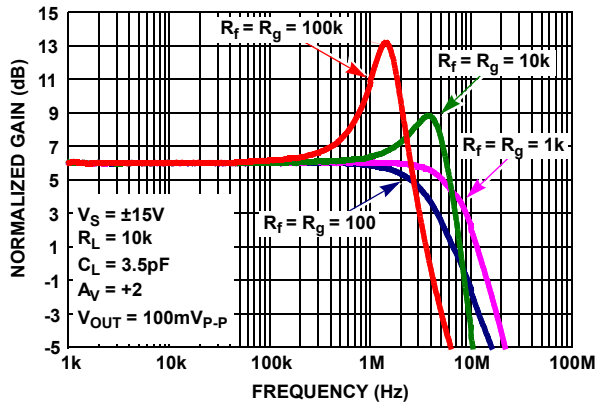

FIGURE 36. CHARACTERIZED CLOSED LOOP GAIN vs R_f/R_g

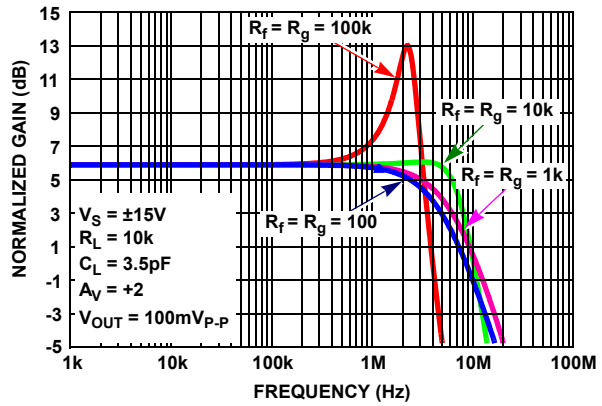

FIGURE 37. SIMULATED CLOSED LOOP GAIN vs R_f/R_g

Characterization vs Simulation Results (Continued)

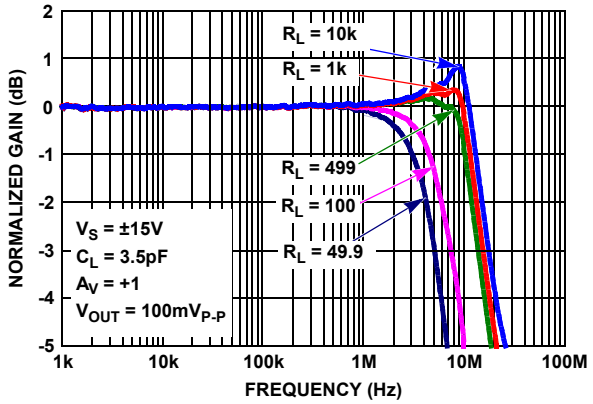

FIGURE 38. CHARACTERIZED CLOSED LOOP GAIN vs R_L

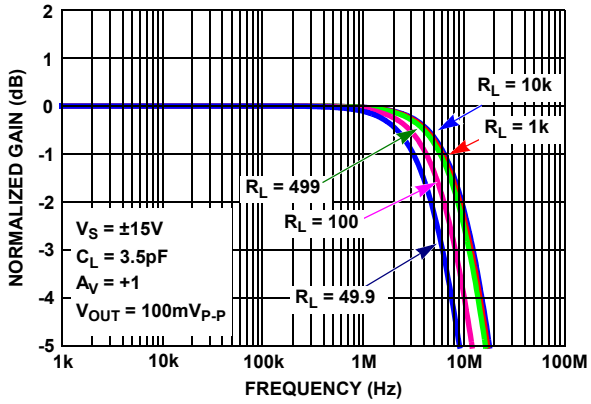

FIGURE 39. SIMULATED CLOSED LOOP GAIN vs R_L

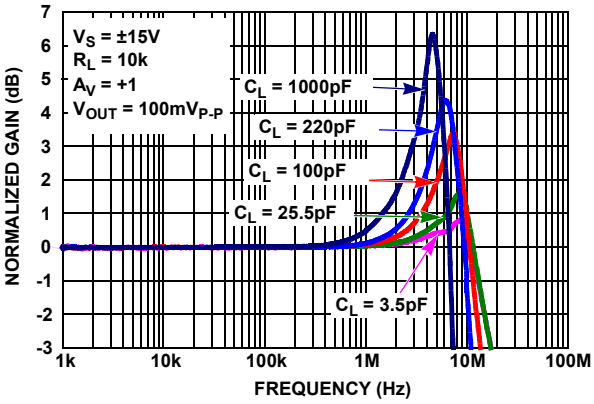

FIGURE 40. CHARACTERIZED CLOSED LOOP GAIN vs C_L

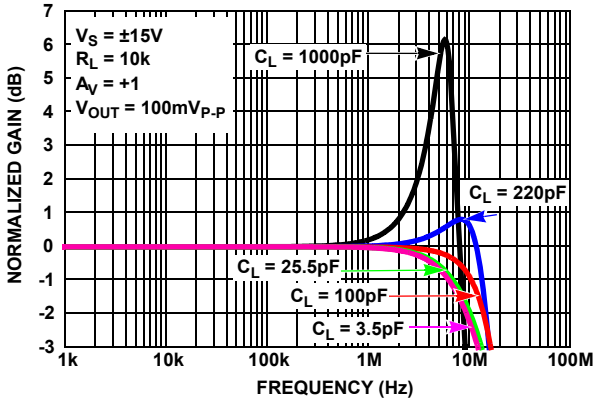

FIGURE 41. SIMULATED CLOSED LOOP GAIN vs C_L

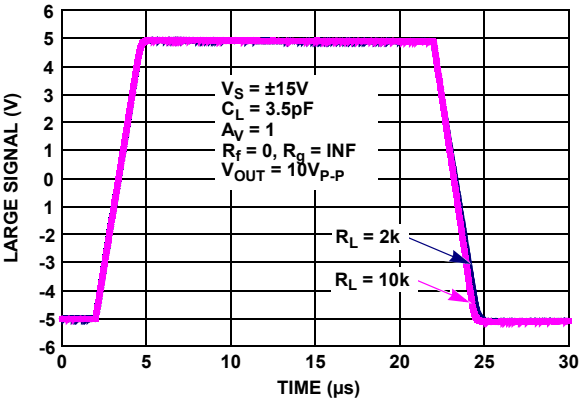

FIGURE 42. CHARACTERIZED LARGE SIGNAL 10V STEP RESPONSE

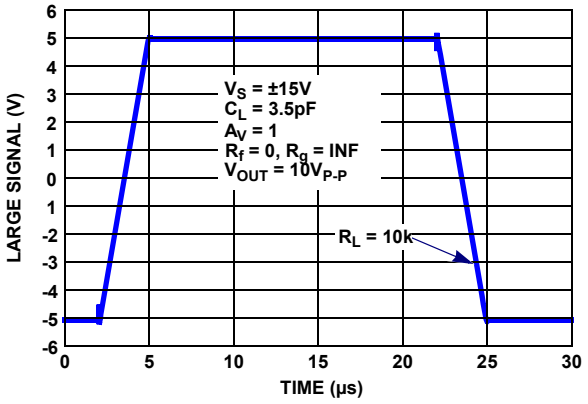

FIGURE 43. SIMULATED LARGE SIGNAL 10V STEP RESPONSE

Characterization vs Simulation Results (Continued)

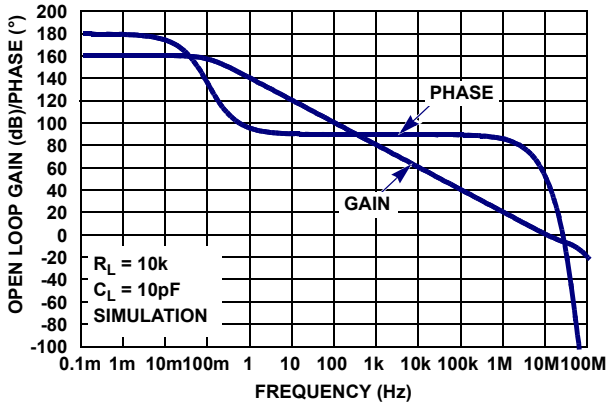

FIGURE 44. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

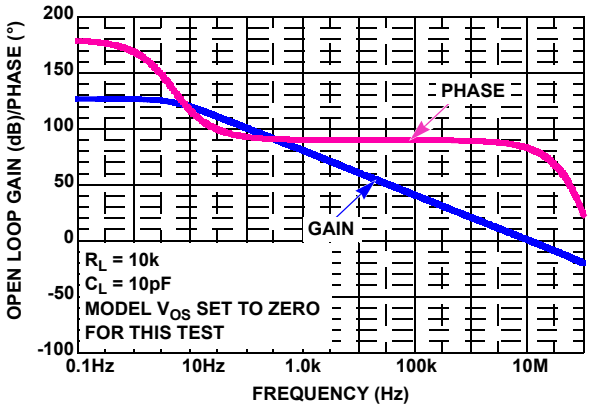

FIGURE 45. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

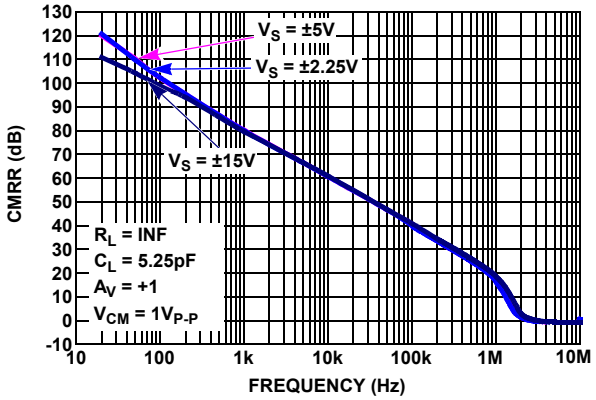

FIGURE 46. CHARACTERIZED CMRR vs FREQUENCY

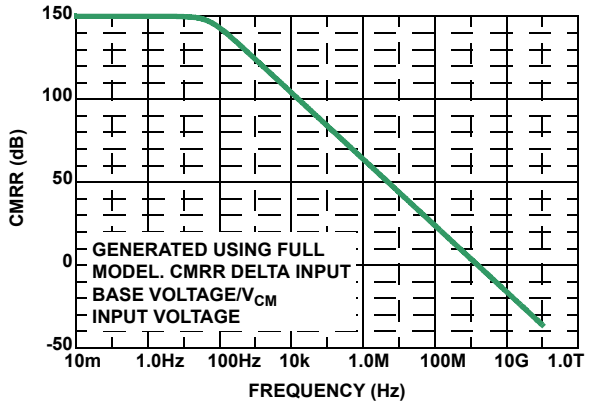

FIGURE 47. SIMULATED CMRR vs FREQUENCY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
10/18/11	FN7725.1	page 13 Figure 31 Netlist. Changed ISL28127 to ISL76627 and added space on line 15 between Vin- and V+.
7/12/11	FN7725.0	Initial Release.

Products

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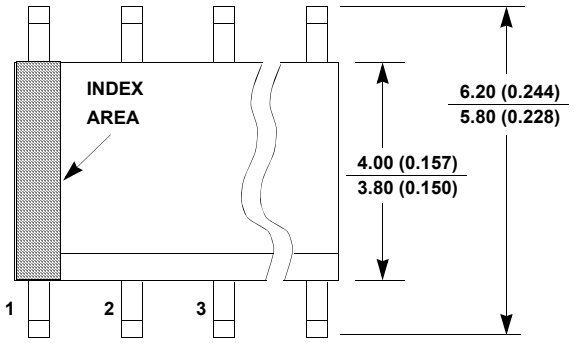
Package Outline Drawing

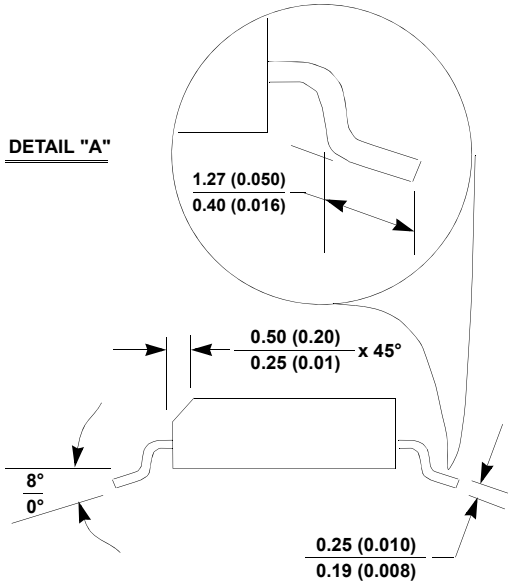
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

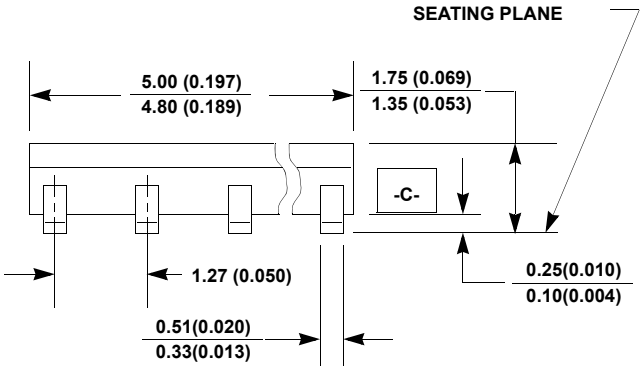
Rev 3, 3/11



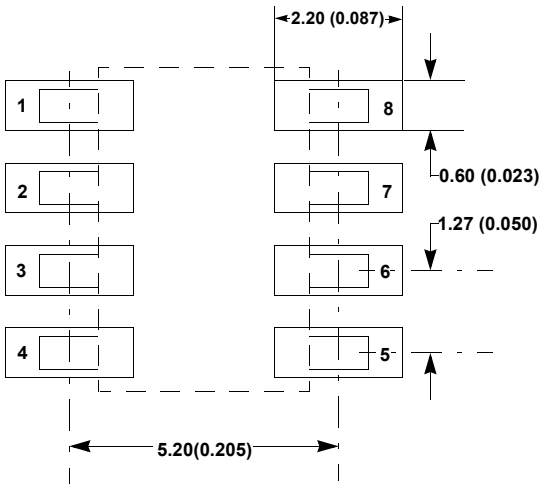
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.