CDB8421

Evaluation Board For CS8421

Features

- Asynchronous Sample Rate Conversion
- CS8416 S/PDIF Digital Audio Receiver
- CS8406 S/PDIF Digital Audio Transmitter
- Header for External Serial Audio I/O
- 3.3 V or 5.0 V Logic Interface
- No software required to operate.
- Demonstrates recommended layout and grounding arrangements.

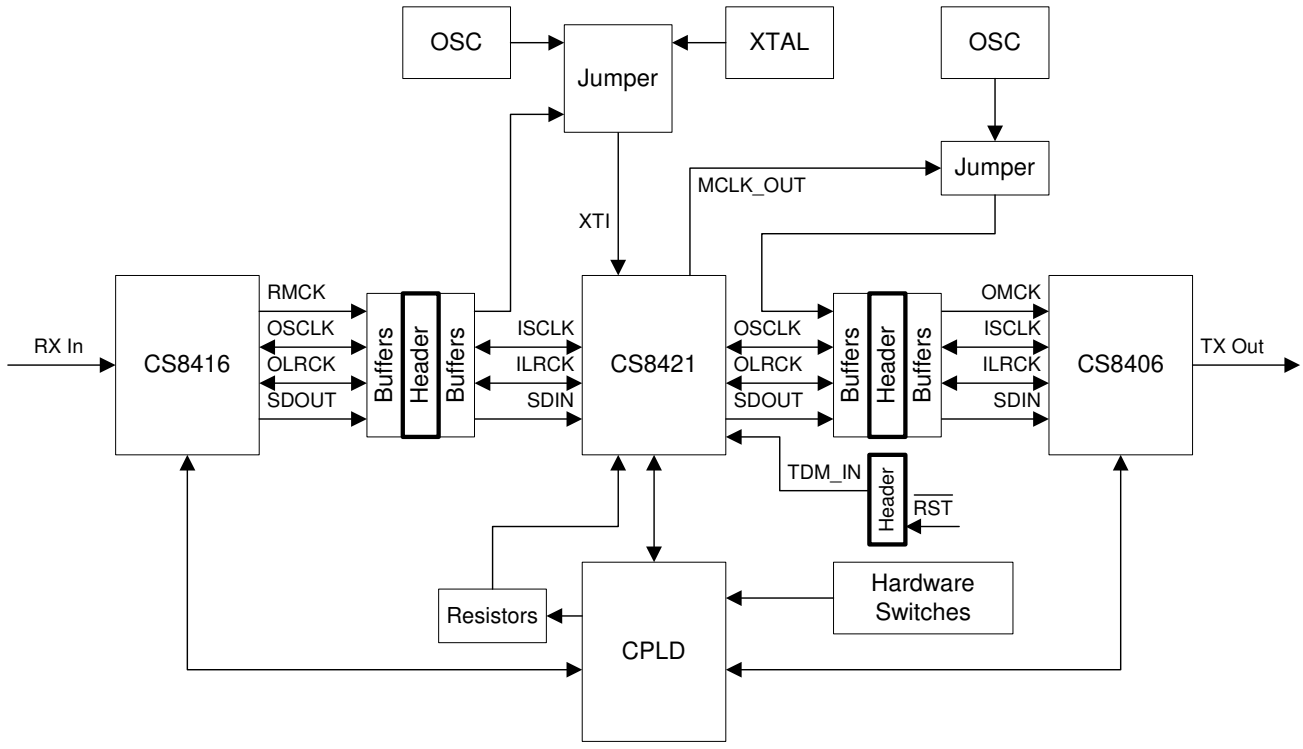
Description

The CDB8421 demonstration board is an excellent means for evaluating the CS8421 sample rate converter. Evaluation requires a digital signal source, digital analyzer, and power supplies.

System timing can be provided by the CS8421, by the CS8416 phase-locked to its S/PDIF input, by an I/O stake header, or by an on-board oscillator. Digital I/O is available via coaxial (RCA) or optical connectors to the CS8416 and CS8406. All configuration control is handled from onboard switches.

ORDERING INFORMATION

CDB8421 Evaluation Board



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1. SYSTEM OVERVIEW

The CDB8421 demonstration board is an excellent means for evaluating the CS8421 stereo sample rate converter. Digital audio signal interfaces are provided in the form of S/PDIF receiver and transmitter and PCM clock/data headers.

The CDB8421 schematic set is shown in Figures 1 through 9 and the board layout is shown in Figures 10 through 12, and the bill of materials is shown in Table 3.

1.1 CS8421 Sample Rate Converter

A complete description of the CS8421 is included in the CS8421 product data sheet [1], available online at *http://www.cirrus.com*

D9 (SRC_UNLOCK) indicates when the SRC is not locked and output from the CS8421 SDOUT pin is not valid.

1.2 CS8406 Digital Audio Transmitter

The operation of the CS8406 transmitter and a discussion of the digital audio interface are included in the CS8406 data sheet [2].

The CS8406 converts the PCM data generated by the CS8421 to the standard S/PDIF data format. The CS8406 can operate in master or slave mode and accepts 128*Fs, 256*Fs, or 512*Fs master clock on the OMCK input pin. The serial audio input data for the CS8406 is received from the serial audio output of the CS8421. Digital Interface format selection of I²S (up to 24-bit), Left Justified (up to 24-bit), or Right Justified (16 or 24-bit) can be made.

S/PDIF output is through J6 or J15.

1.3 CS8416 Digital Audio Receiver

The operation of the CS8416 receiver (see Figure 3) and a discussion of the digital audio interface are included in the CS8416 data sheet [3].

The CS8416 converts the input S/PDIF data stream into PCM data for the CS8421. The CS8416 operates in master or slave mode and can output either 128*Fs or 256*Fs from its RMCK pin. Digital Interface format selection of I²S (24-bit), Left Justified (24-bit), or Right Justified (16 or 24-bit) can be made.

The CS8416 contains an internal input multiplexer which must be set to receive data from either the optical input connector (J12) or coaxial input connector (J5). This is done by setting the appropriate switch on switch-bank S4 to the COAXIAL or OPTICAL position.

D10 (RERR) indicates a receiver error, such as loss of lock.

S/PDIF input is through J5 or J12.

1.4 Clocking

Table 1 shows the available I/O configurations and their respective clock sources. When the CS8416 is selected to master SCLK and LRCK (CS8421 input port set to slave), J7 should be set to 8416. When the CS8421 input port is selected to master SCLK and LRCK (CS8416 set to slave), J7 may be set to 8416, OSC, or XTAL. When the CS8406 is selected to master SCLK and LRCK (CS8421 output port set to slave), J13 should be set to OSC. When the CS8421 output port is selected to master SCLK and LRCK (CS8406 set to slave), J13 should be set to 8421. The board is shipped with a 24.576 MHz crystal/oscillator stuffed at Y1, Y2, and Y3.

CS8421 Input Port	CS8421 Output Port	CS8421 XTI/XTO Clock Source	CS8406 OMCK Clock Source
Master	Slave	CS8416 RMCK	Y3
Slave	Master	CS8416 RMCK, Y1, or Y2	CS8421 MCLK_OUT
Slave	Slave	CS8416 RMCK, Y1, or Y2	Y3

Table 1. Clock Sources

1.5 Clock and Data Headers

The CDB8421 includes headers for input (J8) and output (J11) port clocks and data. These headers can enabled/disabled using S4. When not using these headers, SDIN should be jumpered to SDOUT on both J8 and J11. The pin functions for headers J8 and J11 are shown in Table 7.

The CDB8421 also includes a header for TDM operation (J16). Refer to the CS8421 data sheet for possible TDM configurations [1]. This header can enabled/disabled using J14.

All headers operate at the VL supply, therefore any external circuit connected to these headers should also operate at VL.

1.6 CPLD Board Setup

The CPLD (U2) controls all of the configuration for the CS8421, CS8416, and CS8406. The CPLD decodes switches S1, S2, S3, and S4 and sets the appropriate mode of operation.

Switch S1 controls the master/slave and MCLK/LRCK ratio settings for the CS8421, CS8416, and CS8406. The functions for S1[3:0] are detailed in Table 2.

S1[3:0]	CS8421 Input	CS8421 Output
0000	Slave	Slave
0001	Slave	Master (Master Clock = 128*Fs)
0010	Slave	Master (Master Clock = 256*Fs)
0011	Slave	Master (Master Clock = 384*Fs)
0100	Slave	Master (Master Clock = 512*Fs)
1000	Master (Master Clock = 128*Fs)	Slave
1001	Master (Master Clock = 256*Fs)	Slave
1010	Master (Master Clock = 384*Fs)	Slave
1011	Master (Master Clock = 512*Fs)	Slave

Table 2. Switch S1, Serial Input and Output Master/Slave and Speed Mode Settings

Switch S2 controls the interface format of the CS8406 and the CS8421 output port. The functions for switches S2[3:0] are detailed in Table 3.

S2[3:0]	CS8421 Output Configuration
0000	I²S 16-bit Data
0001	I²S 20-bit Data
0010	I²S 24-bit Data
0011	I²S 32-bit Data
0100	Left Justified 16-bit Data
0101	Left Justified 20-bit Data
0110	Left Justified 24-bit Data
0111	Left Justified 32-bit Data
1000	Right Justified 16-bit Data
1001	Right Justified 20-bit Data
1010	Right Justified 24-bit Data
1011	Right Justified 32-bit Data
1100	TDM Mode, 16-bit Data
1101	TDM Mode, 20-bit Data
1110	TDM Mode, 24-bit Data
1111	TDM Mode, 32-bit Data

Table 3. Switch S2, Serial Output Formats

Switch S3 controls the interface format of the CS8416 and the CS8421 input port. The functions for switches S3[2:0] are detailed in Table 4.

S3[2:0]	CS8421 Output Configuration
000	I²S up to 32-bit Data
001	Left Justified up to 32-bit Data
010	Right Justified 16-bit Data
011	Right Justified 20-bit Data
100	Right Justified 24-bit Data
101	Right Justified 32-bit Data
110	Left Justified 24-bit Data

Table 4. Switch S3, Serial Input Formats

Switch S4 allows any of the PCM clocks/data to be turned off, selection between the OPTICAL and COAXIAL S/PDIF inputs, bypassing the CS8421 sample rate converter, and turning off the CS8421 MCLK_OUT signal. To input and output S/PDIF to and from the CS8421, the switches labeled 8416_PCM, 8421_INPUT_PCM, 8421_OUTPUT_PCM, and 8406_PCM should all be set in the CLOSED position. The functions for switches S4[6:0] are detailed in Table 5.

Switch Name	OPEN	CLOSED
8416_PCM	Inhibits Clock I/O and Data Output from CS8416 to Header J8	Allows Clock I/O and Data Output from CS8416 to Header J8
8421_INPUT_PCM	Inhibits Clock I/O and Data Input from Header J8 to CS8421	Allows Clock I/O and Data Input from Header J8 to CS8421
8421_OUPUT_PCM	Inhibits Clock I/O and Data Output from CS8421 to Header J11	Allows Clock I/O and Data Output from CS8421 to Header J11
8406_PCM	Inhibits Clock I/O and Data Output from Header J11 to CS8406	Allows Clock I/O and Data Output from Header J11 to CS8406
8416_RXSEL	Selects Coaxial Connector (J5) for S/PDIF Input	Selects Optical Receiver (J12) for S/PDIF Input
8421_BYPASS	Selects CS8421 SRC Bypass Mode (no sample rate conversion)	Selects CS8421 SRC Active Mode
8421_MCLK_OUT	CS8421 MCLK_OUT Pin Held Low	CS8421 MCLK_OUT Pin Active

Table 5. Switch S4, Board Setup

NOTE:The reset button must be pressed before a new mode of operation takes affect.

Some speed modes and switch combinations are not compatible with the CS8416, CS8421, or the CS8406. LED's D4, D5, and D7 indicate that a switch setting is not compatible with the corresponding part.

1.7 Power

Power must be supplied to the evaluation board through the +5.0 V binding post (J1). On-board regulators supply +3.3 V and +2.5 V to the rest of the board. Jumper J3 sets the VL supply of the CS8416, CS8421, and CS8406 to either +3.3 V or +5.0 V. All voltage inputs must be referenced to the single black banana-type ground connector (J2).

WARNING:Please refer to the CS8421 data sheet for allowable voltage levels.

1.8 Grounding and Power Supply Decoupling

The CS8421 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 1 provides an overview of the connections to the CS8421, Figure 10 shows the component placement, Figure 11 shows the top layout, and Figure 12 shows the bottom layout. The decoupling capacitors are located as close to the CS8421 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

CONNECTOR	Reference Designator	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J1	Input	+5.0 V Power Supply
GND	J2	Input	Ground Reference
VL	J3	Input	+3.3 V to +5.0 V Variable Power Supply for VD
COAX IN	J5	Input	CS8416 digital audio input via coaxial cable
OPTICAL IN	J12	Input	CS8416 digital audio input via optical cable
COAX OUT	J6	Output	CS8406 digital audio output via coaxial cable
OPTICAL OUT	J15	Output	CS8406 digital audio output via optical cable
PCM Headers	J8 J11	Input/Output	I/O for PCM Clocks & Data
TDM Header	J16	Input/Output	I/O for TDM Clocks & Data

Table 6. System Connections

PIN	SIGNAL
1	Master Clock
2	Serial Bit Clock
3	Left-Right (Word) Clock
4	Serial Data (In for J8, Out for J11)
5	Serial Data (Out for J8, In for J11)
6-10	Ground

Table 7. Header Connections (J8 and J11)

2. BLOCK DIAGRAM

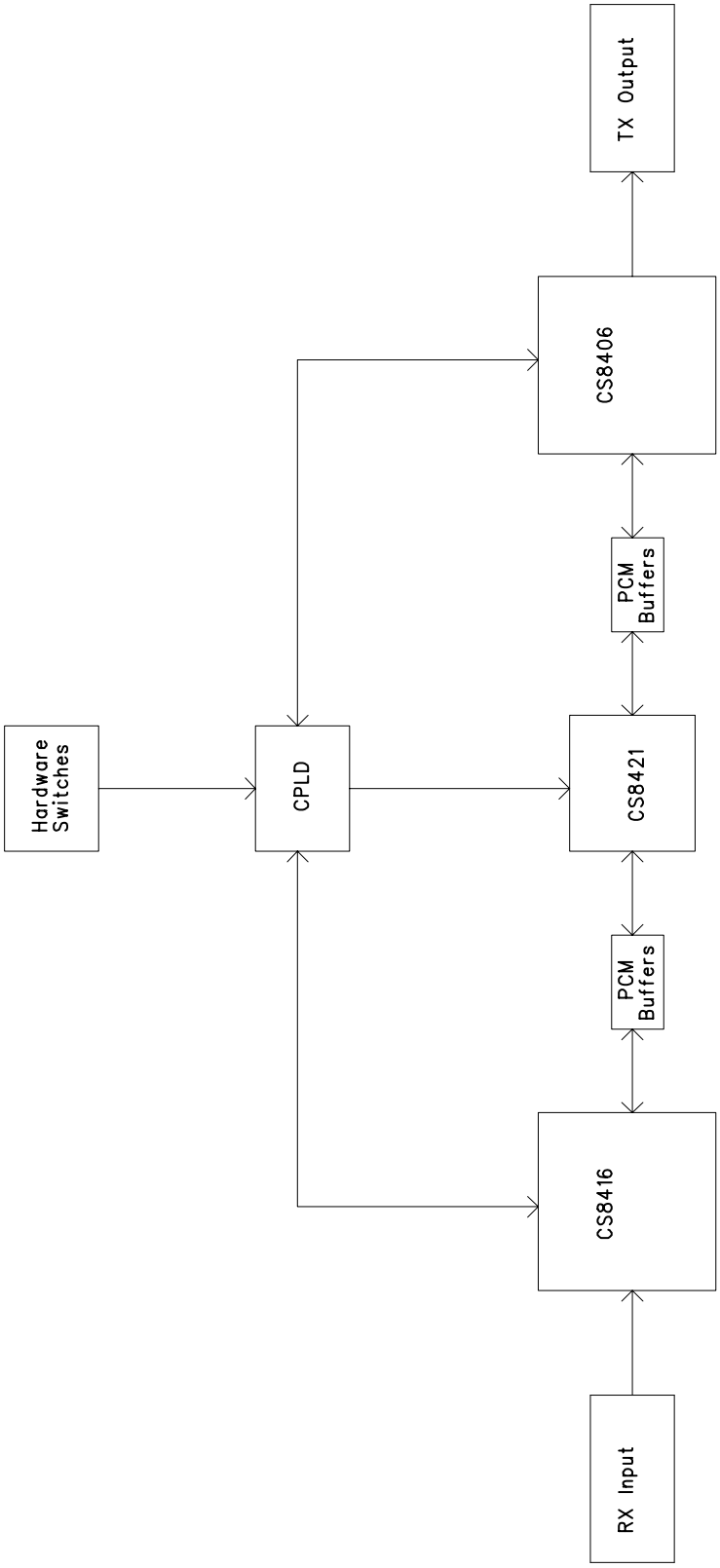


Figure 1. Block Diagram

3. SCHEMATICS

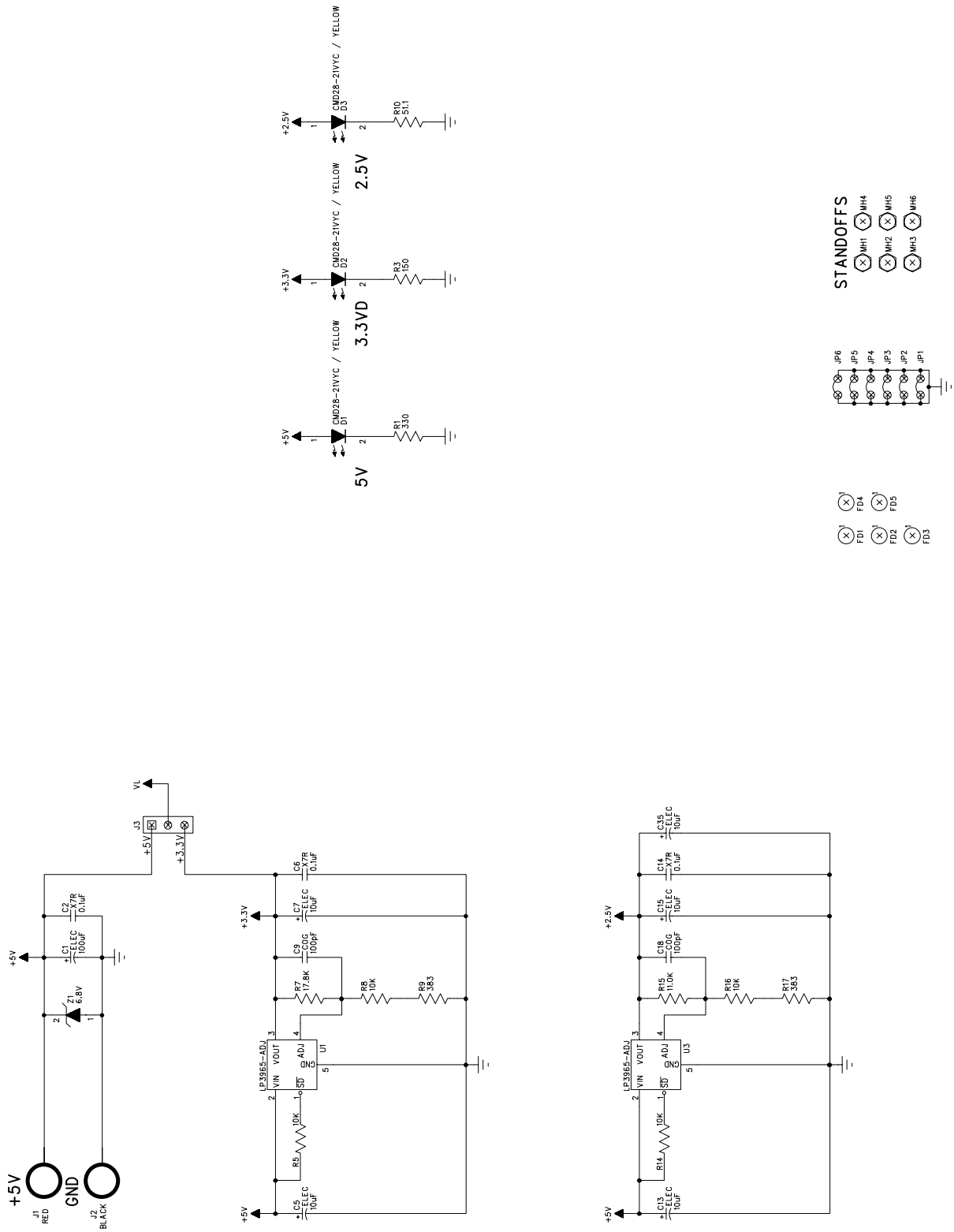


Figure 2. Power

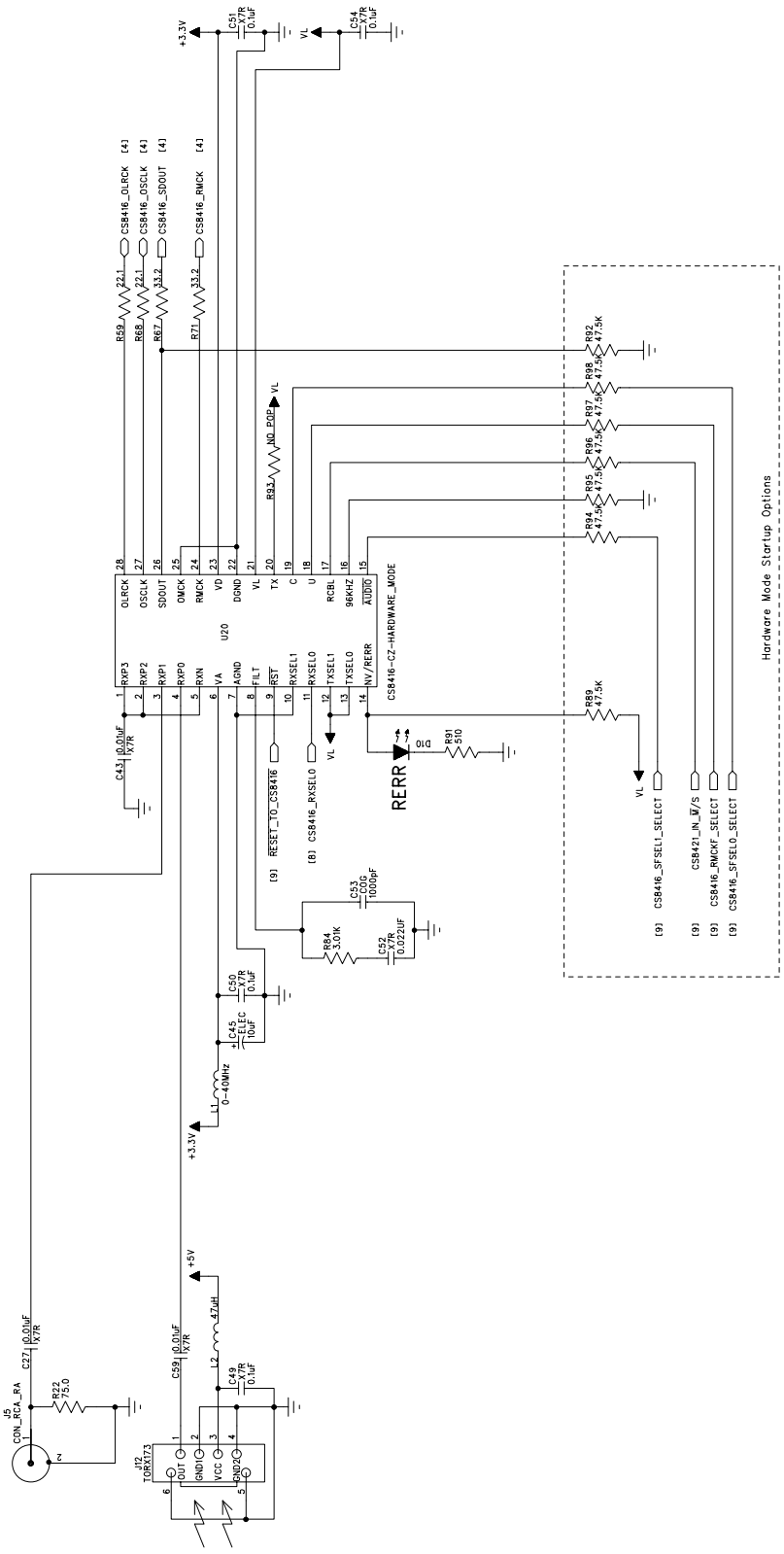


Figure 3. CS8416

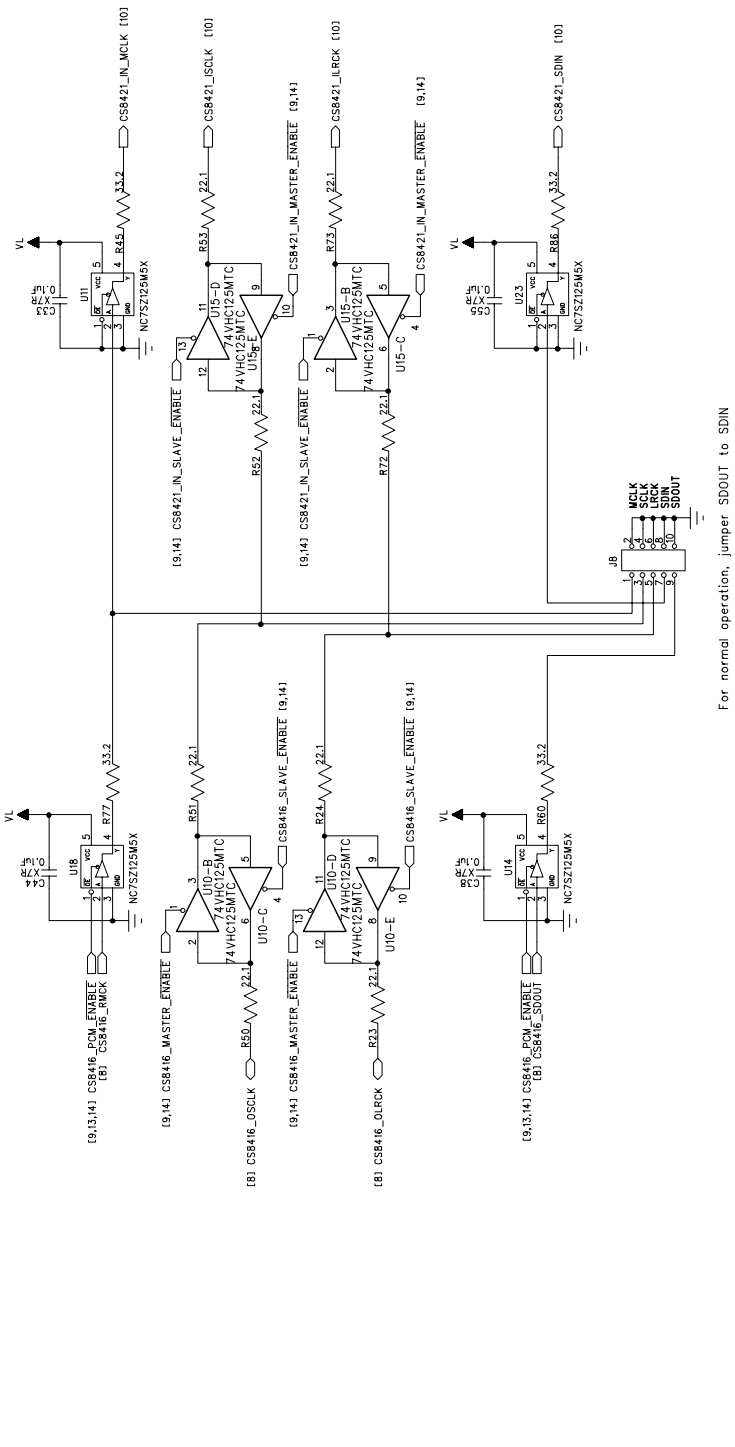


Figure 4. CS8416 to CS8421

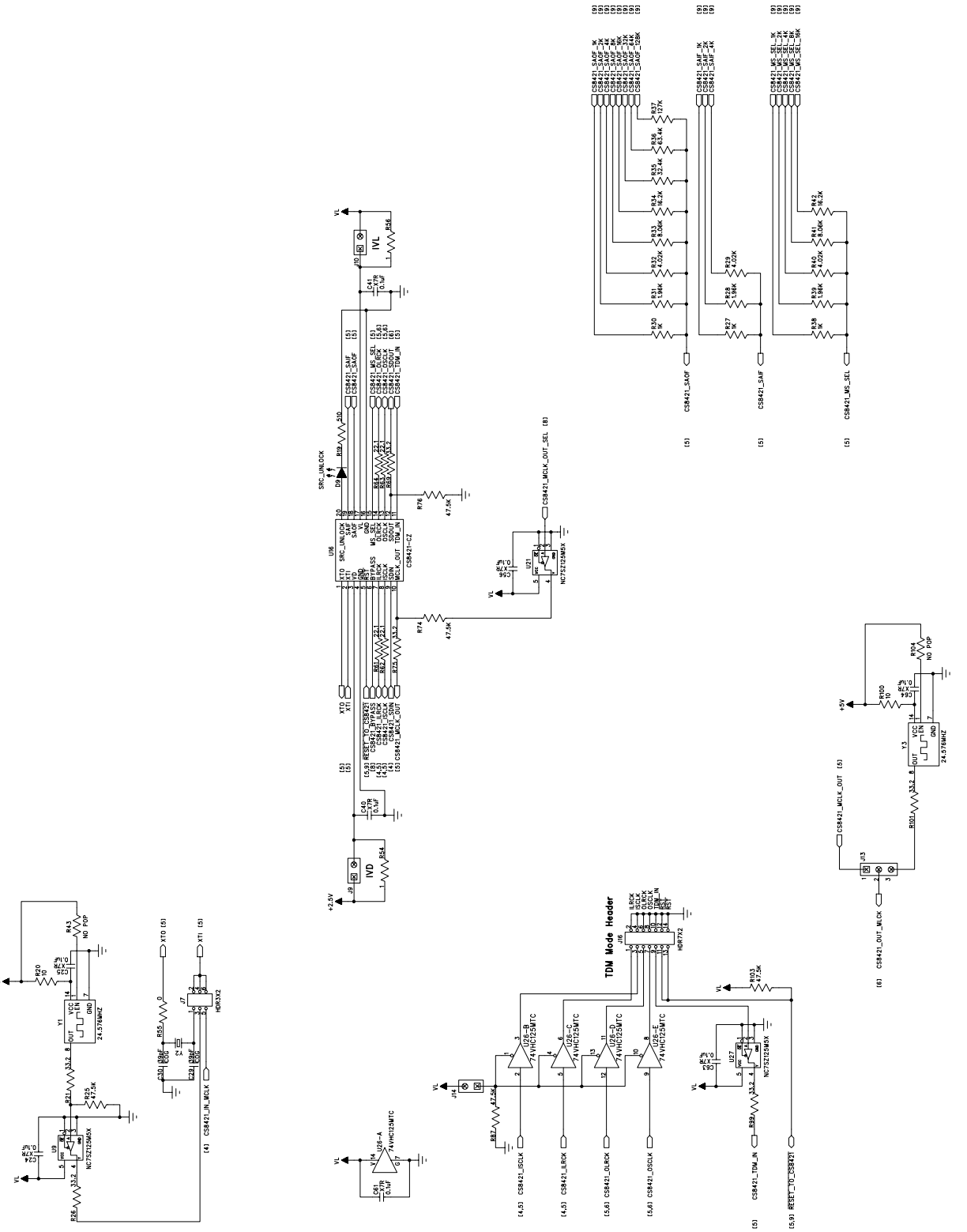


Figure 5. CS8421

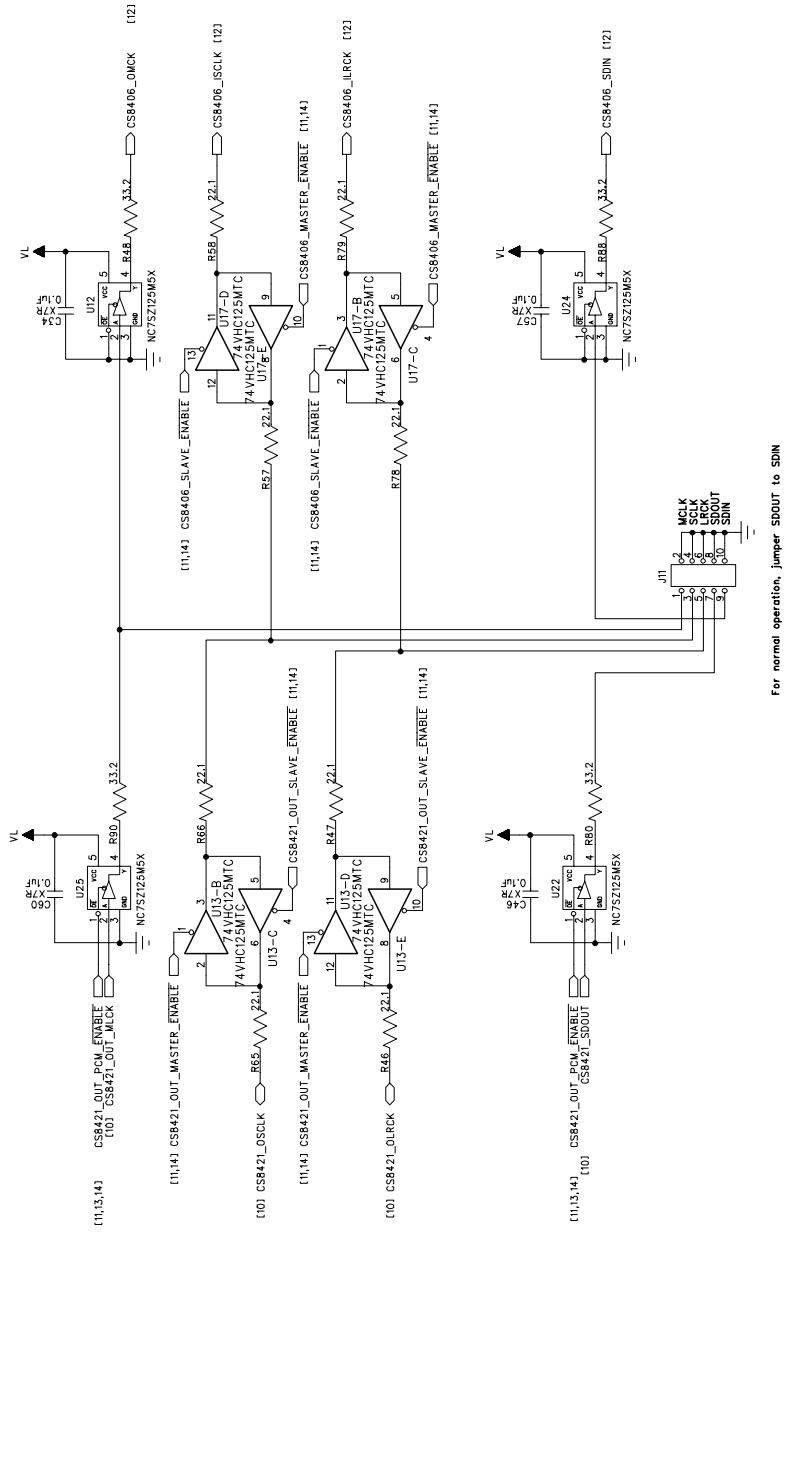


Figure 6. CS8421 to CS8406

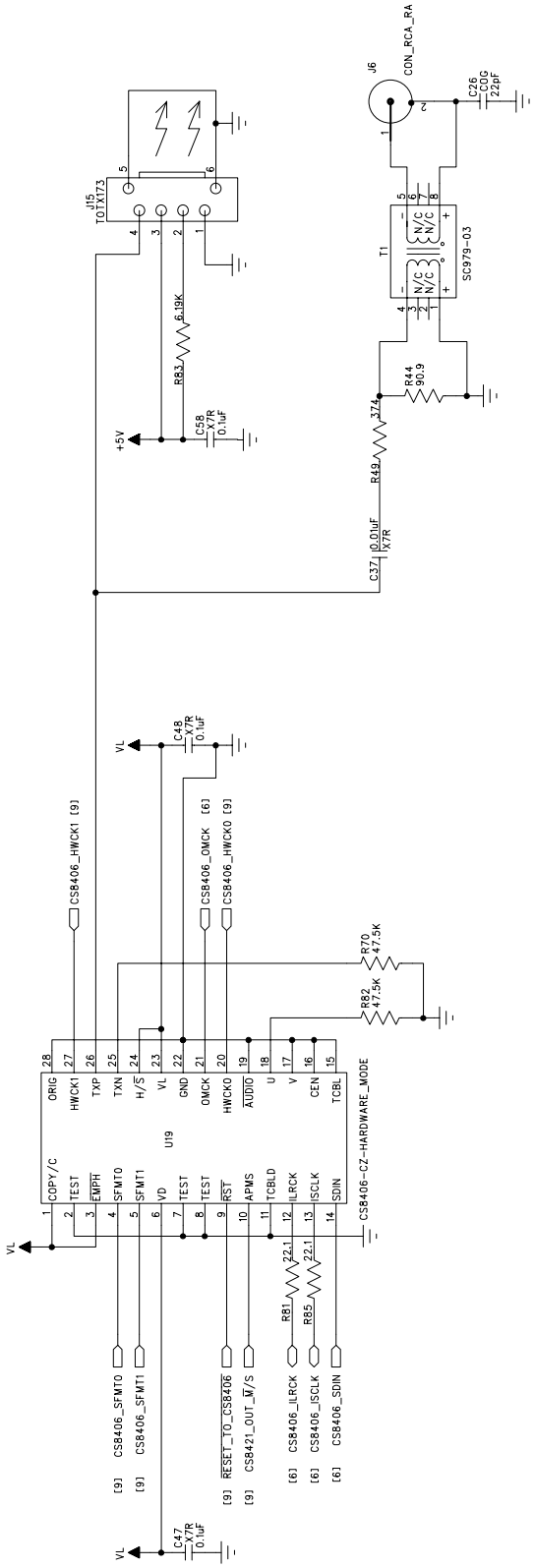


Figure 7. CS8406

CS8421 SAI Port M/S & Ratio Select (S1)

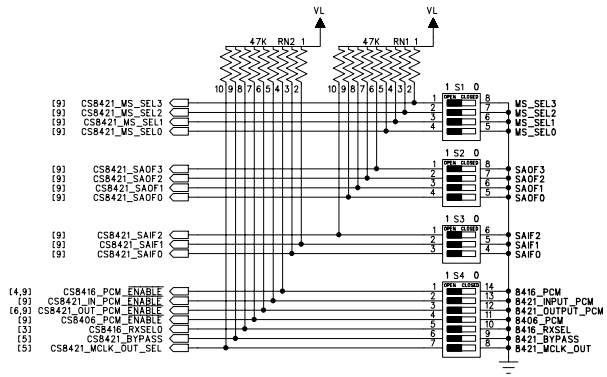
MS_SEL[3:0]	CS8421 Input	CS8421 Output
0000	Slave	Slave
0001	Slave	Master (128*Fs)
0010	Slave	Master (256*Fs)
0011	Slave	Master (384*Fs)
0100	Slave	Master (512*Fs)
1000	Master (128*Fs)	Slave
1001	Master (256*Fs)	Slave
1010	Master (384*Fs)	Slave
1011	Master (512*Fs)	Slave
All other switch settings are reserved		

CS8421 SAI Input Port Options (S3)

SAIF[2:0]	CS8421 Input Port Configuration
000	I2S up to 32-bit Data
001	Left Justified up to 32-bit Data
010	Right Justified 16-bit Data
100	Right Justified 20-bit Data
101	Right Justified 24-bit Data
110	Right Justified 32-bit Data
All other switch settings are reserved	

CS8421 SAI Output Port Options (S2)

SAOF[3:0]	CS8421 Output Port Configuration
0000	I2S 16-bit Data
0001	I2S 20-bit Data
0010	I2S 24-bit Data
0011	I2S 32-bit Data
0100	Left Justified 16-bit Data
0101	Left Justified 20-bit Data
0110	Left Justified 24-bit Data
0111	Left Justified 32-bit Data
1000	Right Justified 16-bit Data
1001	Right Justified 20-bit Data
1010	Right Justified 24-bit Data
1011	Right Justified 32-bit Data
1100	TDM Mode 16-bit Data
1101	TDM Mode 20-bit Data
1110	TDM Mode 24-bit Data
1111	TDM Mode 32-bit Data



BOARD SETUP (S4)

	OPEN	CLOSED
8416_PCM	PCM OFF	PCM IN/OUT
8421_INPUT_PCM	PCM OFF	PCM IN/OUT
8421_OUTPUT_PCM	PCM OFF	PCM IN/OUT
8406_PCM	PCM OFF	PCM IN/OUT
8416_RXSEL	COAXIAL	OPTICAL
8421_BYPASS	BYPASS SRC	SRC ACTIVE
8421_MCLK_OUT	OFF	ON

Figure 8. Mode Switches

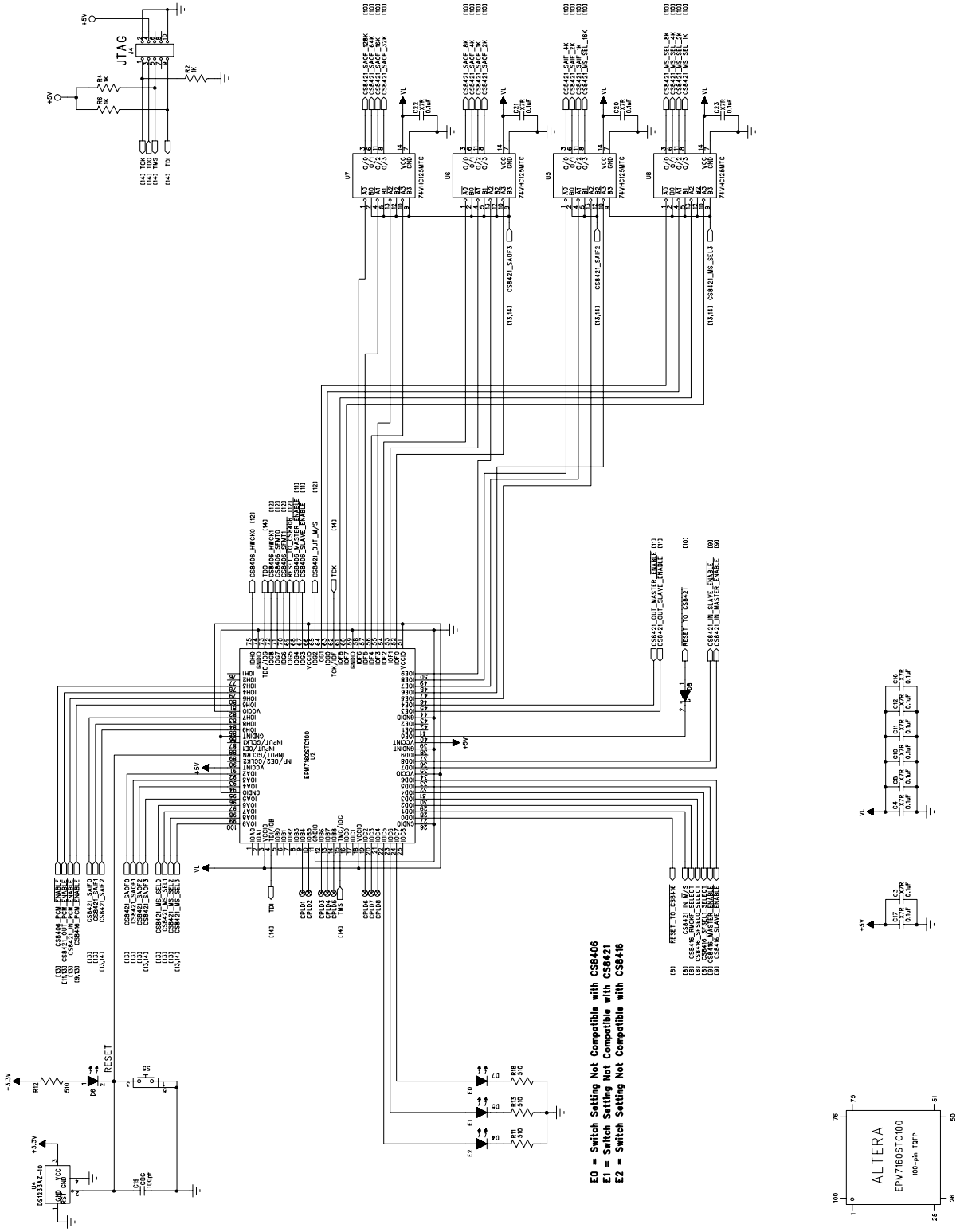


Figure 9. CPLD

4. LAYOUT

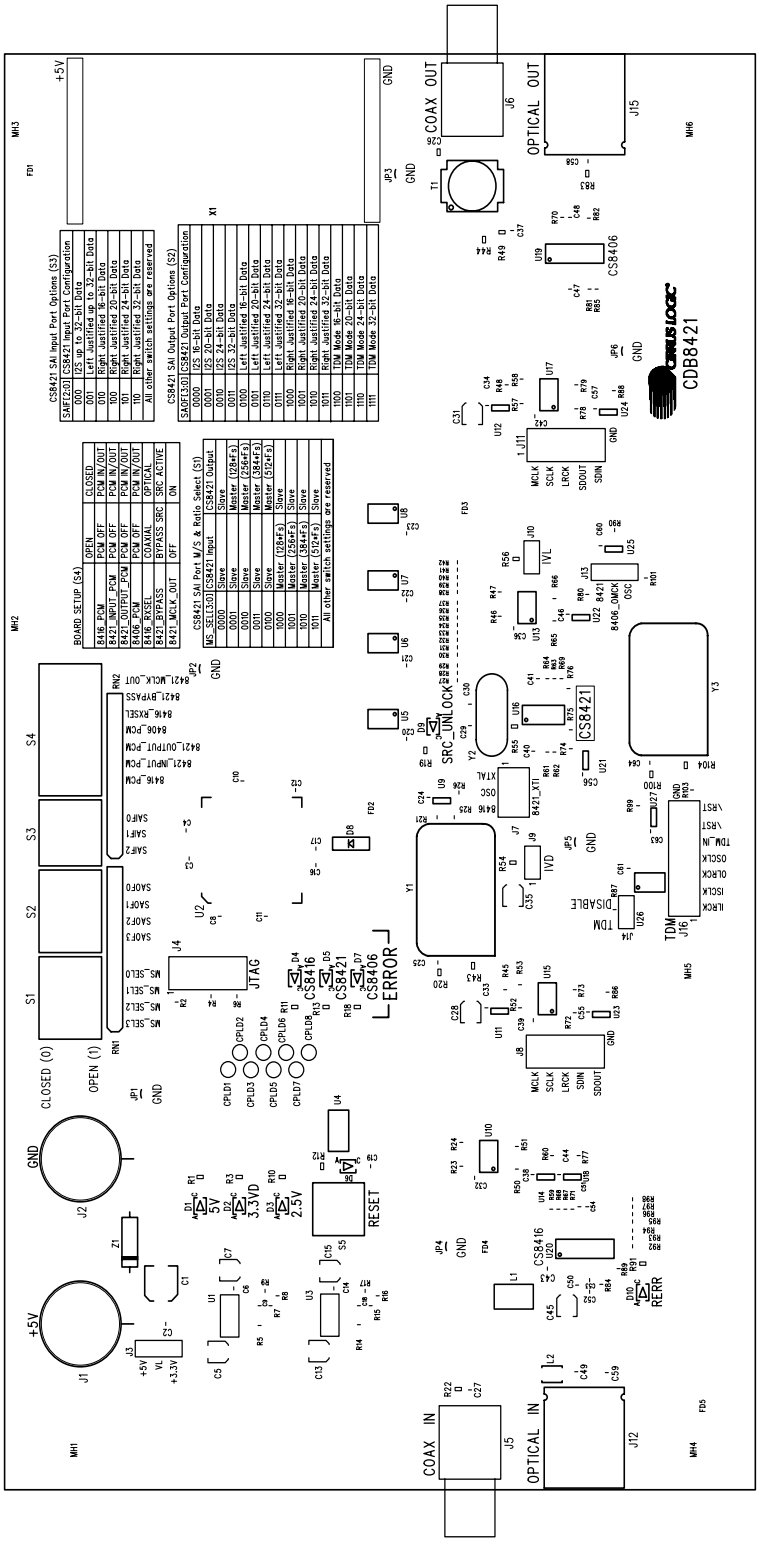


Figure 10. Silk Screen

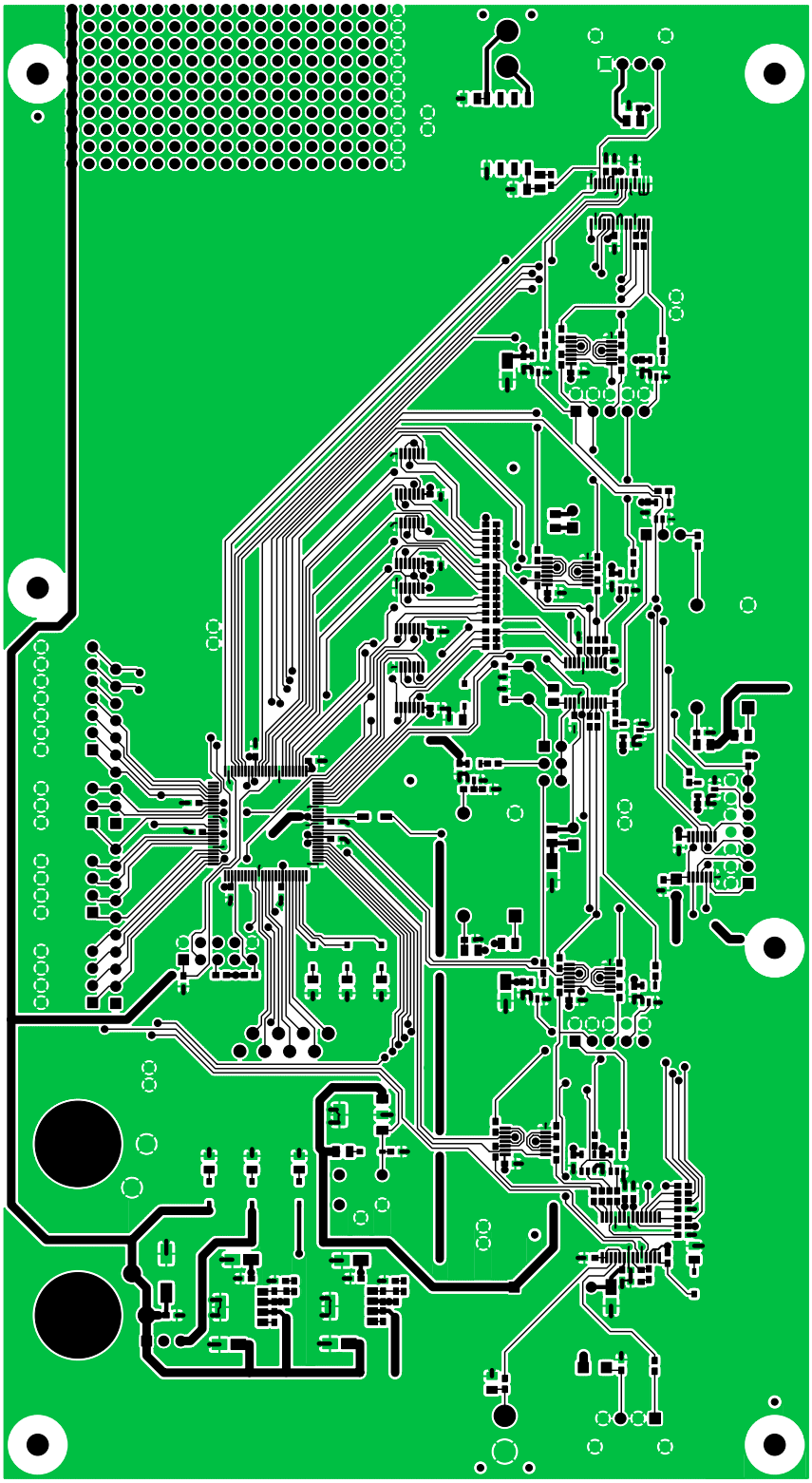


Figure 11. Topside Layer

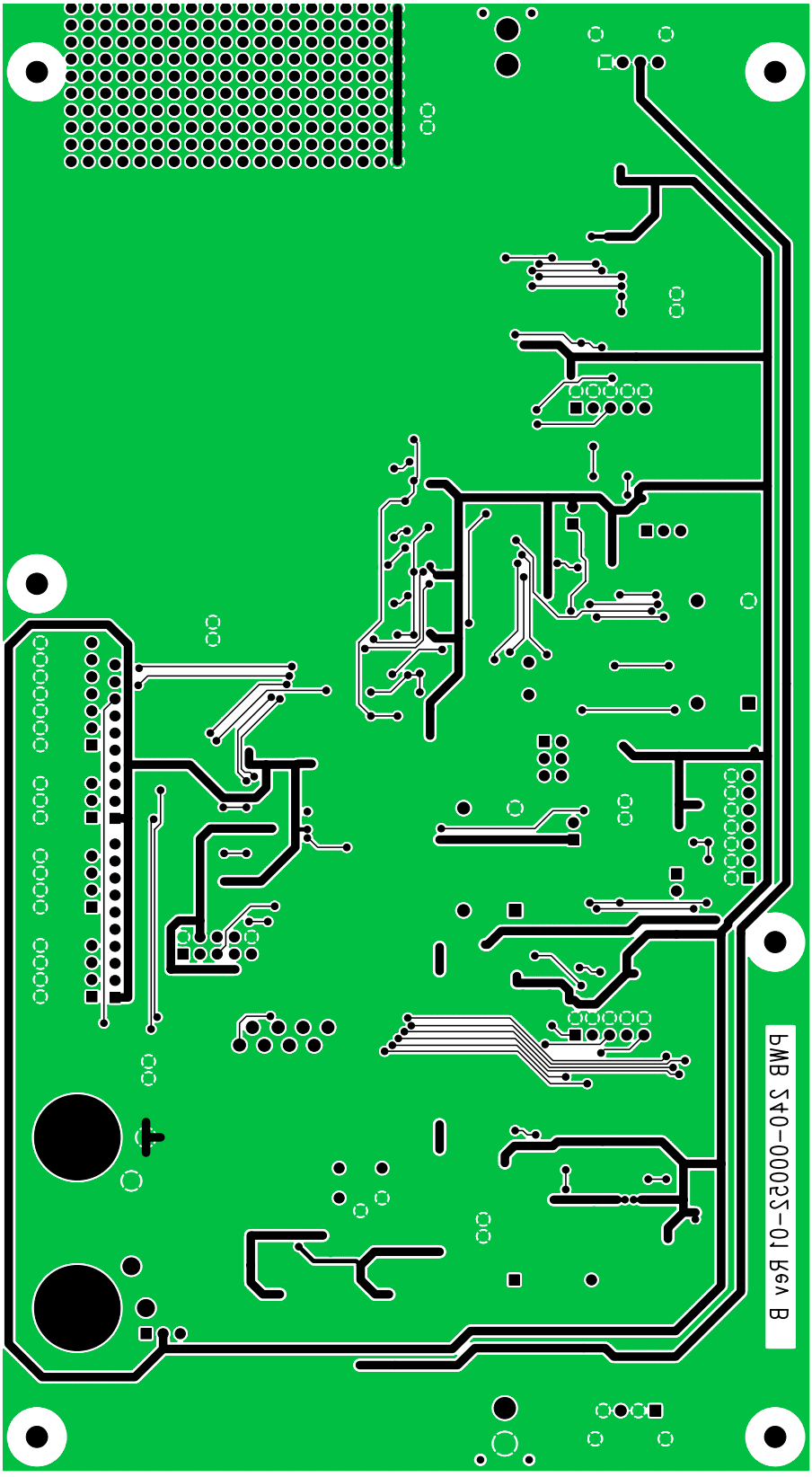


Figure 12. Bottomside Layer

5. APPENDIX A: CS8406 TCBL CONNECTION FOR THE CDB8421 REV. A

Pin 15 of U19 on the CDB8421 Rev. A has been lifted. This eliminates the connection to the TCBL pin on the CS8406 part. The pin should remain lifted and no connection to the pin should be reestablished for the board to operate properly. Changes have been made to CDB8421 Rev. B boards so that the pin need not be lifted.

6. REFERENCES

[1] **CS8421 - 32-bit, 192 kHz, Asynchronous, Stereo Sample Rate Converter web page:**
http://www.cirrus.com/en/products/pro/detail/P1082.html

[2] **CS8406 - 192 kHz Digital Audio Transmitter web page:**
http://www.cirrus.com/en/products/pro/detail/P1009.html

[3] **CS8416 - 192 kHz Digital Audio Receiver web page:**
http://www.cirrus.com/en/products/pro/detail/P1005.html

7. REVISION HISTORY

Release	Date	Changes
DB1	October 2004	1st Release
DB2	November 2004	Corrected figure caption on page 10.
DB3	November 2004	2nd Release -Updated “Schematics” on page 9 and “Layout” on page 17. -Updated “References” on page 21.

Table 8. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**